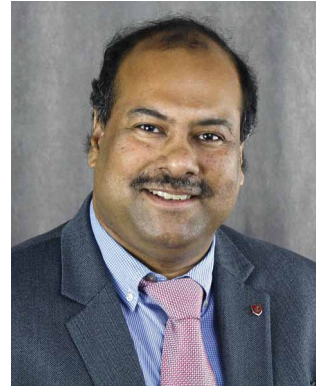


From the EIC



Special Issue on Testability and Dependability of Artificial Intelligence Hardware

■ **THE ARTICLES IN** this issue are divided into two groups: 1) the first group comprises articles that make up the Special Issue on Testability and Dependability of Artificial Intelligence Hardware and 2) the second group consists of general interest articles.

The highlight of this issue is the Special Issue on Testability and Dependability of Artificial Intelligence Hardware. There has been plethora of recent investigations on designing novel hardware architectures for artificial intelligence/machine learning (AI/ML) applications. Though achieving high performance and energy efficiency for the hardware architecture is of paramount importance, testability and dependability of these new architectures need to be addressed before the mainstream adoption. This special issue consists of seven articles from both academia and industry addressing the broad topic of testability and dependability of emerging AI hard-

ware architectures. We thank the guest editors, Fei Su, Chunsheng Liu, and Haralampos-G. Stratigopoulos, for making this special issue possible.

In addition, we present three general interest articles, titled as follows: 1) “Using STLs for Effective In-Field Test of GPUs”; 2) “T-Topology Coupler-Based Bandpass Negative Group Delay Active Circuit Design and Test”; and 3) “FPGA-Chain: Enabling Holistic Protection of FPGA Supply Chain With Blockchain Technology.”

This issue also contains a report on the 2022 International Conference on Computer-Aided Design (ICCAD) written by Tulika Mitra.

Many thanks to Scott Davidson for The Last Byte article titled “Is There an Answer?”

I hope you enjoy reading this issue of *IEEE Design&Test*.

■

A handwritten signature in black ink, appearing to read 'P. Pande'.

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Digital Object Identifier 10.1109/MDAT.2023.3243862
Date of current version: 10 March 2023.