Conference Report

The 41st IEEE VLSI Test Symposium

Naghmeh Karimi
University of Maryland Baltimore County
Baltimore, MD 21250 USA

The 41st IEEE VLSI Test Symposium (VTS) was held in San Diego, CA, USA, on 24–26 April 2023. This venue was the first in-person one since the COVID-19 pandemic. VTS is one of the premier conferences focusing on test, reliability, and security challenges in VLSI circuits. Following the same trend as prior years, VTS was arranged in three days and captured a set of research and innovative practice (IP) sessions, keynotes, panels, embedded tutorials, and doctoral thesis competitions for a total of 31 sessions.

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VTS'23 featured three inspiring keynotes. On the first day, Dr. Subi Kengeri who is the vice president of Artificial Intelligence (AI) Systems Solutions at Applied Materials discussed the heterogeneous integration in the AI era. On the following day, Dr. Madhavan Swaminathan of Penn State University shared his thoughts on semiconductor packaging and heterogeneous integration. Finally, the third keynote given by Dr. Lorie Burmood, Director of Operations at NXP Semiconductors, featured MEMS development and test.

The conference included two embedded tutorials—one on the hardware design and reliability of binary Bayesian reasoning, and the other on the efficient hardware architectures of binary neural networks. Moreover, two panels were scheduled: one on the test and design-for-test (DFT) in the area of the chip and the other on test challenges.

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A total number of 72 submissions were received from 13 countries. The top five contributing countries in terms of submissions were the United States, China, Taiwan, India, Germany, and the Republic of Korea. In particular, the United States' contribution was around 40.2% of the submissions. On average, each submitted paper received 4.3 reviews given by 75 technical committee members from all over the world, and eventually, 24 papers were selected for oral presentation.

In parallel to the eight regular sessions devoted to the selected 24 papers, VTS included nine special sessions covering a broad range of research in the design, reliability, testing, security, and fault tolerance areas. These sessions totally included 27 research papers. In addition, VTS'23 covered six IP sessions on the topics of functional safety, silicon lifetime management, telemetry monitoring, chiplet design and test, silicon debug, and dependability of GPU, HPC, and autonomous systems.

VTS'23, similar to its prior venues, held the E. J. McCluskey TTTC best doctoral thesis competition where 13 PhD students competed in the North American semifinal competition. The final competition will be held at the International Test Conference (ITC) 2023 which will be held in Anaheim in October 2023.

The success of the 41st VTS would not have been possible without the dedication of many volunteers, including a year-round effort from the 26 organizing committee members and months of hard work of 75 technical program committee members. VTS'23 also thanks the corporate supporters including SYNOPSYS, ADVANTEST, and SIEMENS.

Similar to previous venues of VTS, two achievement awards were announced in VTS'23. The 40th VTS Symposium (VTS'22) was selected as the most TTTC successful technical award, and the 2nd IEEE Silicon Lifecycle Management (SLM held at DATE'22 and ITC'22) was selected as the most populous technical meeting of the previous year. In addition, "Fast RF Mismatch Calibration Using Built-In Detectors" authored by Muslum Emir Avci, Sule Ozev, and Chethan Kumar Y. B. was selected as the best paper of VTS'22.

The 42nd VTS will be held in Tempe, AZ, USA, on 22–24 April 2024. ■

Naghmeh Karimi is an associate professor at the University of Maryland Baltimore County, Baltimore, MD 21250 USA. She leads the SECure, Reliable, and Trusted Systems (SECRETS) research lab. She serves as an associate editor of *Springer Journal of Electronic Testing: Theory and Applications (JETTA)* and *IEEE Design&Test*. She has been the corresponding guest editor of IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS); special issue in Hardware Security in Emerging Technologies. Her current research interests include hardware security, VLSI testing, design-for-trust, design-for-testability, and design-for-reliability. Karimi received a PhD in computer engineering from the University of Tehran, Tehran, Iran. She is a Senior Member of IEEE.

■ Direct questions and comments about this article to Naghmeh Karimi, University of Maryland Baltimore County, Baltimore, MD 21250 USA; nkarimi@umbc.edu.