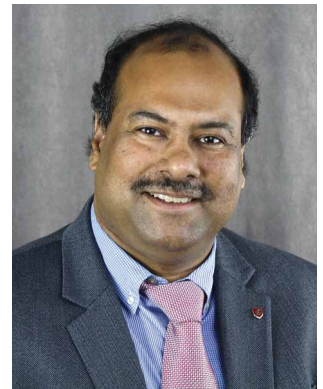


From the EIC

Robust and Secure Systems



■ **THIS ISSUE CONSISTS** of general interest articles. We also have one conference report in this issue.

The seven general interest articles covering varied topics starting from test and fault tolerance to security to design of energy-efficient systems. All these topics are of great interest to the *IEEE Design&Test* readers. The titles of these articles are as follows: 1) “Conventional Tests for Approximate Scan Logic” [A1]; 2) “Impact of Orientation on the Bias of SRAM-Based PUFs” [A2]; 3) “A BIST Approach to Approximate Co-Testing of Embedded Data Converters” [A3]; 4) “Side Channel and Fault Analyses on Memristor-Based Logic In-Memory” [A4]; 5) “Efficient Aspect Verification and Debugging of High-Performance Microprocessor Designs” [A5]; 6) “Testing for Multiple Faults in Deep Neural Networks” [A6]; and 7) “Voltage–Resistance-Adaptive MPPT Circuit for Energy Harvesting” [A7].

This issue also contains the ASPDAC 2024 conference report.

Many thanks to Scott Davidson for The Last Byte remembering Prof. Niklaus Wirth, the inventor of the programming languages Pascal and Modula.

I hope you enjoy reading this issue of *IEEE Design&Test*. ■

Appendix: Related Articles

- [A1] I. Pomeranz, “Conventional tests for approximate scan logic,” *IEEE Des. Test*, vol. 41, no. 3, pp. 5–13, May/Jun. 2024.
- [A2] Z. U. Abideen et al., “Impact of orientation on the bias of SRAM-based PUFs,” *IEEE Des. Test*, vol. 41, no. 3, pp. 14–20, May/Jun. 2024.
- [A3] K. Bhatheja et al., “A BIST approach to approximate co-testing of embedded data converters,” *IEEE Des. Test*, vol. 41, no. 3, pp. 21–28, May/Jun. 2024.
- [A4] P. Inglese, E.-I. Vatajelu, and G. Di Natale, “Side channel and fault analyses on memristor-based logic in-memory,” *IEEE Des. Test*, vol. 41, no. 3, pp. 29–35, May/Jun. 2024.
- [A5] A. Joseph, “Efficient aspect verification and debugging of high-performance microprocessor designs,” *IEEE Des. Test*, vol. 41, no. 3, pp. 36–46, May/Jun. 2024.
- [A6] D. A. Moussa, M. Hefenbrock, and M. Tahoori, “Testing for multiple faults in deep neural networks,” *IEEE Des. Test*, vol. 41, no. 3, pp. 47–53, May/Jun. 2024.
- [A7] Z. Zhang, “Voltage-resistance-adaptive MPPT circuit for energy harvesting,” *IEEE Des. Test*, vol. 41, no. 3, pp. 54–62, May/Jun. 2024.

Partha Pratim Pande, *Editor-in-Chief*
Washington State University
Pullman, WA 99164-2752 USA

Digital Object Identifier 10.1109/MDAT.2024.3373750

Date of current version: 24 April 2024.