Noise Generation and Coupling Mechanisms in Deep-Submicron ICs

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On-chip noise generation and coupling is an important issue in deep-submicron technologies. Advanced IC technology faces new challenges to ensure function and performance integrity. Selecting adequate test techniques depends on the circuit, its implementation, and the possible physical failures and parasitic coupling models. This new demand for test technology practices precipitated the investigation of *dI*/*dt* and *dV*/*dt* noise generation and propagation mechanisms.

The impact of noise and coupling mechanisms on IC performance is different from that related to traditional failure mechanisms on which test technology efforts have recently focused. Testing techniques for noise will extend the domain of conventional test approaches to mixed parametric and functional test strategies. The *dI*/*dt* and *dV*/*dt* noise generation (switching noise) and propagation mechanisms address this larger domain of test approaches.

Simultaneous switching noise

Simultaneous switching of multiple digital gates demands large transient-current spikes. These spikes cause simultaneous switching noise (SSN), also known as *dI*/*dt* noise, power supply noise, or ground/power bounce. The package V_{DD} pin introduces series resistance R_{VDD} and inductance L_{VDD} in the path from the external power supply to the on-chip power supply. For a single gate, the transient voltage at the power supply due to resistive and inductive effects is given by

$$V_{DD\_on\text{-}chip} = V_{DD} - R_{VDD}I_{DD} - L_{VDD}(dI_{DD}/dt)$$

The second term in the expression is a transient *IR* drop on the on-chip V_{DD}, and the third term is the *dI*/*dt* noise; transient current pulse I_{DD} causes both. The return path of I_{DD} passes through the V_{SS} package pin, closing the loop and generating a positive spike at the on-chip V_{SS} node due to V_{SS} pin inductance and resistance, as Figure 1 (next page) shows. The overall effect of the switching current is a transient reduction of the on-chip power supply voltage ($V_{DD\_on\text{-}chip} - V_{SS\_on\text{-}chip}$) due to both the *IR* drop and *dI*/*dt* noise. The current's time derivative, for well-sized logic gates, is proportional to the input rise or fall time and the transistors' maximum saturation current.

When multiple gates switch simultaneously, the individual switching currents combine to increase the amount of SSN. The reason output driver gates switch simultaneously is that all of an output bus' nodes should switch at once. For core logic cells, the different propagation paths found have a Gaussian path delay distribution.

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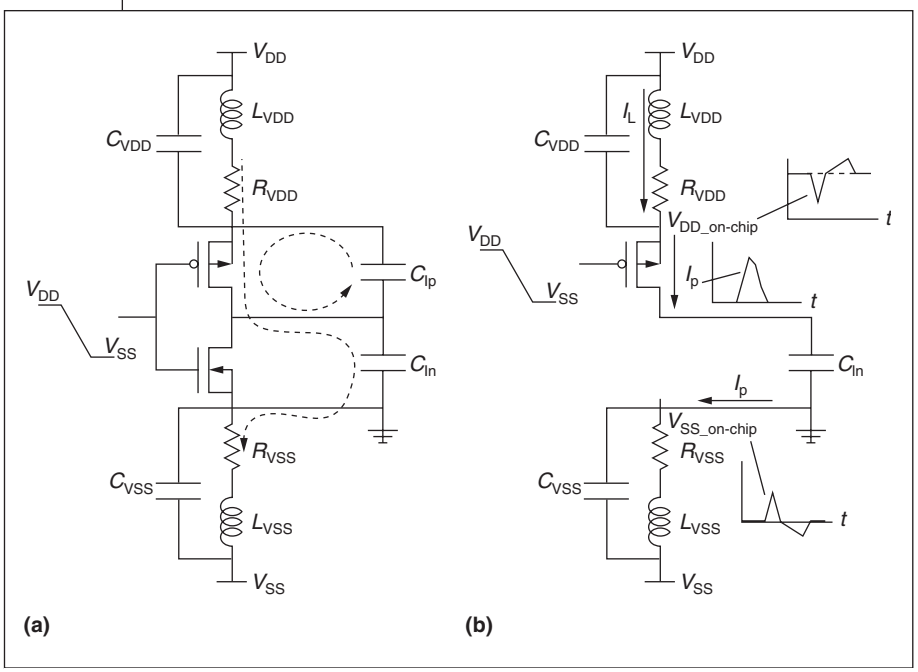

Figure 1. Circuit model and switching current paths in a simple combinational gate (a), and waveforms of the current in the transistor branches and the V_{DD} at the chip node for a high-to-low transition (b).

Table 1. Average inductance per pin for different packages and bonding systems.

Package/ bonding system*	Average inductance per pin (nH)
DIP 68 pins, plastic	35.0
DIP 68 pins, ceramic	20.0
SMT 68 pins	7.0
PGA 68 pins	7.0
PGA 256 pins	15.0
QFP 44 pins	2.5
DIP 18 pins, plastic	13.7
SOIC 18 pins	8.5
QSOP 18 pins	3.6
BGA	3.0
Wire bond	1.0 to 2.3
Solder ball	0.1

* BGA: ball grid array; DIP: dual inline package; PGA: pin grid array; QFP: quad flat package; QSOP: quarter-sized outline package; SMT: surface mount technology; SOIC: small outline IC

To improve system performance and maximize clock frequency, this path delay distribution is made as narrow as possible. However, this practice increases simultaneity because most paths have similar delays, and the gates along those paths switch almost simultaneously. Increasing the system's degree of parallelism increases the logic's degree of simultaneity and, consequently, increases SSN. One way to reduce the simultaneity is to make the propagation path delay distribution uniform instead of normal, using regular logic structures and self-timed logic.

SSN reduction techniques

Reducing the package pins' parasitic impedance is the simplest way to minimize SSN. Table 1 shows typical pin inductance values for several packaging systems. Multiple pins and bonding wires for the power supply connection can reduce the total power supply inductance in a given package. For example, the Intel Xeon microprocessor has 190 V_{DD} (power) pins and 189 V_{SS} (ground) pins, representing 63% of the total 603 package pins.

In a complex digital circuit, the parasitic capacitance of the nonswitching gates, the parasitic capacitance between the positive power supply metal lines and the substrate, and the parasitic capacitance between the n-wells and the substrate all contribute to form an on-chip decoupling capacitance between $V_{DD\_on\text{-}chip}$ and $V_{SS\_on\text{-}chip}$. This capacitance provides part of the current required to charge or discharge the switching gates' output nodes, and so reduces SSN. To further reduce SSN, designers place additional on-chip decoupling capacitance on chip. On-chip decoupling capacitors for modern microprocessors are on the order of several hundreds of nanofarads and can occupy up to 10% of the chip total area. The total on-chip decoupling capacitance forms a resonant circuit with the package power supply pins' inductance and resistance. SSN produces a damped oscillation at the resonance frequency of the package chip system. Designers must take special care in the design of the overall on-chip power supply decoupling to place the resonant frequency far away from the system clock fre-

quency and to include enough damping to avoid SSN accumulation from one clock cycle to the next.

For complex deep-submicron designs with very small feature sizes, fast switching speeds, and high circuit density, on-chip power supply voltage drop from *dI*/*dt* noise is comparable to the *IR* drop. The on-chip power bus inductance is important, in addition to the package inductance.[1] Therefore, the on-chip power supply is not the same across the chip. Adequate sizing and routing of the power buses and placement of distributed on-chip decoupling capacitances are the most effective techniques to maintain on-chip power supply variations under control. This is also a crucial issue in mixed-signal ICs, where isolation of digital and analog power supplies is necessary to avoid coupling of digital noise to the chip's analog sections.

SSN effects and testing

Excessive SSN introduces additional signal delay, causes false switching of logic gates, and, in mixed-signal ICs, affects the performance of the analog and RF sections. For example, sampling operations or frequency synthesis are two digitally controlled analog functions. SSN noise can couple to the circuits that generate the synchronization signals for those functions and produce phase noise. SSN originates clock jitter in high-speed and high-accuracy digital-to-analog converters that raises the noise floor and produces distortion at the output, worsening the signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR). SSN also contributes to phase noise in phase-locked loops for clock recovery in high-speed digital circuits or for frequency synthesis in RF transceivers.

Delay testing can detect SSN effects on digital circuits.[2] A voltage drop of 10% to 15% due to SSN during a logic cell's output switching can cause an increase in the cell propagation delay of 20% to 30%. Finding the input vector sequence that maximizes SSN generation is one of the most important concerns for SSN testing. Researchers are pursuing several approaches to find the worst-case SSN by selecting the appropriate set of input vectors. Some selection methods use static timing analysis;[3] high-level circuit simulations use simple models for the logic cells and the power supply distribution.[4] These approaches require accurate models of switching-signal timing, as well as prior knowledge of the circuit's physical implementation.

Interconnect coupling

Parasitic coupling between adjacent interconnect lines is a major limiting factor in deep-submicron ICs. The coupling causes the injection of noise from active lines to near lines. This mechanism of noise coupling is called *crosstalk*.

Circuit modeling

A complete model for crosstalk must reflect the electromagnetic behavior of signal propagation, and this corresponds electrically to a distributed *RLC* model. However, there are many practical situations in which a lumped capacitive model can accurately describe an on-chip line coupling to predict the crosstalk-induced noise. Assigning an appropriate coupling model in the design stage is important to avoid significant under- or overestimation of the crosstalk effect, which would lead to inefficient or malfunctioning circuits. It is also important to choose a model that is simple enough to make basic design rules for implementation in automatic routing tools, which must check thousands or hundreds of thousands of nodes.

The nature of coupling is either simple capacitive (*C*, where *dV*/*dt* of the signal is important), or capacitive-inductive (*LC*, where both *dV*/*dt* and *dI*/*dt* are important). In addition, the interconnect model can have either distributed or lumped parameters. Designers must consider three factors when selecting a crosstalk model: signal rise time, driver resistance, and line resistance. The following example illustrates the influence of these factors.

Suppose two 1-mm-long lines of a (0.5×0.5)-micron cross section are separated by 1 micron with a ground line 10 microns away from one of them, as Figure 2 (next page) shows. The process involves computing the *L* and *C* parameters, obtaining the characteristic impedance for each line (128 ohms and 135 ohms), and calculating and simulating its propagation time (15 ps/mm). The three factors influence the nature of coupling, as the HSpice simulation results in Figure 3 (next page) show.

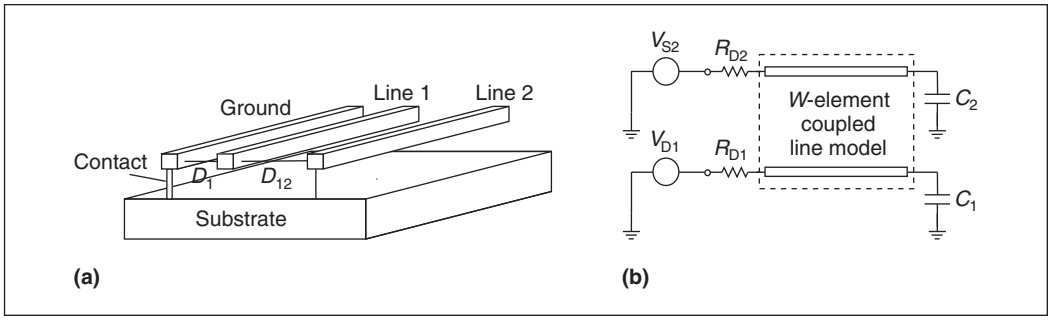

Figure 2. Geometry of a typical interconnect line (a), where D_1 = 10 microns, and D_{12} = 1 micron; circuit used in the HSpice simulations with parameters obtained from the previous line structure (b).

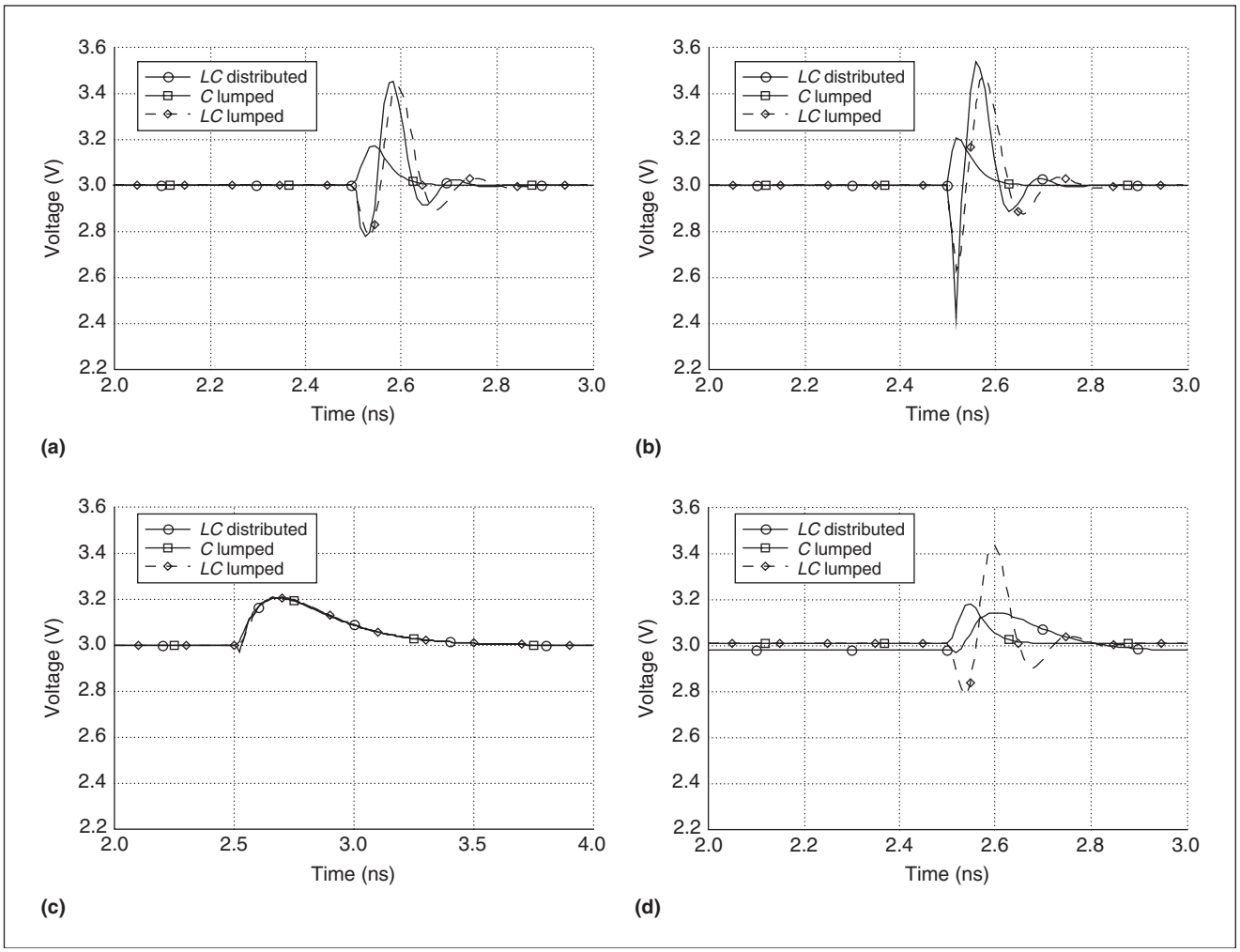

Figure 3. Four cases, from HSpice simulations with the same coupled lines and different driver and signal parameters. In each section, the figure shows the waveform for three different models of coupling (distributed *LC*, lumped *C*, and lumped *LC*): a transition of a 40-ps rise time, with R_{D1} = 100 Ω and R_{D2} = 100 Ω, makes the lumped *C* model sufficient (a); a low resistance (R_{D1} = 100 Ω and R_{D2} = 100 Ω) and a shorter rise time (30 ps) requires a distributed *RLC* model (b); the same conditions as in (b), but with a high drive resistance (R_{D1} = 800 Ω, R_{D2} = 800 Ω), make a lumped *C* model sufficient (c); and the same conditions as (a), but with a lossy line, cause capacitive coupling (the lumped models do not include line resistance), and once again the lumped *C* model is sufficient (d).

Technology trends

The trend of increasing the integration level of ICs has a negative impact on interconnect performance. The reason is twofold: First, the cross section is smaller in the scaling-down process, and this increases the line's resistance. The aspect ratio (thickness to width) is larger than 1 to reduce resistance while maintaining high horizontal interconnect density, but this trend increases the coupling capacitance. Second, the spacing between lines is smaller, and therefore the effective capacitance increases. This increase, along with the increase in line resistance, causes an increase in the *RC* constant, and, consequently, in the delay. In addition, crosstalk between lines due to mutual capacitance and inductance becomes worse.

Two technological solutions can alleviate these problems. One is the use of low-resistivity lines (copper-based alloys instead of aluminum), and low-permittivity dielectric materials instead of silicon dioxide, to reduce capacitance. The other solution is reverse scaling of the upper levels of interconnects, presenting a far greater cross section.

Both the use of new materials and reverse scaling increase the importance of inductive coupling, which does not depend on materials but on the return current path, and does not scale proportionally with capacitance and resistance. The upper levels are in principle further from a reference (the lower levels shield them from the substrate) and therefore present a higher characteristic impedance. In addition, these are the levels reserved for long global interconnects, and consequently the drivers must have a low equivalent resistance to reduce the signal switching time. The combination of these characteristics tends to favor the inductive nature of coupling for upper interconnect levels.

Test issues

Crosstalk causes two effects: an unwanted pulse (spurious signal) in a quiet line, and a change in transition delay in a switching line. The magnitude of these perturbations depends on the values of the electrical parameters involved: lines, drivers, and load capacitances.

An on-going argument is whether coupling effects are a design or a test issue. Although avoiding crosstalk-related problems is important in the design stage, the complexity of present chips implies the analysis of hundreds of thousands of interconnects. Only simplified models can perform this analysis on a reduced number of interconnect groups that are potential candidates for important crosstalk effects. Even when these necessary simplifications are close to reality, process parameter fluctuations may induce an increase in the effect previously calculated, which will only appear in the field. Therefore, efficient test methods must consider crosstalk as a detectable fault.[5]

Separate test strategies are necessary to address the two crosstalk effects. The first effect, a spurious signal, is analogous to an extension of the classical D fault, which propagates until it reaches a primary output. Thus, standard algorithms, like Podem, can adapt to generate suitable test patterns for crosstalk.[6] These algorithms try to find a pair of vectors for each analyzed crosstalk fault such that the transition causes a maximum effect, preferably by simultaneous switching of several nodes coupled to the same victim. Layout information is necessary to generate a realistic list of target faults. The difficult part is deciding what constitutes a maximum effect, as this depends on the dynamic noise immunity of the subsequent gates. The second vector allows propagation through the most favorable path in terms of spurious signal propagation. The spurious signal has limited width and amplitude, and therefore has a limited propagation capability, which depends both on the spurious signal waveform and on the subsequent gates' susceptibility.[7] For example, imagine a spurious signal in node X and two possible logic paths, P1 and P2, to a primary output (PO). The effect of the spurious signal at the PO might be negligible if it propagates, say, through path P1, whereas it may cause a logic error if it propagates through path P2. Then if the test vector sensitizes path P1, the algorithm would not detect a fault even though the circuit could still be faulty. It is important to assign a meaningful cost function to choose between the different paths.[8]

With respect to crosstalk-induced delay, the existing algorithms are based on test strategies for delay faults. As in the case of spurious signal detection, a two-vector pattern generates

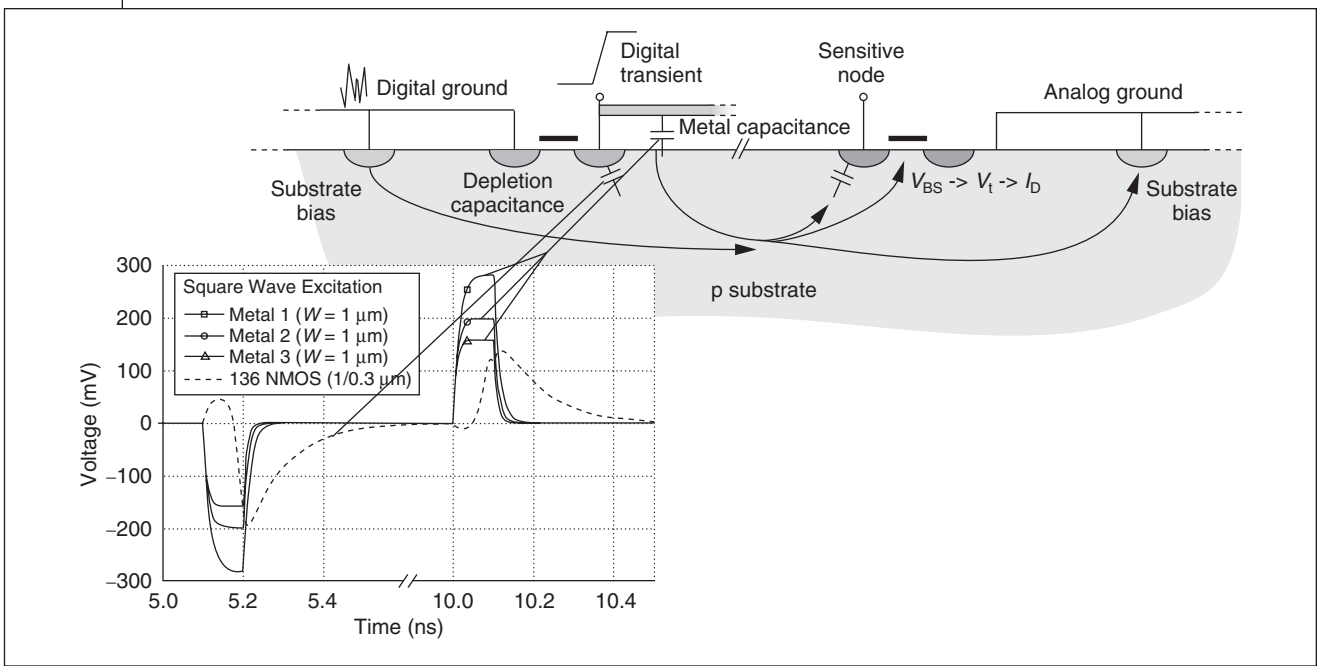

Figure 4. Schematic diagram showing the mechanisms of substrate noise generation and reception. The waveforms compare the magnitude of noise injection from interconnects against noise from NMOS transistors.

the induced fault by causing simultaneous (or almost simultaneous) transitions in a victim line and one or more affecting lines. A path that maximizes coupling's effect using back-trace and backtrack procedures generates the delayed transition in the victim line.

Substrate coupling

Noise coupling through the common substrate in silicon technologies has become an important problem in mixed digital/analog and RF circuits. Its distributed nature has made its treatment and solution difficult.

Sources of substrate noise

Figure 4 shows schematically how noise couples to the substrate in a mixed-signal circuit. Noise generators include switching devices (both through depletion capacitances and impact ionization currents), substrate contacts, and switching interconnects. At the receiving end, substrate fluctuations affect a sensitive device through parasitic capacitances and body effect. Concerning the propagation path, CMOS technology uses two different types of wafers. Pure digital technologies use highly conductive (about 10 mΩ-cm) substrates, named epi-P+, with a thin, epitaxial, resistive layer on top. In these substrates, noise penetrates the epi layer and propagates basically on top of the conductive bulk, with negligible attenuation with distance. The advent of high-frequency analog circuits again favors substrates, named P–, that have a uniform high resistivity (about 10 Ω-cm). Here noise current densities are higher near the surface, decreasing more deeply inside the low-conductive substrate. Experimental results with a mixed-signal test circuit show that an epi-P+ substrate propagated three times as much noise as a P– substrate.[9] Special packaging and grounding techniques can reduce or reverse this ratio.

To reduce substrate noise, the dominant noise generators must first be identified. Impact ionization currents are about an order of magnitude lower than currents introduced through depletion capacitances.[10] In a mixed-signal circuit, the switching noise introduced through the biasing contacts is usually the most important source of substrate noise.[1] Substrate extraction tools usually ignore noise coupled from interconnects. To calibrate the importance of this noise source, Figure 4 shows simulation results comparing noise from interconnect lines to noise from

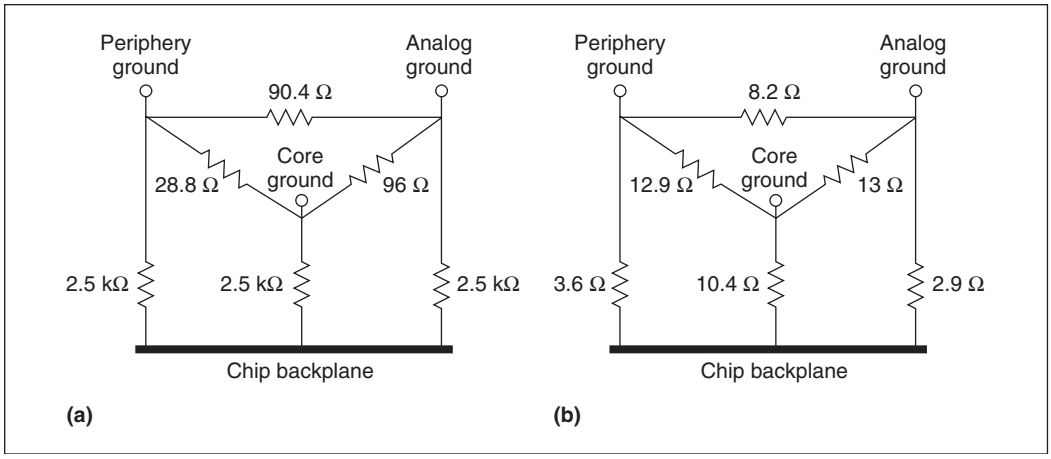

Figure 5. Resistances measured between the different ground nodes and the chip backside, in a mixed digital-analog circuit, manufactured in a P– wafer (a) and an epi-P+ wafer (b).

switching NMOS transistors. In both cases, we extracted and simulated a simple test layout, and used the SubstrateStorm tool to extract substrate parasitics.[11] We first measured the noise that 1-micron-wide, 500-micron-long lines injected. Then we replaced the lines by an array of 136 minimum-size NMOS transistors switching simultaneously. The same square signal with a 0.1-ns rise/fall time drives either the lines or the transistors. We used a 0.35-micron BSIM3 model for the transistors, and we modeled each 1-micron segment of the interconnects as an *RCR* circuit. Figure 4 shows that the noise the lines injected is larger than the noise that the 136 inverters injected, even for the top metal-3 lines.

Techniques to reduce substrate noise effects

Three different perspectives address substrate noise reduction:

- Design the sensitive circuitry so that it is immune to noise.
- Reduce the amount of noise generated and injected to the substrate.
- Keep the noise from reaching the sensitive parts by either using passive barriers or eliminating the noise by sinking it to ground.

Using well-known differential or high-PSRR topologies helps maximize the immunity of analog circuits. In fact, noise that analog power supplies pick up can be far more important than noise coupled directly to transistors, because the circuit can have large area contacts that connect to the analog ground (such as standard I/O pads). But noise amplitude is not the only sensitive parameter.

In sampled circuits, the synchronicity between the analog-signal sampling instant and the noise generation instant is also important. A noise pulse might not affect a given circuit unless it arises at some critical moments. For RF circuitry, the frequency constraint is more important than the timing constraint. Here noise might not affect the victim unless its frequency content overlaps the bands of interest. The noise spectrum contains fundamental clock frequencies and harmonics, as well as resonance frequencies that the package and internal circuitry produces. It is possible therefore to design the global characteristics of a system on a chip so that the noise and RF signal spectrums are compatible.

In several evaluation circuits, pad cells are the main vehicles of noise coupling in the system. These cells have large areas for substrate biasing and diode protection. Several of these pads can easily provoke a virtual short circuit between the different supplies in the circuit, making any layout technique that increases isolation useless. As a reference, we measured resistances between the grounds (analog, core, and periphery) of a mixed-signal circuit with a total of 21 analog and 18 digital pads, all of them taken from standard libraries.[9] Figure 5 shows the results. Resistances between grounds

are only a few tens of ohms for the circuit manufactured in a P– wafer, and a few ohms in the case of an epi-P+ wafer.

In these conditions, it's worth reconsidering duplication of the digital supplies (core periphery) because the substrate cancels out the desired isolation. On the other hand, digital output drivers are one of the main sources of switching noise. Techniques such as limiting voltage transient speeds, avoiding the strict simultaneity of switching, or using balanced or current mode signal transmission can minimize these effects.

Researchers have proposed several techniques to isolate a circuit's sensitive parts from its noisy ones. Wells are typically useless, due to their large areas. Shallow reverse-biased junctions and oxide trenches are a better option, although they are limited to avoiding propagation in the channel stopper and near the surface. An ideal solution, despite its cost, is silicon-on-insulator technology, which designers are beginning to use for analog and RF applications.

A different approach to avoid noise reaching sensitive parts is to collect disturbances to ground. This includes using classical layout techniques such as guard rings or using Kelvin (dedicated) grounds for substrate biasing. Nevertheless, layout techniques at the circuit core are completely useless if there is a lower impedance path through the pad periphery, the scribe line, or the bulk in epi-P+ wafers. Even if the main noise path is in the circuit core, noise can efficiently collect to ground only if a very low impedance path is made available. At high frequencies, this means using extremely low-inductivity packages and bonding. Another option for noise sinking is to take advantage of the conductive bulk of epi-P+ wafers, which can be grounded from the backside and serve as a low-impedance noise collector. Figure 5 also shows the measured resistances between the different surface ground nodes and a chip backplane (including die attachment). The resistances across the epi-P+ wafer are extremely low. Unfortunately, the potential advantage of this approach is lost if bonding wires must ground the backplane. Today, new packages with exposed pad technology allow direct connection of the chip backside to PCB ground, thus giving a renewed attraction to this approach.

SWITCHING NOISE (dI/dt and dV/dt) has become an important source of problems in modern ICs. Its impact will increase in future deep-submicron technologies, as transient times are reduced below 100 ps and circuit complexity increases. The common substrate and interconnects easily couple these sources of noise to other parts of the chip. Switching-noise effects in digital circuits range from false switching to delay faults, and in analog circuits can affect the performance directly or through other types of noise like phase noise or clock jitter. From a test viewpoint, these effects constitute a fault in circuit performance. Although designers can use CAD tools to analyze the magnitude and effects of noise during the design phase, the extreme complexity of circuits avoids a detailed prediction of all the possible problems. New testing strategies should screen out defective circuits that don't meet performance demands because of switching-noise problems, by considering mixed circuitry and functional test. ■

Acknowledgments

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