Cache Where you Want! Reconciling Predictability and Coherent Caching

Ayoosh Bansal * Jayati Singh *, Yifan Hao*, Jen-Yang Wen*, Renato Mancuso† and Marco Caccamo‡
* University of Illinois at Urbana-Champaign, {ayooshb2, jayati, yifanh5, jwen11}@illinois.edu

† Boston University, rmancuso@bu.edu

† Technical University of Munich, mcaccamo@tum.de

Abstract—Real-time and cyber-physical systems need to interact with and respond to their physical environment in a predictable time. While multicore platforms provide incredible computational power and throughput, they also introduce new sources of unpredictability. Large fluctuations in latency to access data shared between multiple cores is an important contributor to the overall execution-time variability. In addition to the temporal unpredictability introduced by caching, parallel applications with data shared across multiple cores also pay additional latency overheads due to data coherence.

Analyzing the impact of data coherence on the worstcase execution-time of real-time applications is challenging because only scarce implementation details are revealed by manufacturers. This paper presents application level control for caching data at different levels of the cache hierarchy. The rationale is that by caching data only in shared cache it is possible to bypass private caches. The access latency to data present in caches becomes independent of its coherence state. We discuss the existing architectural support as well as the required hardware and OS modifications to support the proposed cacheability control. We evaluate the system on an architectural simulator. We show that the worst case execution time for a single memory write request is reduced by 52%. Benchmark evaluations show that proposed technique has a minimal impact on average performance.

Index Terms—hardware/software co-design, worst-case execution time, cache coherence, memory contention

I. Introduction

The last decade has witnessed a profound transformation in the way real-time systems are designed and integrated. At the root of this transformation are the ever growing data-heavy and time-sensitive real time applications. As scaling in processor speed has reached a limit, multi-core solutions [1] have proliferated. Embedded multi-core systems have introduced a plethora of new challenges for real-time applications. Not only this adds a new dimension to scheduling, but remarkably the fundamental principle that worst-case execution time (WCET) of applications can be estimated in isolation has been shaken.

In multi-core systems, major sources of unpredictability arise from inter-core contention over shared memory resources [2], [3]. Memory resource partitioning techniques present a suitable approach to mitigate undesired temporal interference between cores [4]–[6]. However, memory resource partitioning is particularly well suited only for systems where data exchange between cores is scarce or nonexistent [7]. Heavy data processing or data pipelining workloads, on the other hand, are often internally structured as multi-threaded applications, where coordination and fast data exchange between parallel execution flows on different cores is crucial. This exchange is based on shared memory.

Modern platforms generally feature a multi-level cache hierarchy, with the first cache level (L1) comprised of private per-core caches. When multiple threads access the same memory locations, it is crucial to ensure the coherence of different copies of the same memory block in multiple L1 caches. Dedicated hardware circuitry, namely the *coherence controller*, exists to maintain this invariant. Because maintaining coherence requires coordination among distributed L1 caches, it introduces overhead.

Cache coherence introduces two main obstacles for realtime systems. First, hardware coherence protocols are a preciously guarded intellectual property of hardware manufacturers. As such, scarce details are available to study the worst-case behavior for coherent data exchange. Second, coherence controllers are not designed to optimize for worst-case behavior. One approach to achieve predictable coherence consists of re-designing coherence protocols and controllers [8], [9]. Doing so, however, requires extensive modifications to existing processor design, with a possibly significant impact on performance.

In this paper, we propose a new approach to achieve predictable coherence. The key intuition is that if memory blocks accessed by multiple applications are cached only in shared levels —e.g., last-level cache— multiple copies of cache lines do not exist and coherence is trivially satisfied. Based on this, we define a new memory type that is non-cacheable in private (inner) cache levels, but cacheable in shared (outer) caches, namely Inner-Non-Cacheable, Outer-Cacheable (INC-OC). INC-OC memory type coexists with traditional memory types. Control over

which type of memory should be used for different areas of an application's working set is then provided to the developer and/or compiler. The key **contributions** of this work can be summarized as follows:

- A novel solution for predictable time access to coherent data without variability induced by coherence mechanisms.
- Prototype evaluation on an architectural simulator [10].

II. SOLUTION OVERVIEW

The main idea is to allow application developers or compilers to use their knowledge of the application to choose between the trade-offs of worst-case vs. average use access time with fine granularity. The choice of cacheability determines which level of caches can the data be cached in and which levels of cache data cannot be cached. Data locations for which strong worst-case latency guarantees are required would be selectively cached in shared levels. Data coherence is achieved as all accesses go to the same cached copy of such data. Coherence overheads and variability are avoided.

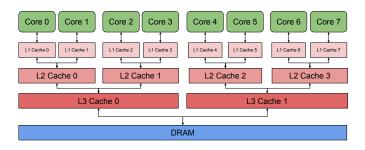


Fig. 1. Generalized multi-socketed multi-cluster processor.

Consider a hypothetical system as shown in Figure 1. For each core (C) consider a set M which consists of all memory blocks that are in its data pipeline. A memory block can be a specific cache (\$) or DRAM. For example:

$$M(C0) = \{L1\$0, L2\$0, L3\$0, DRAM\}$$
 (1)

$$M(C1) = \{L1\$1, L2\$0, L3\$0, DRAM\}$$
 (2)

$$M(C7) = \{L1\$7, L2\$3, L3\$1, DRAM\}$$
 (3)

We propose that for any cache line which is assessed by only a subset of cores, the cache line be stored/cached on only the intersection of the sets M of these cores. Consider a cache line accessed by Core 0 and Core 1. This cache line can be stored in L2 Cache 0, L3 Cache 0 and DRAM but not in L1 Cache 0 or L1 Cache 1.

$$M(C0) \cap M(C1) = \{L2\$0, L3\$0, DRAM\}$$
 (4)

Consider another cache line that is accessed from Core 0 and Core 7. Based on our proposal this data block should not be cached at all and be stored in DRAM only.

$$M(C0) \cap M(C7) = \{DRAM\} \tag{5}$$

Under these restrictions, explicit mechanisms to maintain data coherence are not required. The restrictions should be expressed at application level, possibly as granular as a cache line, so hard real time applications can leverage predictable access time to shared data, while non real time applications running on the same system can enjoy the higher throughput of hardware managed cache coherence as they are not affected by the occasional spikes.

In reality, the closest existing support is cacheability control for two cache levels expressed at memory page granularity in ARVv8-A ISA, as further described in Section IV-B. The implementation and evaluation are based on an ARVv8-A processor simulator, Figure 3, and limited to two cacheability levels.

III. RELATED WORK

Multi-core systems have enabled multi-threaded realtime workloads. Real-time applications with parallel, precedence-constrained processing tasks are often represented as periodic (or sporadic) DAG tasks [11]. Scheduling of DAG tasks has received considerable attention [11]– [13]. Alongside, application-level frameworks to structure real-time applications to follow the DAG model have been proposed and evaluated [14].

In practice, however, the implementation and analysis of DAG real-time tasks is challenging because analytically upper-bounding the worst-case execution time (WCET) of a processing node is hard. As multiple DAG nodes are executed in parallel, they interfere with each other on the shared memory hierarchy. Well known sources of interference arise from space contention in the shared cache levels [15], [16]; contention for allocation of miss status holding registers (MSHR) [17]; bandwidth contention when accessing the DRAM memory controller [5], [18]; and bank-level contention due to request re-ordering in the DRAM storage [6]. Our work focuses on tightening and simplifying the analysis of the WCET bound by making shared data accesses immune from unpredictable temporal effects of cache coherence controllers.

Cache contention among parallel tasks is a major cause of interference [16]. Mitigation approaches include selective caching [19], [20] and cache partitioning [4], [21]. Strict resource partitioning among cores is effective for independent tasks. But data sharing is necessary to implement processing pipelines, such as real-time tasks following the sporadic DAG model. In [22], the authors acknowledge that data-sharing between tasks is inevitable in mixed criticality, multi-core systems. In light of these considerations, previously proposed solutions have been adapted to allow sharing [23], [24].

The problems introduced by data sharing in real-time signal processing applications were studied in [25]–[27],

which demonstrate that the overhead from cache coherence protocols can severely diminish the gains aimed to be achieved through parallelism in multi-core systems. But more importantly, the overheads of cache coherence are unpredictable and can have large variance. In this work we focus exclusively on the unpredictability caused by cache coherence. Our solution is to allow shared data to bypass private levels and be cached directly in shared cache levels.

Previous works have addressed cache coherence in multiple ways. Giovani et al. propose a coherence aware scheduler [26] which staggers the execution of tasks that share data. The solution only works at task level granularity and may force idle times on processor. Predictable MSI [8] solves the coherence unpredictability by using a TDMA coherence bus and a modified MSI coherence protocol. The solution is invisible to software and provides predictability with reasonable overheads, but requires major changes to hardware coherence controllers that are difficult to implement and verify [28]–[30]. MC2 [22] improved upon [23], [24] by allowing data sharing across processors. The coherence effects are avoided by making the shared memory uncacheable or assigning tasks with shared memory accesses to the same core. The scheduling option is restrictive and like [26] may force processor idling. Extra accesses to uncached memory, i.e. main memory, are slow and may increase the WCET. On-Demand Coherent Cache [31] converts tasks accessing shared data to critical sections, hence disallowing concurrent execution of any tasks that share data. SWEL [32] focuses on high performance computing and message passing workloads. It proposes heuristic mechanisms in hardware to cache only private and read only data in L1 caches. There are no predictability assurances as the cache line placements decisions are based on observations at run time and optimize for throughput.

Our proposed solution does not impose any scheduling restrictions on the application and does not burden it to maintain coherence. In addition, it provides the developer freedom to choose which data to cache where, to optimize the average and worst-case performance trade-offs. This solution can be implemented without any changes to hardware coherence implementations and works with any coherence protocol. Minimal changes to the cache controller's logic are required. The overall effect is a complete avoidance of cache coherence overheads based on the developer's choices.

IV. Background

Let us first familiarize ourselves with the terms and concepts used in this work.

A. Cache Coherence

Cache Coherence [33] is a feature of modern multi-level, distributed CPU caches. In traditional cache architectures, it is fundamental that the contents of private levels of caches are kept *coherent* across multiple cores. A hardware cache coherence controller is present for this purpose. It

ensures that any valid copies of a cache line contain the same data. Cache coherence controllers work by assigning additional states to cache lines. Let us consider the example of MSI cache coherence protocol [34] as shown in Figure 2. In this protocol a cache line can be in one of the following three states:

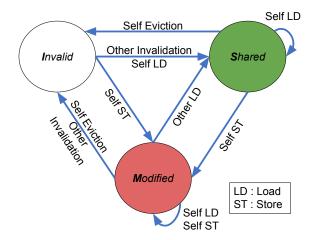


Fig. 2. MSI States and Transitions

- *Invalid*: Cache line is not allocated or contains invalid data. This is the initial state.
- Shared: Cache line contains valid data. A cache line in shared state can only be read from. Other caches may have the same cache line in Shared or Invalid state. Data cached in this line is the same as the corresponding location in main memory.
- Modified: Cache line contains valid data. A cache line in modified state can be used to read or write data. Other caches cannot have the same cache line in any state other than *Invalid*. Cache line contains dirty data, i.e., the current content of the cache line may be different from the corresponding location in main memory.

A cache line transitions between these state based on Self vs. Other load/store (LD/ST) events, as shown in Figure 2. Here, Self refers events generated by the the core under analysis. Evictions are cache line replacements. Other refers to messages to handle events by other cores.

B. Memory Types

A vast majority of modern multi-core embedded systems are implemented using ARM architectures. We focus on the latest major version ARMv8-A, extensively used in current platforms. This includes recent versions of Nvidia Tegra, Qualcomm Snapdragon and Samsung Exynos, among others [35]. There are 100+ mobile and embedded SoC compliant with ARMv8-A Instruction Set Architecture (ISA). In this architecture, a uniform physical memory address space describes traditional memory resources (e.g. DRAM space), as well as configuration space for on-chip and external devices. In order to adopt the correct caching policy for any given memory region, the

hardware allows specifying a set of meta-data, or *memory type*, for each memory page. The memory type specification informs the hardware of how load/store operations within a given memory range should be handled. Memory type attributes are encoded in each virtual memory page table descriptor. In setting up virtual memory, the OS is responsible for encoding the correct memory type in the page table entry (PTE) of any portion of memory being accessed. If virtual memory is disabled, no memory type can be associated with a memory range. This forces the hardware to be conservative and to treat any load/store operation as non-cacheable accesses.

ARMv8-A standard allows defining two main attributes in the memory type. First, cacheability: i.e., whether or not a memory location should be cached or not. There exist two cacheability attributes: inner cacheability and outer cacheability. If a memory region is marked as inner (resp., outer) cacheable, its content can be cached in the inner (resp., outer) cache levels. What constitutes inner vs. outer is implementation defined. Generally, however, private cache levels (e.g., L1) are inner caches. Conversely, shared cache levels are usually outer caches. Second, memory types encode a shareability attribute. Once again, this can be specified independently for inner and outer caches. If a memory region is defined as inner shareable, any of its cached lines are kept coherent by the hardware in the inner cache levels. The same goes for outer shareable memory.

In this work, we focus on a subset of possible memory types [36]. Specifically, Table I defines the memory attributes used throughout the paper. The default memory type is Normal Cacheable. This type of memory is cacheable (and shareable) at all levels of caches. The other frequently used memory type is Uncacheable. This memory type is typically used to describe I/O memory. We define a new memory type: Inner Non Cacheable, Outer Cacheable (INC-OC) and also address kernel support in Section VI-B. This type of memory is accessed by the processor cores only. It is cached in all shared (outer) cache levels but not cached in any caches private (inner) to any cores.

C. Architectural Support

One of our goals is minimal changes. So we first explore existing support for cacheability control in popular Instruction Set Architectures (ISA) and corresponding compliant processors. We find that while ARMv8-A ISA supports inner and outer cacheability control, hardware implementations simplify away this support. Conversely, X86 and MIPS ISA do not support high granularity cacheability control for different cache levels.

- X86: Intel 64 defines various levels of caching like Uncacheable, Write Combining, Write Through, Write Back [37]. Two methods are provided to specify the type of caching, namely, Memory Type Range Registers and Page Attribute Table. The defined caching types do not differentiate between the various levels of caches.
- ARM: ARMv8-A ISA allows managing the cacheability of Inner and Outer regions independently [38]. Most ARM processors however simplify their design by treating Inner Non-cacheable Outer Cacheable type as Non-Cacheable memory. This applies to Cortex-A53 [39], Cortex-A57 [40], Cortex-A72 [41]. Other ARM compliant processors implement similar simplifications. Nvidia Denver and Carmel architectures ignores the Outer Cacheability attribute [42], [43].
- MIPS: MIPS treats cacheability control in a simpler manner. MIPS32/64 ISA only defines Cached and Uncached memory types [44]. A lot of fields are left as implementation dependent though. One of the recent MIPS processors, M6200 supports only Cached and Uncached memory types [45].

V. APPROACH OVERVIEW AND MOTIVATION

The main idea behind our solution is to allow application developers or compilers to use their knowledge of the application to choose between the trade-offs of worst-case vs. average use access time. The choice of cacheability determines whether or not certain data will be cached in private L1 levels. Data locations for which strong worst-case latency guarantees are required can be selectively cached only in shared levels. Data coherence is achieved as only one cached copy of such data locations can exist. Coherence overheads and variability are avoided for any access to such locations.

A. Architectural Prerequisites

For cacheability control to provide predictable time access, two core requirements must be met. First, a shared cache level must exist between the entities that share the worst case latency sensitive data. Consider Multi-Socket Multi-Core (MSMC) architectures. The chips in such sockets do not have a shared cache level. Their first common memory level is the main memory and hence our solution would translate to using uncacheable memory type. The second requirement is that for the given shared cache level, a method must exist to limit the cacheability to that level. Consider a multilevel cache architecture like Nvidia Carmel SoC. Cluster of 2 cores share a L2 cache level. 2 such clusters share an L3 cache. In such

TABLE I Memory Types

Name	Cacheability	Description
Normal Cacheable	Inner Cacheable, Outer Cacheable	Data caching allowed in all caches
Uncacheable	Inner Non-Cacheable, Outer Non-Cacheable	Data caching not allowed
INC-OC	Inner Non-Cacheable, Outer Cacheable	Data caching allowed in Shared caches only

cases, either the data sharing needs to be limited or enough memory types must exist to limit cacheability to each cache level. This level of fine grained control is not supported by current ARMv8-A ISA. For the remainder of this paper we consider a system as shown in Figure 3.

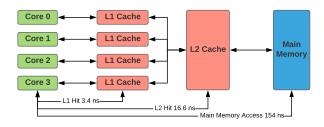


Fig. 3. System model

B. Coherence Cost

Cache coherence introduces a new dimension to cache function. A cache hit can no longer be defined as simply having the data in the cache. Correct state and privilege are now also a requirement for a hit. The implementation details of cache coherence controllers are proprietary and hence it is generally difficult to estimate or measure the exact latency of every operation. Cache access operations can be one of:

- *Hit:* The data block is present in the cache and in a state that allows the desired operation. For example *Shared* for Load and *Modified* for Store.
- Miss: The data block is not present in the cache and needs to be retrieved from a lower cache level or main memory.
- Coherence Miss: The data block is present in the local cache or a remote cache at the same level. But the state of the block does not allow the desired operation. For example Store on a cache line in Shared state.

Another example is shown in Figure 4. Consider a 2 core processor with 2 cache levels. In this example, the core attached to L1 Cache1 initiates a store operation. This cache does not have the data block for the Store, but L1 Cache2 has the data block in *Modified* state. Cache2 has to invalidate its cache line and write back the dirty data to the shared L2 cache. The L2 cache can then send the data to L1 Cache1 which can finally execute the Store. L1 Cache1 now contains the cache line in Modified state. These series of events can lead to long latency in executing a single memory access. We refer to this situation as a *Dirty Miss* in this paper.

Figure 5 illustrates the cost of a *dirty miss*. Using an instrumented simulation, see Section VI-F1, we can set up custom scenarios. Simulation logs show when some events of interest complete. The time reported is simulation ticks which are a direct equivalent to cycles in a hardware system.

At time 0, a core initiates a single write request. The target cache line is in Modified state in another L1 cache. It takes 4 cycles for the L1 cache to get the request from the processor, determine the current state of the cache line and take actions accordingly. It takes a further 124 cycles or total 128 cycles for L2 cache to receive the first request and take actions accordingly. The next 601 cycles are spent in completing the coherence steps, as shown in Figure 4, and delivering data to the requesting L1 cache. It takes $4.7 \times$ cycles to resolve a dirty miss compared to L2 communication delay.

C. Coherence Complexity

Hardware cache coherence simplifies the development of general purpose multi-threaded software. Many applications are served well by the transparent handling of data coherence by the hardware. But for real-time applications this creates another uncontrolled source of unpredictability in their worst-case execution time. Cache coherence protocols in SoCs are defined by vendors with only the main stable states [43], [46]. There are a plethora of transient states in coherence state machines and many low level details that impact the overall coherence state machine operation [47]. This makes any analysis on existing cache coherence controllers difficult. Our approach of caching shared data in shared cache only, completely removes the cache coherence controller from the shared data access process. Hence the effect of coherence on worst case analysis and during certification of the system is trivially handled.

D. Private vs Shared Access

In this section we discuss the difference between accessing Shared vs Private data on two real platforms.

- Cortex-A53 [48]: Quad-core ARMv8-A processor [49].
- Xeon E5-2658 [50]: 14 core, 2 hyperthread per core, Intel processor on a desktop workstation.

We developed synthetic benchmarks to study the effect of cache coherence on real platforms. We measure the average latency to complete a Load or Store to data already present in L1 caches. All cores do the same operations simultaneously. The resulting average latency is a combined effect of single access latency, parallelization, bandwidth contention and opportunistic hardware optimization like prefetchers. Consider Figure 6. For the first cluster of bars, Load, every core reads sequential memory. For the second cluster, Store, every core writes to sequential memory and then reads the value back. The read back ensures that the captured latency includes Store to cache and not to an internal write buffer only. In *Private* case (left bars) every core accesses private data sets, in Shared (right bars) they all share one data set. The Shared case therefore shows the additional overhead of cache coherence protocols.

The Lock latency is the average latency to acquire and release a spinlock. In case of *Private* every core accesses a different spinlock. All lock operations complete within the

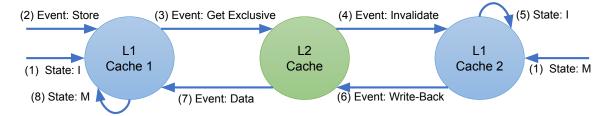


Fig. 4. Transitions of a Dirty Miss

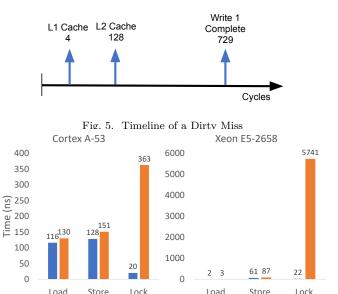


Fig. 6. Private vs Shared Access Latency

Private

Shared

Private

Shared

Private L1 cache and there is no waiting on the lock and no one else is trying to acquire it. In *Shared* every core acquires and releases the same lock. The critical section is empty. Spinlock implementation is below and uses gcc built-in atomics [51]. The acquire and release sequence is hence less than 10 assembly instructions. In case of shared lock, hence, most of the time is spent on access contention.

```
lock: while(__sync_lock_test_and_set (&lck, 1))
{};
unlock: sync lock release (&lck);
```

While exact overheads of cache coherence are hard to measure on real platforms, it is evident that the latency to access data is dependent on whether it is being shared across different cores. The Load/Store measurements represent latency differences near full memory bandwidth and hence the effect of coherence itself is diminished. Locks on the other hand require that the underlying micro-ops/instructions complete in order. Locks are hence affected more by the overheads of maintaining coherence.

VI. IMPLEMENTATION

As noted in Section IV-C, existing COTS ARMv8-A platforms cannot use INC-OC memory type hence the

evaluation is limited to simulations. We implement the controlled cacheability on the gem5 architectural simulator [52] to realize a system as shown in Figures 3 and 7. The simulation system is configured to be representative of a Cortex-A53 [48]. The memory hierarchy is comprised of 32 KB L1 cache per core, 2 MB L2 cache and 4 GB DRAM. This is in line with typical Cortex-A53 based SoCs [49]. We chose configurable cache parameters to mirror Cortex-A53 though some differences would surely exist. For both the Cortex-A53 [48], [49] and the simulated system, memory access latency are as shown in Figure 3.

Further in this section we describe our implementation and how it would function on a real system. Our modifications add the support for the INC-OC memory type in gem5 simulator. The design is presented top to bottom, starting from application layer and all the way to cache microarchitecture. This design is close to what the authors, to the best of their knowledge, believe a hardware implementations should be like. gem5's cache framework Ruby does not support uncacheable memory type. Access latency to uncacheable memory is much higher than any cache. Hence any comparison with uncacheable memory is not interesting.

A. Application

Our primary aim is to provide applications the mechanism to decide between the tradeoffs of worst case vs average access time. ARM ISA allows expressing cacheability of memory at a per-page granularity. We modified mmap [53] memory allocation API to accept additional flags that are used by the kernel to determine the cacheability of allocated pages. As part of the evaluation of this work we modified some standard benchmarks to use this cacheability control. An example INC-OC allocation is shown here:

B. Kernel

For an OS to provide the cacheability control to the userspace application, two components are required: first, APIs to allow applications to choose the memory type, as shown above. Second, page table entries need to be set up with the right value as defined by the ISA to use the INC-OC memory type. We implemented both

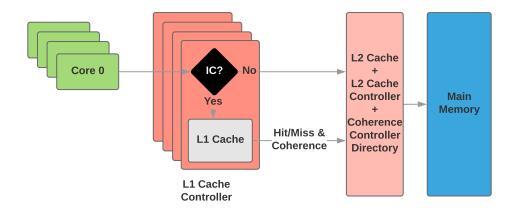


Fig. 7. Memory Access Flow

these components for Linux ARM64. Our mmap syscall implementation allows for additional flags to be passed by an application. These flags are then used to determine the memory type to set the page tables. We created a new memory type in the kernel for INC-OC. Linux kernel defines 6 memory types¹. Two more memory types can be defined. So we were able to add the new memory type with minimal changes. The kernel changes can run on any ARMv8-A compliant platform and set the memory type bits for INC-OC as defined in the ARMv8-A ISA, but the eventual handling depends on the underlying hardware. In accordance to Cortex-A53 documentation [39] when such cacheability bits for INC-OC type are set by the Linux kernel, Cortex-A53 treats these memory pages as uncacheable. This is a simplification in processor implementation as described in Section IV-C. In our simulation system the same cacheability bits allow the underlying caches to handle cacheability of memory requests in accordance to the full specification of the ARMv8-A ISA. The kernel changes in form of a patch are available [10].

C. Processor

We use the existing Timing Simple Processor in gem5 that runs ARMv8-A ISA. We modify the Translation lookaside buffer (TLB) to cache the additional page table attributes and add them to every memory access sent to the memory subsystem. Similar changes will be required in the real processors to propagate the cacheability information from page tables to memory requests.

D. L1 Cache Controller

We modified the L1 cache controller to check if the request is for Inner Cacheable (IC) memory. The further handling is dependent on this check.

1) Normal Memory: Our L1 cache controller follows the MSI protocol. The L1 cache controllers do not communicate with each other. Any L1 cache only communicates with its processor core and the shared L2 Cache. Hence

L1 caches send requests to the L2 cache controller which completes all relevant actions before sending a response back to the L1 cache.

2) INC-OC Memory: If a memory request is marked as Inner Non-Cacheable the request is directly forwarded to the L2 cache as shown in Figure 7. Similarly, any responses to these requests from the L2 cache are forwarded to the processor. Since INC-OC data blocks are never cached in the private L1 caches, multiple copies of the same data can not exist, therefore, no extra logic is required to maintain coherence. The cost of this change is that all requests to INC-OC cache lines go directly to the L2 cache, including what could have been L1 cache hits.

E. L2 Cache Controller

The L2 cache is the only shared cache in our system as depicted in Figure 3. It is strictly inclusive i.e. it contains any cache line that is cached in an L1 cache. The DRAM subsystem that connects to this L2 cache was not modified and emulates a constant access time main memory.

- 1) Normal Memory: The L2 cache controller serves as the coherence directory for this machine, in addition to the shared cache. It maintains information about all cached lines and manages all requests from L1 caches. It is able to ascertain the steps involved in fulfilling such requests, like sending out invalidations or collecting acknowledgements for the invalidations.
- 2) INC-OC Memory: L2 Cache Controller was modified to support the INC-OC memory type. INC-OC cache lines share the same memory space as normal memory type. But once allocated as an INC-OC cache line, the coherence state machine marks them separately and treats them like single-core system cache lines. A cache line can convert between INC-OC or normal types but needs to be invalidated in between. A cache line cannot be simultaneously treated as INC-OC and Normal Cacheable memory. Due to the direct forwarding of all INC-OC requests to L2 caches, there is increased contention on the L2 cache bandwidth. Since the L2 cache is already inclusive of L1 caches there is

 $^{^{1}}$ arch/arm64/include/asm/memory.h

no increase in contention for L2 cache space. This change converts the coherence problem to a cache bandwidth contention problem which is well studied in literature [5], [18].

A major functional change in the L2 cache is the requirement to handle Load/Store exclusive (LDXR/STXR) instruction pair. To this end we maintain a markup of LDXR instructions on cache lines and only accept the STXR if the cache line has not been modified since the corresponding LDXR from the same core. This is a new requirement for INC-OC memory type, as in case of Normal memory type, all LDXR/STXR instructions are handled in the private cache itself.

F. Simulation Modes

We use the simulation system in two modes. Trace mode uses the memory subsystem in isolation to replay data access traces. Full system mode emulates a complete hardware platform.

- 1) Trace Mode Simulation: Trace mode for gem5 was developed by Hassan et al. [8]. It allows using the gem5 memory subsystem alone. The processor subsystem is replaced by a synthetic request injection. Based on an input trace file a dummy processor generates memory requests. The trace file contains memory address, operation (read/write) and time stamp for initial request injection. We manually construct traces to create custom scenarios. These scenarios do occur in real systems but are difficult to reproduce and observe.
- 2) Full System Simulation: In this mode the simulator emulates a real platform. The cache and memory subsystems are the same as previous mode. But there is a full fledged ARMv8-A compatible processor subsystem. This mode supports running a Linux kernel. Benchmark applications are oblivious of the underlying simulator and run as if on a real platform. As noted in Section VI and Figure 3, we have selected simulation parameters so that the simulated system's cache access latency are close to Cortex-A53 [48], [49]. This full system simulation brings together all aspects of our implementation as described in Sections VI-A-VI-E. The simulator with all the changes is available [10].

G. Discussion and Limitations

The design is close to what the authors, to the best of their knowledge, believe a hardware implementations should be like. It seems impractical to have dedicated ports from the processor to each level of the memory system. So the processor should only interact with the respective L1 caches. The L1 cache, based on parameters in the memory request, can then determine if it should allocate lines for such a request. This design choice does slow down access to INC-OC lines. Additional cycles are spent in competing with any pending L1 cacheable memory requests and going though the L1 cache controller logic. A direct port would have bypassed all this but we believe that the

silicon and metal costs will be prohibitive. The cascading communication path also makes our solution scalable to multilevel caches as long as there is enough ISA support to express the memory types that define cacheability at each level.

VII. EVALUATION

The evaluation is based on custom scenarios, microbenchmarks and benchmarks from the SPLASH2 [54] suite.

A. Trace Mode Simulation

As described before in Section VI-F1, *Trace* mode synthetically injects accesses to the memory subsystem of gem5, based on input trace files. The traces can be manually written to create specific scenarios.

Figure 8 shows an extended scenario similar to Section V-B. A write request to the same address is generated by each core, simultaneously. Write 1 complete is the same *dirty miss* scenario as Figure 5. We additionally note the time when all 4 write requests finish. Similar experiments for read requests were conducted but are not shown. **Shared** state data, that can safely co-exist on multiple private caches, is served better by normal memory than INC-OC.

The trace files and gem5 coherence log that provides the timing information is available [10].

Observation: The total time to process the *dirty miss* is 52% shorter for INC-OC memory. For all 4 write requests the total time was reduced by 74%.

Limitation: A dirty miss is a fairly common occurrence for shared data accesses but multiple parallel write requests for the same data does not happen in well written programs. From a coherence perspective, a similar situation can occur when atomic accesses, like spinlocks, request exclusive access to cache lines in course of executing LDXR instruction.

B. Full System Simulation

In full system simulation, programs are run inside a full fledged Linux kernel running over the simulation platform. This presents a close equivalence to a real machine. To reduce the variability in program execution time caused by CPU and DRAM, we use the timing simple models for both included in gem5. These models provide constant time DRAM accesses and simplified instruction pipelines, while still maintaining detailed timing of events. Also, between *Normal* and *INC-OC* only an *mmap* argument flag² is changed before compilation. The programs are otherwise identical. All this helps limit the evaluation to purely a comparison between *Normal* and *INC-OC* memory types.

 $^{^2}$ As shown in Section VI-A.

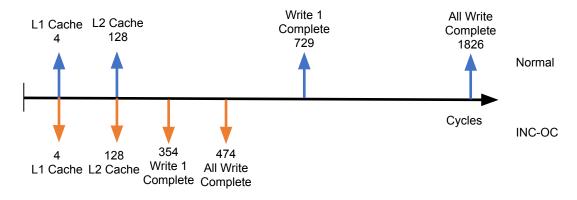


Fig. 8. Worst-Case Write-Request Contention

1) Synthetic Benchmarks: In Figure 9 we show the results of running the microbenchmarks discussed in Section V. As before, Load, Store and Lock refers to the average latency of completing these operations. For Normal Cacheable memory we measure the latency on Private memory blocks per core and also memory blocks shared among all cores. Next, we repeat the shared memory experiments with INC-OC memory type.

Observation: Latency to acquire locks reduces significantly by the use of INC-OC memory type. Load and Store time is increased for INC-OC.

Discussion: The forced ordering of locking primitives avoids other effects, but since data coherence among contending cores depends on coherence hardware, the effect of coherence dominates. In case of loads and stores the combined effect of bandwidth limitations, additional latency and parallel handling of coherence of individual lines makes INC-OC average access latency higher.

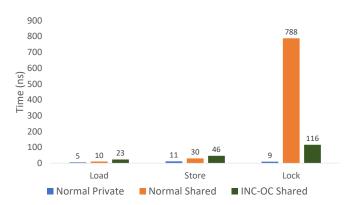


Fig. 9. Full system simulation synthetic benchmarks

2) Benchmark Evaluation: In Figure 10 we compare the worst case run time for SPLASH2 [54] benchmarks on the full system simulation. For Normal all memory used is normal cacheable. Blind INC-OC blindly allocates every variable, that is visible across threads created by the benchmark, with INC-OC memory type. For Program Aware INC-OC we identify program variables and memory

locations that can be safely accessed as Normal memory. Our optimization treats as normal memory those variables that (1) are accessed by a single thread, that (2) remain constant in parallel parts of the benchmark, or that (3) are within memory ranges that are divided among threads by offset ranges. Results are normalized to the *Normal* case. The reported measurements represent the worst-case runtime observed in 100 runs with warmed caches. All benchmarks use spinlocks for synchronization which are allocated with an INC-OC memory type, except in the *Normal* case.

Observation: Blind INC-OC execution times are up to 5.7× higher than Normal, while Program Aware INC-OC's performance is near identical as Normal.

Discussion: The blind approach is overly conservative in INC-OC allocation, while Program Aware INC-OC precisely targets truly shared memory requests. But this is a manual process of understanding the program and making choices about cacheability. We expect this to become a part of the regular practice for the development of multi-threaded real-time applications. Nevertheless, this is the true cost of the proposed solution. The near identical performance is attributable to a small percentage of INC-OC accesses in Program Aware INC-OC, max 0.08% across benchmarks. This highlights the need for a precise and selective mechanism for handling coherence overheads in multi-threaded and parallel applications³.

Due to limitations of space a variability analysis is not shown, gem5 simulator aims at deterministic repeatability of execution. Consequently, even in full system mode the observed standard deviation in execution time of benchmarks is quite small, roughly 1% of execution time.

VIII. SECURITY IMPLICATIONS

Since we are expanding the user space software's control of low level hardware, security implications need to be carefully considered.

³See Section IX-C for further discussion on this.

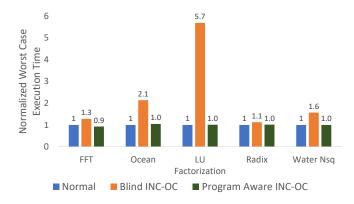


Fig. 10. Benchmark evaluation for Full System simulation.

A. Locks

RISC and CISC architectures handle atomic operations differently at architectural level. This difference has important implications for the use of INC-OC memory type.

- 1) CISC: Atomic operations in X86, like XCHG, disallow any access to the targeted memory area till all involved micro-operations are complete. This is achieved by asserting a LOCK [37] signal to block any access to the relevant memory buses. If the targeted memory area is in a private cache the memory location is modified internally and cache coherency mechanism ensures that the operation is carried out atomically. For atomic operations to INC-OC and Uncacheable memory the LOCK signal will have to be asserted to shared memory buses. This opens up the possibility of a core starving all other cores of memory bandwidth by continuously executing atomic operations on INC-OC or Uncacheable memory [55].
- 2) RISC: RISC ISA like ARM and MIPS, use Load-Linked Store-Conditional semantics to implement lock free atomic operations. Since system resources are never locked, the vulnerability, as discussed above, does not apply.

B. Cache Conflicts

As a result of the introduction of INC-OC memory type userspace applications can now directly allocate cache lines in shared cache levels. Such allocations can be used to force cache lines owned by other applications to evict from the cache. But all related attack are already possible with *Normal* cacheable memory via directed private cache misses [56]. The access patterns and size required to achieve the same effect via normal cacheable memory depends on the inclusivity and allocation policy of the caches.

IX. DISCUSSION

In this section we discuss the strengths and limitations of cacheability control and INC-OC memory type.

A. Hardware/Software changes

Our solution requires changes to existing hardware. But the changes are minimal as we leverage existing ISA features. In comparison, competing techniques modify the cache coherence controller implementation and behavior. Cache coherence protocols are difficult to verify [57] and certify for real-time behaviour. Any solution that changes the coherence protocol states, transient states or timing etc is hence difficult to adopt. The development and verification costs can be prohibitive. INC-OC memory does not modify the coherence protocols or controllers. The memory type itself classifies the memory requests for INC-OC type to be handled outside of the standard coherence state machine. So while cache controllers need to be modified to handle the new memory type, the coherence controller itself remains unchanged.

The kernel modifications required to support the INC-OC memory types are also small. Since Linux kernel already has a notion of *memory types* the introduction of INC-OC type required less than 10 new code lines. Allowing *mmap* system call to set the memory type in a simple implementation required less than 100 new code lines.

B. WCET Analysis

Due to the complex nature of the coherence protocols, a WCET analysis of coherence controllers, even for those designed for real-time systems, can be an onerous task. INC-OC memory type eliminates the need for such an analysis.

C. Precise Impact

A problem with existing solutions for predictable cache coherence is that they impact all data accesses, independently from the data being private or shared. On the other hand, INC-OC memory type is used explicitly and precisely. Default memory type for memory allocation API is normal memory. As discussed before, the mechanism of this selection can be as simple as passing an additional flag during memory allocation. The solution can be selectively applied by the developer who can judiciously decide between the worst case and average memory access times on a case by case basis. For this reason, significant performance benefits can be observed via OC-INC on the same benchmarks compared to the alternative solution proposed in [8], namely Predictable MSI (PMSI). Specifically, although [8] uses a less realistic simulation setup, applications using PMSI incur a 1.45× slowdown compared to the baseline. Conversely, our evaluations indicate that INC-OC has near identical performance to the Normal baseline. As previously mentioned, this precision comes at the cost of manual application code refinement. We argue however that such refinement could largely be automated at compile-time. That is, as long as identification of shared data can be automatically performed, which has been successfully attempted in the past [20].

D. Applicability

Detailed cache coherence parameters of a system may limit if INC-OC memory type is useful.

- 1) Coherence Protocol: A prerequisite for INC-OC memory type being useful is that the L2 cache access time is less than the worst case access time for normal cacheable memory. While in our observation that is true for some platforms, it is possible to build a processor where this is not true. A larger number of cores trying to modify the same data at the same time will increase the worst case if the data is cacheable in private caches. On the other hand, coherence protocols like MOESI that allow dirty data to be communicated directly among private caches without requiring write-back would decrease the worst case latency for private caches. The exact applicability of INC-OC memory type depends on the full characteristics of the cache and coherence controllers that are usually not publicly documented by vendors. Vendors tend to include only the stable coherence state information in their product documentation [37].
- 2) Bus Structure: We implement a directory based coherence, i.e. where the directory, L2 cache in this case, maintains the list of all L1 caches that are using a particular cache line. The directory sends directed message to all L1 caches when required. A snooping coherence bus may reduce the worst case access time for normal cacheable memory, albeit it is known that snooping approaches do not scale well with large number of cores.
- 3) Non-Uniform Cache Architectures: Non-Uniform Cache Architectures (NUCA) [58] use a physically distributed last level cache to reduce wire delays for cache access. From a given processor core, different banks of the NUCA cache have different access latency. For worst case analysis with INC-OC memory type the largest latency bank, accessible by a core, should be considered.

E. Other Sources of Variability

Use of INC-OC memory type eliminates the inter-core interference due to cache coherence only. Both shared and private caches are still affected by cache misses and bandwidth contention. caused by different cores. One core's cache line can still be evicted by other core's accesses. Additionally, the multiple cores still share the memory bandwidth of shared caches and all the way to the memory. This is another source of contention that the use of INC-OC memory does not remove. In fact due to direct forwarding of requests to shared caches, the use of INC-OC memory increases the shared cache bandwidth usage. These sources of contention have existed since the use of memory caches. They are not specific to multicore systems. Many existing works have addressed these problems as discussed in Section III.

F. Application Models

The impact of INC-OC memory type is heavily dependent on application characteristics. On the one end of

the spectrum are Non-Blocking algorithms [59] or Worker Queue models that severely limit data sharing. For these applications INC-OC's contribution will be small. On the other end, Data Streaming models or chains of producers and consumers involve multiple threads continuously sharing and modifying large amounts of data. In this case, OC-INC would lead to significant improvements in predictability. Due to limitations of platform and benchmarks we have not been able to evaluate these application models yet.

X. CONCLUSION

In this paper we present the INC-OC memory type and a series of mechanisms to select memory types from user-space. Memory types can be defined at a page granularity. A developer can selectively and judiciously decide which memory type to use based on application requirements. INC-OC memory type bypasses private caches, hence avoiding coherence overheads and reducing worst-case memory access latency. Overall, judicious use of INC-OC memory type can help applications reduce their worst-case execution-time by reducing the unpredictability arising from black-box hardware coherence management.

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