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# Composing Graph Theory and Deep Neural Networks to Evaluate SEU Type Soft Error Effects

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Abstract-Rapidly shrinking technology node and voltage scaling increase the susceptibility of Soft Errors in digital circuits. Soft Errors are radiation-induced effects while the radiation particles such as Alpha, Neutrons or Heavy Ions, interact with sensitive regions of microelectronic devices/circuits. The particle hit could be a glancing blow or a penetrating strike. A well apprehended and characterized way of analyzing soft error effects is the fault-injection campaign, but that typically acknowledged as time and resource-consuming simulation strategy. As an alternative to traditional fault injection-based methodologies and to explore the applicability of modern graph based neural network algorithms in the field of reliability modeling, this paper proposes a systematic framework that explores gate-level abstractions to extract and exploit relevant feature representations at lowdimensional vector space. The framework allows the extensive prediction analysis of SEU type soft error effects in a given circuit. A scalable and inductive type representation learning algorithm on graphs called GraphSAGE has been utilized for efficiently extracting structural features of the gate-level netlist, providing a valuable database to exercise a downstream machine learning or deep learning algorithm aiming at predicting fault propagation metrics. Functional Failure Rate (FFR): the predicted fault propagating metric of SEU type fault within the gate-level circuit abstraction of the 10-Gigabit Ethernet MAC (IEEE 802.3) standard circuit.

*Index Terms*—GraphSAGE (Graph Based Neural Network), Gate-level Circuit Abstraction, Deep Neural Networks, Functional Failure Rate (FFR), Single Event Upset (SEU), Single Event Transient (SET) and Soft Errors.

#### I. INTRODUCTION

System engineering focuses on the integration of new smallscale technologies, which constantly advancing the state of the art. Current quality requirements from industrial standards and end-user requirements for high dependability applications expedite reliability modeling and assessment into an increasingly significant endeavor. The aggressive technology node scaling increased the vulnerability of radiation-induced soft errors. The issues due to radiation-based effects, particularly, Single Event Effects (SEEs) seriously impact the circuit's reliability and, the effects of impacts on the functional behavior of the circuit are challenging to evaluate. A valuable approach to tackle the challenge is the fault injection (or) simulation principle that provides precise and accurate information about circuit behaviour under stress and allowing the calculation of actual circuit-level reliability metrics.

#### A. Motivation

As mentioned above, the exhaustive fault injection method is the ultimate reliability assessment method in terms of accuracy, but it is very inconvenient in terms of time and EDA licenses; which, makes this approach infeasible on medium and large scale circuits. Therefore, a new test methodology has proposed here. The fundamental idea is to provide an alternate solution to avoid unreasonable test costs by maintaining good statistical significance in results of proposed scope. Research proposals based on Graph Theory and Deep Learning (DL) techniques are more advanced and greatly favoured by researchers to learn statistical dependencies of system-function on related parameters. This motivation develops into a method of applying GraphSAGE algorithm and trying to find the best way to develop relevant feature databases from the gate-level netlist and subsequently applying to a downstream deep neural network for the functional failure reliability metric assessment.

### B. Related Works

Application of Artificial Intelligence (AI) and Deep Learning approaches to extract feature database of information in the graph network domain, were benefited in different fields. In recent years, different supervised and unsupervised DL approaches have proposed for graphical node embedding. The process of leveraging a node's features into a vector form is called the node embedding. Node2vec [1], Graph Convolutional Networks (GCN) [2] and GraphSAGE [3] have recently gained much attention from researchers for node embedding process. The application of graph-based neural network algorithms (GCN and node2vec) for circuit's reliability modeling, have proposed in papers [4] and [5] respectively. There is sufficient literature for machine learning (ML) applications in system reliability engineering. But, most of the classical machine learning algorithms rely on black-box modeling (not transparent in modeling the metrics). Here, we aiming a framework which could learn the structural information of circuit's gate-level abstraction in an unsupervised way (without the true target-probability information) based on graphSAGE algorithm and applied these node embedding vectors to a

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downstream deep learning algorithm. A proper mathematical fault propagating metric given in eq.1 has modeled in this scenario. The analyzed results providing the case of much better numerical superiority in fault propagational metric predictions and interestingly reducing the time complexity.

## C. Organization of the Paper

The organization of the paper includes a brief introduction followed by sections II, III, IV, and V. Section II covers not only the theoretical background of the physical phenomena and mathematical functions to be modeled but also a brief description of graph theory and graph-based neural networks. The workflow of the framework has provided in section III. Section IV illustrates the results of the fault propagating metric predictions and, finally, a conclusion to the holistic approaches provided in section V.

## II. BACKGROUND & METHODOLOGY

## A. Reliability Modeling at Gate-Level

Single Event Upset (SEU) and Single Event Transient (SET) are the principal consequences of Single Event Effects (SEEs). Single Event Effects are challenging phenomena to analyse or predict when the silicon material of the circuit interacted with the radiation particles. The Single Event Upset widely used here as a prominent SEE representative, and use-case mainly implies an inversion of the stored value in a flip-flop, latch, or memory cell as the result of the radiation-induced charge. Single Event Transient represents a transient pulse of an arbitrary width due to the radioactive event and probably propagate through the combinatorial network and latched to the downstream sequential element. Among SEU and SET events, more probably SEUs will change the state sequences of the circuits and lead to a classified functional failure of the circuits. The functional failure rate due to SEU ( $FFR_{i,seu}$ ) at the given flip-flop (i), predicting through this framework. The fault propagational probability metric  $FFR_{i,seu}$  described as:

$$FFR_{i,seu} = FIT_{i,seu} \cdot \prod_{j \in T,L,F} DR_{ij}$$
(1)

$$FFR_{seu} = \sum_{i \in FF} FFR_{i,seu} \tag{2}$$

where,  $DR_{iT}$ ,  $DR_{iL}$ , and  $DR_{iF}$  represent the fault derating or masking factors such as Temporal Derating (TDR), Logical Derating (LDR) and Functional Derating (FDR) respectively. Similarly,  $FIT_{i,seu}$  denotes the rate of soft errors at the flipflop (*i*) in Failure-In-Time (FIT) unit. Readers could refer the papers [6]–[10] for the deep insights about the radiationinduced soft errors and their inevitable intrusive nature in the functioning of microelectronic devices in aggressive radiation environments.

1) **Temporal Derating:** Temporal (or time) derating represents the opportunity window of an event (SET or SEU) and it's probability to be latched to the downstream sequential elements like flip-flop, latch or memory.

2) *Logical Derating:* The porpagational probability of SEU or SET, within the combinational (or) sequential cell networks based on their logical boolean functions is quantified as logical masking probability (or) logical derating factor.

3) **Functional Derating**: The probability of the SEU/SET event affects the function of the circuit's actual application. Even though the possibility of changing the circuit's state sequences is significant due to SEU/SET, the effect may be benign or masked because of the application scope.

#### B. Graph Theory and Deep Learning Algorithms

1) Graph Theory: The graph theory is renowned for a mathematical representation of the data objects and their pairwise relationships in a graph model. In this context, the gate-level abstraction of the circuit has transformed into a graph network where vertices ( $\nu$ ) analogous to the flip-flops and gates, and the directed edges ( $\varepsilon$ ) represent the connection between them from input ports to output ports direction. The mathematical graph-function G of the transformed network given as:

$$G = (\nu, \varepsilon) \tag{3}$$

2) GraphSAGE: The GraphSAGE [3], a general inductive framework which leverages node's feature information to efficiently generate node embeddings for previously unseen data. GraphSAGE could be also explained as a graph based neural network with sampler and aggregator functions. Basically the GraphSAGE framework learn a function that generates the node embeddings by sampling and aggregating features from a node's local neighbourhood. Most common approaches like node2vec algorithm [1] require the availability of all the graph-nodes during the training phase of the node embedding process, and those approaches are inherently transductive and generally unable to postulate the learning function to unseen nodes. But an inductive node embedding meant to be an optimized generalization across the graph with same form of features. That is, we can leverage the node features of unseen graph part of a circuit by the embedding generator which trained once with a more generalized graph models of the circuit. This embedding part provides not only the local role of nodes in the graph but also their global positions. A sampler function defines the node's neighborhood definition through a uniform sampling of a fixed number of nodes instead of sampling the entire neighborhood space at each depthwise iteration. It will result in boosting the optimal usage of memory and reduce run-time complexity. Generally, usage of the word 'Depth' means a measure of a fixed distance from the source node for the neighborhood search. At each iteration of depth, an aggregator function has employed. From the stateof-art of the graphSAGE framework, numerous aggregator functions are available like Mean aggregator, Long short-term Memory (LSTM) aggregator, Pooling aggregator and Graph Convoultional Network (GCN) based aggregator. Here we implemented a Pooling aggregator with help of a python neural network libraries. The basic idea of the graphSAGE simplified and explained in the figure 2.

3) Deep Neural Network: Deep Neural Network (DNN) is an important step in machine learning applications. DNNs are trying to model data of complex distributions by combining different non-linear transformations. The elementary bricks of deep learning approaches are artificial neurons (perceptrons), which are inspired by biological neurons. An artificial neuron combines the input signals with adaptive weights and uses an activation function to deliver the output. In this work, a general fully connected DNN has implemented. The other main categories of deep learning methods are Convolutional Neural Network (CNN) and Recurrent Neural Networks (RNN).

## C. Fault Injection Simulation Paradigm

As above mentioned, the true database required to train and predict the fault propagating metric  $(FFR_{i,seu})$ , obtained through an exhaustive Fault Injection (FI) campaign. In an exhaustive FI campaign, an SEU type fault injected independently at each flip-flop in each clock cycle of the time duration between transmission and reception of the input packets, as given in figure 1. If the injected fault (SEU) in a single clock cycle propagates through the circuit and subsequently causes the circuit's function to fail, it will account for the functional failure. Finally,  $FFR_{i,seu}$  was obtained by summing the functional failures per flip-flop over the total number of clock cycles required for the operation. In total, 1100 flip-flops from different blocks of the circuit (such as TX, RX, Wishbone Interface, Fault State-machine, and Sync\_clk), are tested and recorded functional failure rates ( $FFR_{i,seu}$ ) as true database.

Transmitting Packet Sequence	Transmission	Received Packet Sequence	
	SEU FI - Timeline	Packet Failure by SEU	
• XGE_MAC (Tx)		• XGE_MAC (Rx)	

Fig. 1. Transmission between XGE\_MAC Transmitter (TX) and it's Receiver (RX)

#### III. METHODOLOGY ILLUSTRATION

The whole approach has explained through successive workphases as follows:

## A. Phase I

The proposed work implements a method to map the gatelevel netlist as a Probabilistic Bayesian Graph (PGB) in the Graph Modeling Language (GML) format. To accomplish this goal, a Verilog Procedural Interface (VPI) based library function (a user-defined library) linked to a standard simulation tool (ModelSim/open-source tool). A gate-level netlist mapped to the graph model has represented in figure 2. Parallelly, the FI database simulated in this phase of the workflow.

#### B. Phase II

In the second phase of the approach, a feature matrix (X) corresponding to graph nodes extracted using the GrpahSAGE algorithm. As mentioned in section II-B2, GraphSAGE includes two principal steps. The premier step was the sampler algorithm. The sampler algorithm defines the neighbourhood space of a source node. In this scenario, we defined the parameter K = 2, which means that the sampler will sample up to the depth of 2 neighbourhood space. In the second step of the GraphSAGE algorithm, an aggregator has implemented at each depth  $(1 \le k \le K)$ . This could be seen in Phase II of figure 2, where blue and green line indicates the aggregators at depth k = 1 and k = 2 respectively. Here, a max-pooling aggregator was implemented. The mathematical abstraction of the pooling aggregator [3] formulated as:

$$AGGRE_k^{pool} = max(\{\sigma(W_{pool}h_{u_i}^k + b), \forall u_i \in N_k(v)\}), (4)$$

where equation 4 represents the aggregator function at depth k and it basically a neural network with parameters  $W_{pool}$  and b. Parameters optimized through unsupervised learning.  $N_k(v)$  represents k-neighbourhood of vertex v and  $h_{u_i}^k$  indicates the aggregated neighborhood vector and,  $\sigma$  is the activation function of the neural network. In this way, we could represent the whole GraphSAGE algorithm as a graph-based neural network. At the end of this phase, each node reformed into a corresponding vector and alternatively form a matrix representation (X) of the circuit as given in figure 2.

### C. Phase III

Phase III of figure 2 elucidates the DNN algorithm that exercised for prediction purposes. There are two parts included in phase III. The first part is the training part of DNN, and the second one is the testing part of DNN. In the training part, 40 % of the feature matrix and corresponding target probability metric from FI - database, are taken to postulate a hypothesis that best describes the target probability distribution ( $FFR_{i,seu}$ ) by supervised learning method. The optimized parameters (Weights and Bias) of the best fit of the target distribution should provide as model parameters. In the testing part, the proposed model applies to an unknown input vector and predicts the target probability metric. The DNN architecture consists of 5 dense layers, including the input and the output layers.

#### D. Phase IV

The final phase includes a comparison between the predicted and target probability metrics. The compared results plotted in figure 3, as well as the impacts of results provided in table I.

## IV. EXPERIMENTAL RESULTS

In figure 3, the functional failure rates of flip-flops to be predicted were shown in red color, and the corresponding predicted probabilities have shown in blue color. The case study has conducted with the gate-level circuit of the 10-Gigabit Ethernet MAC. The graphical comparison gives a

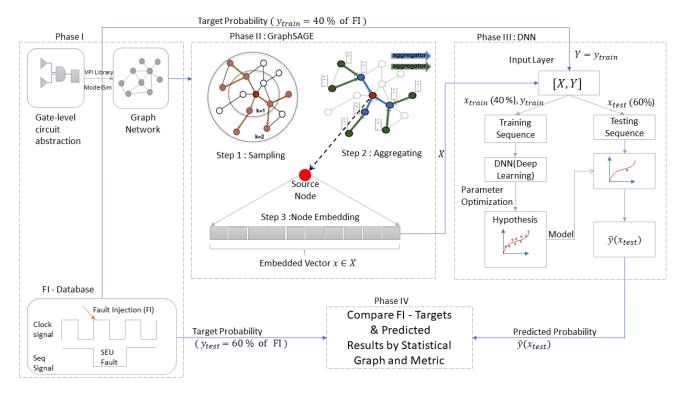


Fig. 2. A Systematic workflow diagram of the implemented scientific work

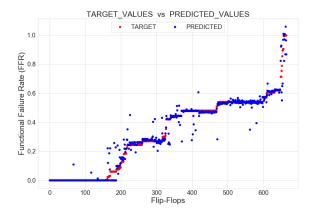


Fig. 3. Graph Comparison : Mean Absolute Error (MAE) = 0.0186 and coefficient of determination ( $R^2$  Metric) = 0.96 with a test size of 60%

visualization of how well the prediction replicates the observed database. In this case, the DNN prediction achieves the coefficient of determination  $(R^2)$  value of approximately 0.96, where the best model fit value of  $R^2$  metric is 1, and the worst value is 0. In statistics, the R-squared  $(R^2)$  value is the measure of goodness-of-fit of the proposed regression model and, the projected R-squared value (0.96) able to explain most of the variation in the response data. The entire work repeated and achieves a good prediction accuracy with other standard circuits (e.g., The USB 1.1 Function IP Core).

Table I outlines the impacts of accelerated predictions in

 TABLE I

 Impact of Prediction in Time and Tool Requirements

Model	Time	Tool	Model Fit $(R^2)$
Fault Injection Fault Injection	17 hours $\approx$ 5 days	7 Modelsim 1 Modelsim	Target Model Target Model
GraphSAGE + DNN (Test + Training)	< 10 minutes	1 Modelsim	0.96

terms of time and simulation tool requirements. Even-though GraphSAGE and DNN based ensemble algorithm provide a significant reduction in the required test resources without compromising the quality of modeling, the implemented algorithm depends on 40% of FI-database for training the downstream DNN as picturized in Phase III of fig.2. But, it is quite impressive to note that the test and training phase of the whole algorithm takes only less than 10 minutes.

## V. CONCLUSION

An accelerated testing methodology; that is scalable and very cost-effective in resource handling, has developed for medium and largescale circuits to predict Functional Failure Rate due to SEU type fault without dropping the significance of the statistical modeling.

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