ANALOG FEEDBACK-CONTROLLED MEMRISTOR PROGRAMMING CIRCUIT FOR ANALOG CONTENT ADDRESSABLE MEMORY

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Abstract

Recent breakthroughs in associative memories suggest that silicon memories are coming closer to human memories, especially for memristive Content Addressable Memories (CAMs) which are capable to read and write in analog values. However, the Program-Verify algorithm, the state-of-the-art memristor programming algorithm, requires frequent switching between verifying and programming memristor conductance, which brings many defects such as high dynamic power and long programming time. Here, we propose an analog feedback-controlled memristor programming circuit that makes use of a novel look-up table-based (LUT-based) programming algorithm. With the proposed algorithm, the programming and the verification of a memristor can be performed in a single-direction sequential process. Besides, we also integrated a single proposed programming circuit with eight analog CAM (aCAM) cells to build an aCAM array. We present SPICE simulations on TSMC 28nm process. The theoretical analysis shows that 1. A memristor conductance within an aCAM cell can be converted to an output boundary voltage in aCAM searching operations and 2. An output boundary voltage in aCAM searching operations can be converted to a programming data line voltage in aCAM programming operations. The simulation results of the proposed programming circuit prove the theoretical analysis and thus verify the feasibility to program memristors without frequently switching between verifying and programming the conductance. Besides, the simulation results of the proposed aCAM array show that the proposed programming circuit can be integrated into a large array architecture.

1 INTRODUCTION

Associative memories are inherent in human brains. Through association, the features of a new object can be matched with another object with similar features existing in our memory, and thus this new object can be simply remembered. In general, associative memories allow us to link uncorrelated information and hence are an essential feature of our intelligence[1].

Inspired by the biological and psychological concept of associative memories, different hardware approaches to such systems have been realized recently. W. A. Borders et al. proposed an analog spin-orbit torque device for ANN-based associative memory operation [2]. Pavlov associative memory has been implemented in circuits by different groups [3][4]. In recent years, memristive CAMs have been regarded as critical hardware in a wide range of associative memory applications: Li et al. designed the first aCAM which allows for searching in analog values[5]; G. Pedretti et al. used aCAM to introduce a new compute concept for tree-based learning techniques (e.g., decision trees and random forests)[6]; C. E. Graves et al. proposed an 86×12 memristor ternary CAM (TCAM) array for pattern matching[7]; Furthermore, differential CAM (dCAM) is also a viable option for associative memory architectures[8].

However, good memristor programming techniques are necessary for both aCAM and dCAM arrays to achieve an accurate and fast writing process without losing high memory density. Here we present a novel LUT-based programming algorithm for memristors that utilizes an analog feedback control mechanism to enable highly precise programming of a 10T2M aCAM cell[9]. We will also show the possibility to integrate the proposed programming circuit in a 10T2M aCAM array. With the proposed programming circuit, the aCAM array can properly set, reset, or read the conductance of the memristor within a single cell, and hence provide individual addressing. Besides, our results prove that the memristor programming algorithm is possible to replace the traditional Program-Verify algorithm for memristor programming in analog CAMs.

2 ANALOG FEEDBACK-CONTROLLED MEMRISTOR PROGRAMMING CIRCUIT

2.1 10T2M aCAM Cell

To enhance the programming capability of the 10T2M cell proposed in [6] and [9] using our proposed algorithm, we implemented a series of modifications as shown in Fig. 1, including:

- 1. The original aCAM design utilizes 1T1R structures with memristors connected to the OE electrode, and the CAM search is performed in the reset direction. Our design features an interchanged position between the memristor and transistor T1, with the Memristor AE now connected to the transistor. This configuration results in improved performance during set operations by eliminating the body effect, when applying a set voltage. [10]
- 2. The SL_{HI} originally shared by all PMOS and memris-



Figure 1: The 10T2M aCAM cell. This architecture consists of a low-bound (LB) cell (yellow block) and a high-bound (HB) cell (purple block) that define the boundaries of analog matching ranges. The memory cell can work in the search mode and in the program mode. In search mode, the memory performs a parallel operation to find if there is a matching word stored inside the array. In program mode, the memristor conductance is programmed to change the analog boundary of the matching word. To set the memristor, a positive voltage that exceeds the device's threshold voltage from OE to AE must be applied, while resetting requires a negative voltage.

tors in [6][9] are divided into 3 different signal lines $(SL_{AE}, INV, and FEB)$. This division will help the proposed memristor programming circuit to achieve the LUT-based programming algorithm and better control the analog feedback loop.

3. T11 and T12 are added in the LB cell and the HB cell respectively. These transistors add a "don't care" option in CAM search to each cell. They also ensure in during a search operation that the CAM cell is disconnected from the ML. These transistors are used to disconnect the CAM cell from the match line (ML) during a search operation, which prevents false matches caused by the internal capacitance charging at the beginning of each search pulse. In the program mode, when these transistors are off, any input at the data line (DL) won't affect the voltage at the match line (ML), which enables the use of the ML voltage in the programming circuit to write to an individual memristor.

2.2 The LUT-based memristor programming algorithm

Traditionally, the Program-Verify Algorithm is the state-ofthe-art algorithm used to program memristors[11][12]. However, while utilizing this algorithm, frequent switching between searching and programming is necessary, which leads to high programming accuracy but also results in high dynamic power consumption and lower programming speed. Besides, it requires stricter timing in peripheral circuits. Here, we present a LUTbased algorithm that can perform programming and verification simultaneously.

The demonstration of the proposed algorithm first starts with the analysis of the circuit in search mode shown in Fig. 2 (a). This



Figure 2: (a) Memristor comparator circuit in search mode with $V_{read} = 0.6 \text{ V}$. If a sweeping voltage is applied at the transistor gate, the output voltage V_{out} will decrease from V_{read} to 0. When the intermediate voltage between the transistor and memristor equals $V_{read}/2$, the corresponding VDL is marked as V_{DLS} . (b) A CMOS circuit with $V_{set} = 1.8$ V. The resistor in this circuit has a fixed conductance G_{mem} , which is the same as the memristor conductance in circuit(a). If a sweeping voltage is applied at the transistor gate, the output voltage V_{out} will increase from 0 to V_{set} . When $V_{out} = \alpha V_{set}$ (0 < α < 1), the corresponding V_{DL} is saved as V_{DLP} . This circuit is used to help understand the relationship between V_{DLS} , the boundary voltage in circuit (a) and V_{DLP} , the boundary voltage in circuit (b) (c) A memristive circuit with $V_{set} = 1.8$ V. If a DC voltage V_{DLP} is applied at the transistor gate, the output voltage V_{out} will decrease from V_{set} to 0 due to the increasing memristor conductance. When $V_{out} = \alpha V_{set}$ (0 < α < 1), the corresponding memristor conductance in circuit (c) should be the same as the conductance of the resistor in circuit (b).

circuit is called the "Memristor Comparator", which is present in the LB cell and the HB cell of the 10T2M aCAM cell. In circuit (a), the memristor is supplied with a low VDD (V_{read} = 0.6 V), which means the conductance of the memristor remains is close to constant. To simplify the calculations, the inverter in this circuit is assumed as ideal $(V_{out} = VDD - V_{in})$. First a linear voltage sweep is applied as transient simulation ranging from $0 < V_{DL} < V_{read} = 0.6 \text{ V}$ at the input V_{DL} of the aCAM cell. By increase of V_{DL} the output voltage V_{out} will drop from a high voltage to a lower voltage, since the intermediate voltage between transistor and memristor will rise. If the resistor and the transistor reach the same conductance, ideally V_{out} will drop from V_{read} to 0. During the simulation, the V_{DL} value which leads V_{out} drop or rise is the desired programming value since it represents the boundary voltage to which the input is compared. For schematic (a), this V_{DL} value is named V_{DLS} . If the transistor body effects are neglected, the drain current of the transistor at the V_{DLS} point can be calculated as below:

$$I_D = K' \frac{W}{L} \left[(V_{DLS} - V_T) \frac{V_{read}}{2} - \frac{1}{2} \left(\frac{V_{read}}{2} \right)^2 \right]$$

= $\frac{V_{read}}{2} G_{mem}$ (1)

analysis of the circuit in search mode shown in Fig. 2 (a). This $_{2}$ Then the relationship between V_{DLS} and the memristor conduc-

tance (G_{mem}) can be deducted from the above equations:

$$V_{DLS} = G_{mem} \frac{L}{W} \frac{1}{K'} + V_{read} + V_T$$
(2)

Equation. 2 demonstrates that the relation of the conductance of the memristor within the memristor comparator from Fig. 1 to the resulting boundary votlage V_{DLS} is linear. This circumstance can be utilized to simplify programming by allowing for the programming of a boundary voltage instead of a conductance within the memristor comparator. Conclusion (1)

Secondly, schematic (b) is compared with schematic (a) to analyze the relationship between V_{DLP} and V_{DLS} , since in programming mode, when sweeping the V_{DL} a certain specific boundary voltage V_{DLP} can be observed. Circuit (b) is a CMOS circuit that substitutes the memristor in (a) with a resistor of the same conductance to assume it as a constant device. $SL_{OE} = 1.8$ V and $SL_{+AE} = 0$ V, which means that a set voltage is applied and the transistor T1 in circuit (b) can reach saturation region. Now a simulation is performed by inserting a linear voltage sweep $(0 < V_{DL} < V_{set} = 1.8 \text{ V})$ at the transistor gate. With sweep of V_{DL} , the output voltage will rise from a low voltage to a high voltage. After this the V_{DL} is saved which makes the V_{out} rise to a certain value $V_{dth} = \alpha V_{set}$ (0 < α < 1), and name this V_{DL} value as the boundary voltage in programming mode V_{DLP} . Assuming that the inverter in this circuit is ideal $(V_{out} = VDD - V_{in})$ and neglecting the transistor body effects, then the boundary voltage in programming mode can be calculated as below:

$$(1-\alpha) V_{set} = \frac{1}{G_{mem}} \left[\frac{K'}{2} \frac{W}{L} \left(V_{DLP} - V_T \right)^2 \right]$$
(3)

Based on Equation. 1 and Equation. 3, the relationship between V_{DLS} and V_{DLP} can be written as:

$$V_{DLS} = \frac{(V_{DLP} - V_T)^2}{2(V_{set} - V_{dth})} + \frac{1}{4}V_{read} + V_T$$
(4)

The equation above demonstrates the relationship between V_{DLS} and V_{DLP} . This allows a specific boundary voltage to be programmed in set mode by retrieving the related boundary voltage in read mode, V_{DLS} , from a lookup table.(Conclusion (2))

The schematic from Fig. 1 (c) the 1T1R is again realized with a memristor. In this case, the input voltage V_{DL} is not swept; instead, a constant DC voltage, V_{DLP} , is applied to the T1 gate. As SL_{-OE} is set to V_{set} , the memristor comparator operates in writing mode. Now start a simulation for both circuit (b) and circuit (c). In circuit (b), V_{DL} will sweep and the output voltage V_{out} will start to rise as discussed before. In circuit (c), the memristor conductance will increase because the memristor will be programmed under a high VDD and V_{set} . Thus, the continuously rising conductance will pull down the output voltage. When the output voltage of circuit (c) is decreased to V_{dth} , it's obvious that at this moment circuit (c) has the same working points as circuit (b) when the output voltage of (b) rises also to V_{dth} . Hence, when V_{out} reaches V_{dth} in circuit (c), the memristor in this circuit has a conductance of G_{mem} , which is the same as the conductance of the resistor in circuit (b).

The above deductions prove that when the output voltages of these two circuits are the same, the memristor conductance in circuit (c) equals to the resistor conductance in circuit (b), and thus at this moment Equation. 4 originally calculated for circuit (b) is also valid for circuit (c) (Conclusion (3)).

Based on Conclusion (1),(2) and (3), a deduction can made be that programming the memristor conductance within circuit (a) can be switched to using a V_{DLP} as input in circuit (c), and wait until the output voltage drops to V_{dth} . (Conclusion (4)) It's obvious that circuit (a) and circuit (c) can represent the working status of the search mode and the program mode of aCAM cells. Consequently, Conclusion (4) provides an algorithm to program the memristors. Using this algorithm the memristor conductance can be calculated based on Equation. 2 and Equation. 4:

$$G_{mem} = K' \frac{W}{L} \left[\frac{(V_{DLP} - V_T)^2}{2(V_{set} - V_{dth})} - \frac{3}{4} V_{read} \right]$$
(5)

Equation. 5 demonstrates that for the same memristor comparator circuit, a LUT between programming voltage (V_{DLP}) and the programmed memristor conductance (G_{mem}) can be built. An example LUT is shown in Table.1. In this table V_{dth} is set at 1.2 V. The equations above are calculated under the assumption that the transistor operates with a common long-channel quadratic function in the saturation region. In reality, the equation between V_{DLP} and G_{mem} depends on the transistor technology. In this paper, the simulations use TSMC 28nm technology. The transistor follows a linear function in the saturation region, and thus the programmed memristor conductance shows a linear relationship with the programming voltage.

2.3 Programming circuit

To achieve the LUT-based memristor programming algorithm proposed above, the programming circuits for 10T2M LB cell is designed in Fig. 3b. For all descriptions below, please refer to this diagram. Because the LB programming circuit and the HB programming circuit have similar circuit behaviors, only the programming operations in the LB cell will be demonstrated in this subsection. To set the memristor, the programming process can be roughly divided into 3 phases:

In the first phase (ϕ 1:Prepare Phase), V_{INV} is charged to a high voltage level (HIGH), and $V_{NORL[0]}$ must remain at a low voltage level (LOW). In this case, the ML voltage V_{ML} is locked at HIGH. This will make VSL_{AE} tend to connect the GND and VSL_{OE} tend to connect V_{SET} . Now the whole circuit is ready for setting the memristor.

At the beginning of $\phi 2$ (Set Phase), V_{STOP} , $V_{NORL[0]}$ and V_{SET} should be charged with corresponding high voltage. $V_{DL_lb[0]}$ also needs to receive the programming voltage. After these signals get stable the conductance of the memristor will gradually increase, making V_{out} descend slowly until reaches its threshold (V_{dth}) , as shown in Fig. 3c.

After V_{out} reaches its threshold V_{dth} , then the circuit comes to $\phi 3$ (Stop Phase). When V_{out} tends to be pulled down, V_{MLC} on the other hand, will continuously rise to HIGH, which will pull down V_{ML} . In the circuit, the trend of ML pull-down will be strengthened by the ML inverter (INV_{ML}) and the ML PMOS (T0). At the same time, because ML controls the set-reset peripheral circuit, a lower V_{ML} will lead to a higher VSL_{AE} and a lower VSL_{OE} , which will switch the set-reset peripheral circuit tile to the resetting state. Besides, a rising VSL_{AE} will



Figure 3: (a) 1T1R set-reset periphery circuit. If V_{CTRL1} is high and V_{CTRL0} is low, a reset of the memristor is performed (reset state); If V_{CTRL1} is low and V_{CTRL0} is high, a set operation will be performed (setting state). (b) LB programming circuit. This circuit receives three power signals (V_{STOP} , V_{SET} and V_{INV}) and two control signals ($V_{NORL[0]}$, $V_{DL \ [b][0]}$) from an external power source, within which $V_{DL \ [b]0]}$ is the only signal that decides the conductance of the programmed memristors. The basic idea behind these circuits is to quickly switch the set-reset peripheral circuit from the setting state to the resetting state when V_{out} reaches a threshold (V_{dth} in Fig. 3d). However, because of the higher memristor reset thresholds and the body effects of the transistor, a smaller V_{STOP} used in the programming circuits won't actually reset the device but merely stop the setting process. (c) Expected Vout transient response. The three phases of the programming circuit come from the changes of Vout. (d) Simplified aCAM array architecture. The proposed array consists of eight 10T2M aCAM cells (8 LB cells and 8 HB cells) in four rows and two columns, which means the array can store four different words at the length of two. All the aCAM cells are programmed using one single programming circuit. The array receives power and control signals from an external power source.

reduce the source voltage of T15 and to a further extent reduce V_{out} . With the above positive feedback, V_{out} drops to LOW at an extremely fast speed.

To reset the memristor, a high voltage needs to apply at $V_{NORL[0]}$, then very high voltage needs to apply at $V_{DL_lb[0]}$ and V_{STOP} . After signals are set up, the memristor can be reset to the lowest possible conductance.

2.4 aCAM array design

For convenience, if the aCAM cell (Fig. 2) is drawn with LB and HB blocks, a simplified architecture of the proposed 8-Cell aCAM array design is shown in Fig. 3d. The array has four working modes: Writing Mode (WR), Resetting Mode (RST), Sweeping Mode (SW), and Verify Mode (VR). Besides, the array has 2 states: the programming state and the searching state. In the programming state, the array is programming the memristor in LB or HB cells to different conductance levels, followed by some checking and verification work. In the searching state, the parallel V_{DL} is input to the array and the array will check if there is a match in a row.

The functions of each working mode are listed below:

- 1. In the WR, the conductance of the memristor in an LB cell or an HB cell is set to the desired value.
- 2. In the RST, the memristor is reset to the lowest possible conductance.
- 3. In the SW, a voltage sweep between 0 to 0.6 V is used at V_{DL} . This mode is used to check whether the aCAM cell works normally.

4. In the VR, 1.9 V is applied at V_{DL} . This mode is used to precisely measure the memristor conductance.

SIMULATION RESULTS 3

An attractive feature of the proposed analog feedback-controlled programming circuits is the possibility to program the memristor conductance only using the data line voltage VDL as a input parameter. To test whether the proposed memristor programming circuits and the aCAM array can achieve the programming functions, simulations for both single-cell programming and array programming have been performed. In the single-cell programming, the results Fig. 5a shows that the programmed conductance shows a linear relationship within a certain range of programmable V_{DL} , which also corresponds to the memristor comparator's dynamic range. Fig. 5b and Fig. 5c show that the programming process under high programming V_{DL} will be stopped earlier by the end of the WR Mode.

Fig. 4c shows the memristor conductance changes of all 8 aCAM cells. Because before setting an LB or HB cell the memristor in this cell is reset to the lowest conductance, the figure proves that setting or resetting a specific cell won't affect other cells. Figure. 4d illustrates the function of aCAM. In the Programming State, 8 aCAM cells in 4 rows are programmed with 4 different matching ranges (windows). Then in the Searching State, when a sweeping V_{DL} is used as input, it's clear to see the shapes of these windows.



Figure 4: (a) A part of wire connections of 2 aCAM cells. Because DL (in columns) and SL_{+AE} (in rows) need to be activated in the Reseting Mode, other cells won't be affected if an LB or HB cell is chosen to reset. Similarly, in the Writing Mode, ML (in rows) and DL (in columns) need to be used, thus setting one single LB or HB cell won't set other nearby cells. (b) The proposed aCAM array is programmed with 4 different words. This diagram shows the transient response of the memristor conductance within 8 LB cells and 8 HB cells. (c) When the same V_{DL} sweeping voltage for searching is applied, the array programmed as Fig. 4b shows four distinct analog windows (matching ranges).



Figure 5: (a) One single LB and HB Cell programming results. In the simulations of single-cell programming, a DC V_{DL} ranging from 0.75 V to 1.8 V (with a fixed step at 0.05 V) is used to set the memristors. The maximum programming period is 35μ s. It's obvious that the programmed conductance shows a linear relationship within a certain range of programming V_{DL} . (b) LB cell V_{out} transient response. The programming time of the memristor first decreases and then increases with the rising V_{DL} (c) HB cell V_{out} transient response. The programming time of the memristor also first decreases and then increases with the rising V_{DL}

4 CONCLUSION

In this article, we implement an analog feedback-controlled memristor programming circuit, which leverages the natural relationship between memristor conductance and the programming data line boundary voltage in memristor CAMs. The simulation results show that the proposed programming circuits meet the expected transient response and could achieve the LUT-based memristor programming algorithm. In addition, we manage to integrate eight 10T2M aCAM cells with a single programming circuit. The simulations prove that the proposed array architecture can achieve the functions of an aCAM array.

Despite the benefits of the proposed hardware architectures, the memristor devices still have many non-ideal characteristics, such as device to device and cycle to cycle variability, read noise and conductance drifts, which are not considered in this article. In addition, the ML parasitics of the proposed array are not fully counted in the simulations, which may affect the final results of the read/write speed and memory density. The aforementioned non-idealities will be considered and analyzed in our future work.

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