

AgileWatts: An Energy-Efficient CPU Core Idle-State Architecture for Latency-Sensitive Server Applications

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User-facing applications running in modern datacenters exhibit irregular request patterns and are implemented using a multitude of services with tight latency requirements (30–250 μ s). These characteristics render existing energy-conserving techniques ineffective when processors are idle due to the long transition time (order of 100 μ s) from a deep CPU core idle power state (C-state). While prior works propose management techniques to mitigate this inefficiency, we tackle it at its root with AgileWatts (AW): a new deep CPU core C-state architecture optimized for datacenter server processors targeting latency-sensitive applications.

AW drastically reduces the transition latency from deep CPU core idle power states while retaining most of their power savings based on three key ideas. First, AW eliminates the latency (several microseconds) of saving/restoring the core context when powering-off/on the core in a deep idle state by i) implementing medium-grained power-gates, carefully distributed across the CPU core, and ii) retaining context in the power-ungated domain. Second, AW eliminates the flush latency (several tens of microseconds) of the L1/L2 caches when entering a deep idle state by keeping L1/L2 content power-ungated. A small control logic also remains ungated to serve cache coherence traffic. AW implements cache sleep-mode and leakage reduction for the power-ungated domain by lowering a core’s voltage to the minimum operational level. Third, using a state-of-the-art power efficient all-digital phase-locked loop (ADPLL) clock generator, AW keeps the PLL active and locked during the idle state, cutting microseconds of wake-up latency at negligible power cost.

Our evaluation with an accurate industrial-grade simulator calibrated against an Intel Skylake server shows that AW reduces the energy consumption of Memcached by up to 71% (35% on average) with <1% end-to-end performance degradation. We observe similar trends for other evaluated services (MySQL and Kafka). AW’s new deep C-states C6A and C6AE reduce transition-time by up to 900 \times as compared to the deepest existing idle state C6, while consuming only 7% and 5% of the active state (C0) power, respectively.

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1. Introduction

Large datacenters running user facing applications are using inefficiently their servers *due to the killer microseconds* [1–3]. Killer microseconds refer to microsecond-scale *idleness* during CPU execution caused by a combination of two major trends. First, various events (e.g., related to NVM storage, faster datacenter networking, and main memory) with latencies in the range of microseconds are prevalent [1, 4, 5]. Second, a new software architecture is deployed in datacenters based on *microservices*, i.e., a large application composed of numerous interconnected smaller services that explicitly communicate with each other. Such applications exhibit irregular request streams, and their services have very tight (i.e., few tens to few hundreds of microseconds) latency requirements [6].

Table 1 reports a typical hierarchy of *core idle states* (i.e., C-states: C0, C1, C1E, and C6)¹ and our new proposed idle states: C6A and C6AE (which replace C1 and C1E; see Sec. 4). The Table shows for each state and two frequency levels (base: P1, and minimum: Pn) the power consumption of a modern server CPU core.² Clearly, the C-state that a CPU core resides in determines the core’s power. Transitioning to a deeper (or shallower) C-state incurs a transition latency during which the core cannot perform useful work. Consequently, power management controllers only switch to a deeper C-state if they predict that waking-up will not be needed before a target residency time.

Under commonly-used C-state transition policies, servers running latency-critical services rarely enter a deep idle power state (e.g., C6) because: 1) residency time is hard to guess, as the duration of busy/idle periods is irregular; and 2) stringent service latency requirements (30–250 μ s [4, 16]) cannot be met when transitioning out of a deep C-state requires tens or hundreds of microseconds. As a result, idle CPU cores only briefly enter shallow C-states (e.g., C1), with

¹C-states that further reduce idle power at the *package-level* (e.g., C8) take longer to transition and require longer residency times [7–9].

²The microsecond-scale transition times in Table 1 represent the worst-case software+hardware entry+exit latency (to start executing the first instruction) and not the actual hardware transition latency[10]. For example, the hardware transition latency for the C1 C-state is only a few nanoseconds (cycles) since C1 mainly performs clock-gating (Fig. 3(a))[11–14].

Table 1: C-states available on the Intel Skylake server (SKX) core [15] and AW’s new C6A and C6AE C-States.

Core C-state	Transition time ²	Target residency time	Power per core
C0 (P1)	N/A	N/A	~4W
C0 (Pn)	N/A	N/A	~1W
C1 (P1)	2μs	2μs	1.44W
C6A (P1)	2μs	2μs	~0.3W
C1E (Pn)	10μs	20μs	0.88W
C6AE (Pn)	10μs	20μs	~0.23W
C6	133μs	600μs	~0.1W

limited power savings.

We claim that the inefficiency of the C-state hierarchy with respect to microsecond-latency events is not fundamental, but a byproduct of being *oriented for client* systems. Major server vendors often design a base microarchitecture upon which both client and server CPUs are built. For example, Intel CPU core design is a single development project where client and server processors are based on the same master design [17, 18]. Within such a project, energy optimizations are mostly targeted towards client CPUs, which are used in battery-operated devices, while server CPUs are mostly optimized for performance. Therefore, features such as C-states are designed for client applications (e.g., video playback, conferencing, gaming [19, 20]), which, in contrast to latency-critical microservices, typically present long and predictable idle periods, allowing processors to exploit existing deep package C-states (i.e., C7, C8, C9, and C10) [21–24] with even larger transition latencies. For example, a client CPU spends >80% of video streaming time in the C8 package C-state [25].

Prior work (Sec. 8) proposes management techniques to enable datacenter processors to leverage existing deep C-states effectively (without changing the C-state architecture). In contrast, our **goal** is to directly address the root cause of the inefficiency, namely the high transition latency (tens or hundreds of microseconds; see Table 1) to/from deep C-states. We propose *AgileWatts (AW)*, a new deep C-state architecture optimized for processors in modern datacenters running user-facing latency-sensitive workloads. AW markedly reduces the transition latency of deep idle power states, while retaining most of their power savings, making deep C-states usable in such datacenter services. AW redesigns the state-of-the-art CPU core deep C-states based on **three power management techniques**. First, instead of shutting off the core power when entering a deep C-state, AW uses medium-grained power-gates distributed across the core and maintains the core context in the power-ungated domain. This approach shaves off several microseconds by removing the need to save and restore the context. Second, instead of shutting down private caches (i.e., L1 and L2), which requires flushing and adds several microseconds to the transition latency, AW keeps them power-ungated, along with a small control logic for cache coherence. AW implements a sleep mode in caches that helps reduce the core voltage to a minimum operational level and limit leakage power of the power-ungated domain.

Third, instead of shutting down the clock distribution, AW clock-gates the core components and clock distribution, while keeping the power-efficient all-digital phase-locked loop (ADPLL [26]) clock generator on and locked. Keeping the ADPLL on shaves few more microseconds of transition latency at a minimal extra idle power consumption.

While we demonstrate the potential of AgileWatts for Intel server processors, which represent more than 80% of the server processor market [27], our proposed techniques are general and applicable to most server processor architectures.

This work makes the following **contributions**:

- To our knowledge, AgileWatts (AW) is the first practical highly-efficient core C-state architecture, directly targeting the energy inefficiency of killer microseconds for datacenter servers running latency-critical applications.
- AW dramatically reduces the transition latency of deep idle states while keeping almost all of their power savings.
- AW architecture employs medium-grained power gating and voltage control to reduce the need for saving/restoring the microarchitectural context and flushing caches. As a result, AW saves several tens of microseconds of transition latency to/from a deep idle C-state.
- Our evaluation shows that AW significantly reduces (by up to 71%) the energy consumption of the evaluated services. AW’s new deep C-states have up to 900× faster transition latency than that of the existing deepest idle core c-state C6 while their power consumption is only 5%-7% of that of the active state (C0).

2. Motivation

Before diving into details, we analyze the opportunity of a new, agile deep idle state for datacenter processors.

It is well known that servers running latency-critical applications usually operate at low utilization 5%–25% [28, 29, 184–187] to keep tail latency under control. It is also understood that dynamic workload behavior prevents modern cores from entering deep idle states during idle periods of such application. Previous work shows that, for a key-value store (e.g., Memcached [30]) workload, cores never enter a C-state deeper than C1 (the shallowest C-state, see Table 1) when running at 20% or higher load [28, 31] (our experiments in Sec. 7 confirm this). A search workload is slightly more efficient, with cores reaching deeper C-states 20% of the time at 25% load, but only 5% of the time at 50% load, thus still spending 55% and 45% of the time in C1, respectively [28]. These examples point to a large opportunity for a new C-state that has a transition latency similar to C1 but much lower idle power than the 1.44W of C1.

Since the deepest C-state is C6 (Table 1), we estimate an upper bound of the average power (AvgP) savings for the ideal case of a deep idle state with the latency of C1 (i.e., 2μs)

and the power of $C6$, i.e., $0.1W$ per core, using Eq. 1.

$$\begin{aligned} AvgP_{baseline} &= \sum_{i \in \{0,1,6\}} (R_{C_i} \times P_{C_i}) \\ AvgP_{savings} &= R_{C_1} \times (P_{C_1} - P_{C_6}) \\ AvgP_{savings\%} &= (AvgP_{savings} / AvgP_{baseline}) \times 100 \end{aligned} \quad (1)$$

R_{C_i} denotes the residency at power state C_i , i.e., the fraction of time a CPU core spends in state C_i . P_{C_i} denotes the average CPU core power in state C_i (reported in Table 1).

Referring to our examples from prior work [28, 30, 31], given 1) the C-state residencies for the search workload at 50% and 25% loads (i.e., $R_{C_0} = 50\%$, $R_{C_1} = 45\%$, $R_{C_6} = 5\%$ and $R_{C_0} = 25\%$, $R_{C_1} = 55\%$, $R_{C_6} = 20\%$), and for the key-value store at 20% load (i.e., $R_{C_0} = 20\%$, $R_{C_1} = 80\%$, $R_{C_6} = 0\%$), and 2) C-states power from Table 1: then there is potential for a 23%, 41%, and 55% reduction in core power for the three loads, respectively. Lighter loads can have even higher power savings.

The rest of the paper illustrates how AW can enable a large part of this substantial power-saving opportunity by defining a new low-latency deep idle state we call $C6A$ ($C6$ Agile).

3. Background

We provide a brief overview of different power management components and techniques used in modern processors.

Server and Client Cores. Major server vendors have nearly the same core microarchitecture for client and server CPUs. For example, Intel CPU core design is a single development project that has two derivatives, one for server and one for client CPUs [17]. Fig. 1 shows the AVX and L2 extension of the Intel Skylake server core over the client core [18].

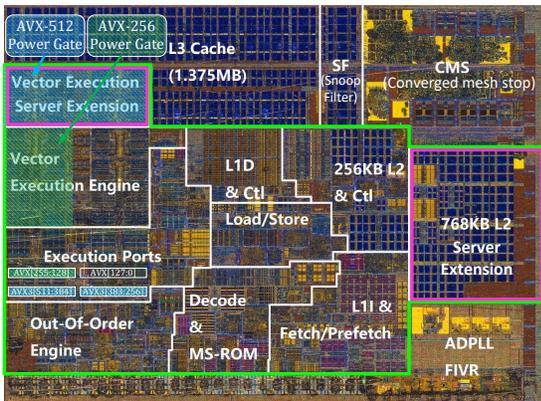


Figure 1: An Intel Skylake server core slice [32]. The core is bordered with green, and the AVX-512 and L2 extensions [18] (unavailable in client CPU cores) are bordered in pink. The 256-bit and 512-bit AVX units have separate power gates [26, 33–35], as shown in the figure.

Clock Distribution Network (CDN). A CDN distributes the signals from a common point (e.g., clock generator) to all the elements in the system that need it. Modern processors use an all-digital phase-locked loop (ADPLL) to generate the CPU core clock [36]. An ADPLL maintains high performance

with significantly less power as compared to conventional PLLs. For example, the power of an ADPLL in Skylake, shown at the bottom right of Fig. 1, is only $7mW$ at $4GHz$ [26].

Power Delivery Network (PDN). The three commonly-used PDNs in modern CPUs are: 1) *integrated voltage regulator* (IVR) [36–39], 2) *motherboard voltage regulator* (MBVR) [26, 40, 41], and 3) *low dropout voltage regulator* (LDO VR) [42–46]. For example, recent Intel server CPUs implement a fully-integrated voltage regulator (FIVR) per core, as shown at the bottom right of Fig. 1 [17, 26].

Staggered Power-gate Wake-up. Power-gating is a technique that is used to eliminate leakage of idle circuits [7, 8, 47, 48]. Typically, the wake-up latency from a power-gated state requires a few to tens of cycles [7, 49]. However, to reduce the worst-case peak in-rush current [50–53] and voltage-noise in the PDN (e.g., di/dt noise [7, 8, 54]) when waking up a power-gate, a power-gate controller uses a *staggered* wake-up technique [50–52], shown in Fig. 2.

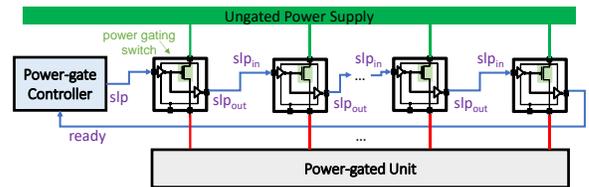


Figure 2: Staggered power-gate wake-up by daisy-chaining the control signals of the power-gating switches.

The technique turns on different power-gate switch cells in a staggered manner, to limit the current spike from the power supply. To do so, the input sleep (slp_{in}) and output sleep (slp_{out}) signals of the switch cells are daisy-chained. The controller issues a signal to the first slp_{in} , and it receives an acknowledgement ($ready$) from the last slp_{out} , indicating that the power-gate is fully conducting. An alternative wake-up technique groups switch cells into multiple chains each in a daisy-chain configuration. Doing so allows the power-gate controller to tune (e.g., post-silicon) a unit’s wake-up time by controlling the assertion time for each chain. Modern CPUs implement the staggering technique [49, 55, 56]; e.g., the Intel Skylake core staggers the wake up of the AVX power-gates over $15ns$ to reduce in-rush current [26][35, Sec. 5].

Core C-states. Power saving states enable cores to reduce their power consumption during idle periods. Modern processors support various C-states, for example, Intel’s Skylake architecture offers the following four: $C0$, $C1$, $C1E$, $C6$ [7, 8, 57]. Table 2 describes the state for various core components for each existing core C-state as well as in our proposed idle states: $C6A$ and $C6AE$ (which replace $C1$ and $C1E$, Sec. 4). While C-states reduce power consumption, during the entry-to and exit-from a C-state a core cannot be used. For example, it is estimated that $C6$ requires $133\mu s$ of transition time (Table 1). As a result, entry-exit latencies can degrade the performance of services that have microsecond-level processing latency requirements, such as in user-facing

applications [30].

Table 2: Skylake server core components’ states in core C-states, including AW’s new C6A and C6AE C-States [58].

C-State	Clocks	ADPLL	L1/L2 Cache	Voltage	Context
C0	Running	On	Coherent	Active	Maintained
C1	Stopped	On	Coherent	Active	Maintained
C6A	Stopped	On	Coherent	PG/Ret/Active	In-place S/R
C1E	Stopped	On	Coherent	Min V/F	Maintained
C6AE	Stopped	On	Coherent	PG/Ret/Min V/F	In-place S/R
C6	Stopped	Off	Flushed	Shut-off	S/R SRAM

Core C-state Entry and Exit Flows. The C1/C1E, and C6 entry and exit flows are shown in Figs. 3(a) and 3(b), respectively, and are discussed in detail in [11–14].

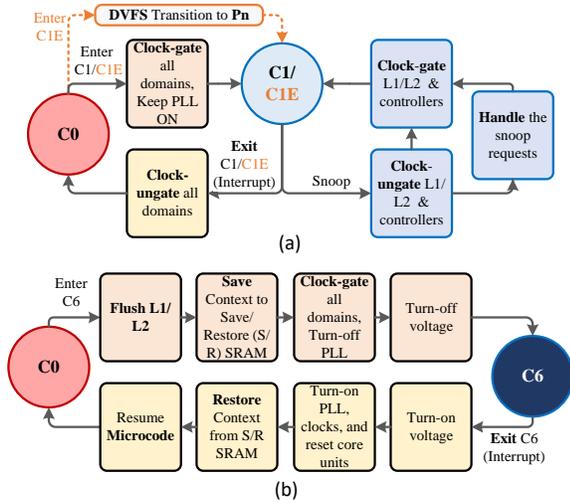


Figure 3: Entry and Exit Flows for (a) C1 and (b) C6.

Core C6 Entry/Exit Latency. We analyze the C6 entry/exit latency based on an x86 implementation [11]. C6 entry latency is dominated by the L1/L2 cache flush time. This flush time varies depending on 1) the fraction of cache lines that are dirty and 2) the core frequency, when entering C6; e.g., flushing a 50% dirty cache at 800MHz takes $\sim 75\mu\text{s}$. The time to transfer core state to/from the save/restore (S/R) SRAM depends on the core clock frequency; e.g., at 800MHz, the latency is $\sim 9\mu\text{s}$. Including control flow overhead and the power-gate controller latency, the overall CPU core C6 entry time is $\sim 87\mu\text{s}$.

C6 exit latency is significantly faster, taking $\sim 30\mu\text{s}$ from the wake-up interrupt to resuming core execution. This latency includes $\sim 10\mu\text{s}$ for hardware wake-up, including power-ungating, PLL relock, reset, and fuse propagation. State and microcode restoration takes $\sim 20\mu\text{s}$ [11–14].

4. AgileWatts (AW) Architecture

AW introduces a new core deep idle power state, C6A (C6 Agile), with close to zero-Watt power consumption and nanosecond-scale entry/exit latency. Thanks to its low latency, servers running latency-critical applications can enter C6A during short and irregular idle periods, unlocking significant energy savings. Additionally, AW defines C6AE (C6A

Enhanced, analogous to C1E), a lower-power variant of C6A that further reduces leakage power by lowering core voltage to a minimum operational level. Our discussion focuses on the C6A design and operation and points out C6AE differences when relevant.

The C6A state is based on two key ideas: *Units’ Fast Power-Gating* (UFPG) (discussed in Sec. 4.1) and a *Cache Coherence and Sleep Mode* (CCSM) (discussed in Sec. 4.2). The new power management flow that coordinates the UFPG and the CCSM at nanosecond granularity is presented in Sec. 4.3.

4.1. Units’ Fast Power-Gating (UFPG)

AW UFPG is a low-latency power-gating (PG) architecture that shuts off most of the core units while retaining the context in place, thus, enabling a transition latency of tens of nanoseconds. Conventional context retention techniques (see C6 C-state flow in Fig. 3(b)) sequentially saves/restores the context to/from external SRAM before/after power-gating/un-gating [11, 24, 26, 35]. This process adds several (e.g., 5–10 μs) microseconds to the entry/exit latency. Instead, AW retains the context in place, completely removing that overhead at a very small additional idle power cost.

AW enables in-place context retention with a *medium-grain* PG approach. This is in contrast to the *coarse-grain* PG used in Skylake client cores, where the entire core is under the same power gate [26, 40, 59, 60] and context is saved/restored externally. Our approach leverages the same ideas used by the PG for the AVX-256 and AVX-512 core units [26, 33–35] in recent server and client cores (see Fig. 1). These PG techniques require only 10 to 20 nanoseconds to power-gate/un-gate a unit [26] [35, Sec. 5] because they power and retain the unit’s context in place and avoid having to save and restore it externally.

AW’s *medium-grain* power gating applies to the majority of the core units (shaded red in Fig. 4) and excludes the L1 and L2 and their controllers (handled separately in Sec. 4.2).

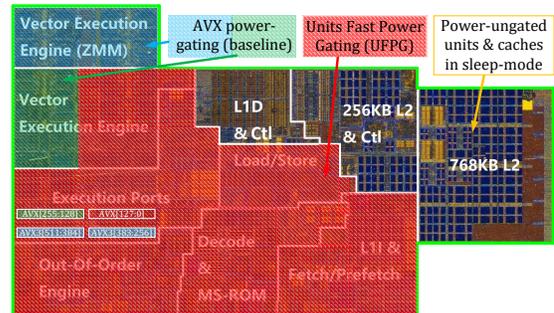


Figure 4: Medium-grain PG for the majority (area shaded in red) of the core units, excluding the L1 and L2 caches and their controllers.

Within the medium-grain PG region, AW leverages multiple techniques to retain the context in place, and enable fast (several-nanosecond) transition latency. The context of

a modern CPU core is $\sim 8\text{KB}^3$ (estimated as the amount of state that C6 saves) [61, 62] and falls into two categories: i) *registers*, such as configuration and status registers (CSRs) or fuse registers, and ii) *SRAMs*, such as firmware persistent data and patches [11, 24]. We discuss next three techniques AW uses to efficiently retain the context during C6A; the first two apply to registers and the third to SRAM.

4.1.1. Placing Unit Context in the Ungated Domain.

One option to retain the context of a power-gated unit is to place its registers outside the power-gated region, i.e., in the core’s un-gated domain, as shown in Fig. 5(a). This is suitable for units with small context (e.g., execution units); Intel likely uses this technique for the AVX execution units [33, 63]. AW uses this technique for all core units that require only a local context to be retained, i.e., this is not applicable to a unit with a distributed context that is impractical to relocate to a centralized un-gated region. The following units satisfy this requirement: 1) all execution units (besides AVX), 2) execution ports, and 3) the out-of-order engine.

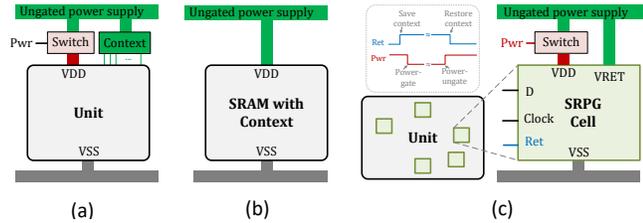


Figure 5: Context retention techniques AW uses when power-gating a unit: (a) Placing context in the core un-gated power domain; (b) placing SRAM with context (e.g., microcode patch) in the core un-gated power-domain; (c) using SRPG cells for distributed context.

4.1.2. State Retention Power Gates (SRPGs). Moving distributed or large context to a separate un-gated area is impractical (e.g., due to timing and wiring constraints). For this reason, AW employs a different retention technique – SRPGs – for units that contain such context. As Fig. 5(c) illustrates, SRPG (i.e., a retention flip-flop) is a special flip-flop fed with two supplies: power-gated and power-ungated. Such a flip-flop typically contains a shadow flip-flop to retain its state when the unit it resides in is power-gated [63–65]. For example, Intel uses this technique in the chipset to retain the state of autonomously power-gated units [33].

4.1.3. Place SRAM Context in Ungated Power Supply.

Part of the CPU core context is located in SRAMs [24]. While the microcode firmware is stored in read-only memory, known as microcode sequencer ROM (MS-ROM), microcode patches and data are stored in a $\sim 2\text{KB}$ SRAM [66, 67]. This SRAM is initialized at boot time and should be retained

³[24] shows that the context saved/restored for an entire Skylake client mobile SoC is $\sim 200\text{KB}$. This includes the context of four cores, an integrated GPU, the uncore, and the system agent. We estimate the single-core context based on a core’s relative die area, showing $\sim 8\text{KB}$ context, similar to previous Intel references [61, 62].

when power-gating the microcode unit. The C6 exit flow re-initializes the content of this SRAM from core’s S/R SRAM in a separate un-gated uncore domain; this process is sequential and can take several microseconds [11, 24]. AW avoids the need to re-initialize the microcode patch SRAM by powering it with a separate core un-gated supply, as shown in Fig. 5(b).

4.2. Cache Coherence and Sleep Mode (CCSM)

To avoid the high latency (tens of microseconds) to flush private caches (i.e., L1D and L2) in order to power-gate them, AW instead keeps them power-ungated (see Fig. 4) when transitioning to C6A. This has two design implications: first, AW needs to employ other power-saving techniques to reduce the power of the cache domain; and second, a core in C6A state still needs to serve coherence requests (i.e., snoops) [68, 69].

AW employs two key techniques to reduce the power consumption of the power-ungated private cache domain. First, unless a coherence request is being served, AW keeps this domain clock-gated to save its dynamic power. Second, AW leverages the *cache sleep-mode* technique [70–74], which adds sleep transistors to the SRAM arrays of private caches. These sleep transistors reduce the SRAM array’s supply voltage to the lowest level that can safely retain the SRAM content while significantly reducing leakage power.

Since private caches are not flushed when a core enters C6A, AW must allow the core to respond to snoop requests [7, 8, 40]. AW keeps the logic required to handle cache snoops in the power-ungated (but clock-gated) domain together with the private caches. It also uses minimal logic (*same logic used in C1*) to detect incoming snoop requests in an always-active (i.e., neither power-gated nor clock-gated) domain. As soon as this logic detects incoming snoop traffic, it temporarily increases the SRAM array voltage through the sleep transistors and reactivates the clock of the private caches for the time required to respond to snoop requests.

4.3. C6A Power Management Flow

AW implements the C6A flow within the core power management agent (PMA) [75]. This flow, shown in Fig. 6, orchestrates the transitioning between the C0 and C6A C-states and handles coherence traffic while in the C6A state.

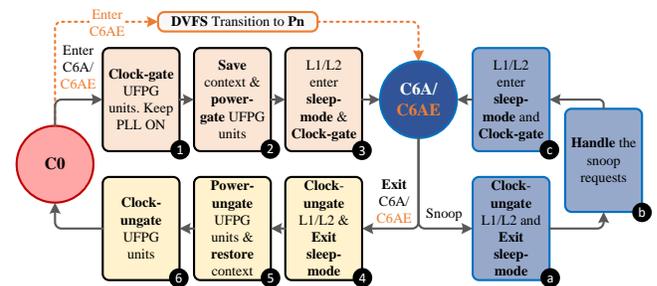


Figure 6: Power management flows for the C6A/C6AE states.

Similar to other C-states, the operating system triggers C6A entry by executing the MWAIT instruction [7, 8]. The first step ① in the entry flow clock-gates the UFPG domain (Sec. 4.1), while keeping the core phase-locked loop (PLL) powered-on. When entering C6AE, the PMA additionally initiates a non-blocking transition to Pn – the P-state with lowest frequency and voltage. Subsequently ②, the flow saves (in place) the UFPG domain context and shuts down its power. Finally ③, the flow sets the private caches into *sleep mode* (Sec. 4.2) and shuts down their clock. After these three steps, the core is in C6A (or C6AE) state.

When a *snoop* request arrives while the core is in the C6A (or C6AE), the PMA temporarily activates the private caches to respond. First, ④ the flow clock-ungates the private cache domain and adjusts its supply voltage to exit *sleep mode*. At this point ⑤, the caches can handle the snoop requests. Finally ⑥, when all outstanding snoop requests are serviced, PMA rolls back the changes in reverse order and brings the core back into the full C6A (or C6AE) state.

When an *interrupt* occurs, the core exits from C6A (or C6AE) and goes back into C0 (active) state. The exit flow is simply the reverse process of the entry flow. First ⑦, the flow clock-ungates L1/L2 and exits *sleep-mode*. Next ⑧, it power-ungates the UFPG units and triggers the restore signal to the SRPG flops (Fig. 5(c)). Finally ⑨, the flow clock-ungates UFPG units, bringing the core to the C0 active state.

5. AW Implementation and Hardware Cost

As discussed in Sec. 4, AW requires in each CPU core: 1) the UFPG subsystem, 2) the CCSM subsystem, and 3) the C6A controller. This section discusses the implementation of each component, its power-performance-area (PPA) cost, and the resulting transition latency for the new C6A and C6AE states.

5.1. PPA Modeling Methodology

Fig. 7 describes at a high level AW’s PPA modeling methodology. In this section, we describe each of the modeling components in detail. Table 3 summarizes the total area overhead and power consumption of AW’s C6A/C6AE C-states. Our power and performance model (described in Sec. 6.2) uses C6A/C6AE power and AW performance overheads to estimate the average power consumption and performance impact of AW for a given workload.

5.1.1. Units’ Fast Power-Gating (UFPG). As discussed in Sec. 4.1, AW’s UFPG places the majority of the core units behind power-gates that are similar to the ones used for the AVX units in recent Intel cores. AW uses power-gates for $\sim 70\%$ of the core area (measured on the die photo in Fig. 4). **Power overhead.** The AVX power-gates and the new UFPG, shut-off all the units in the core front-end and execution domains; however, power-gates only eliminate 95 – 97% of the leakage power [76, 77, 191], thus the UFPG domain has residual idle power while in C6A. Using the Intel core-power-breakdown tool [78], we derive the leakage power contri-

bution of the power-gated units starting from the leakage power of the entire core.⁴ Our estimation shows that the new power-gated units contribute to approximately 70% of the core leakage (i.e., $\sim 70\%$ of C1 power). Hence, the power overhead of UFPG (i.e., 3–5% of the gated leakage power) is $\sim 30\text{--}50\text{mW}$ at base frequency (P1), or $\sim 18\text{--}30\text{mW}$ at minimum frequency (Pn).

The three UFPG techniques combined retain $\sim 8\text{KB}$ context [66, 67], which consume 0.2mW at retention voltage [24]. To estimate the retention power at base (P1) and minimum (Pn) frequencies, we conservatively multiply the retention-level power by $10\times$ and $5\times$, respectively. Therefore, our estimate for context retention power is $\sim 2\text{mW}$ (P1) to $\sim 1\text{mW}$ (Pn).

Performance overhead. In an active CPU core, simultaneous operations in memory or/and logic circuits demand high current flow, which creates fast transient voltage droops [79–88]. One power-gating design challenge is the resistive voltage (IR) drop across a power gate, which exacerbates voltage droops [41, 89–93]. The worst-case voltage droop can limit the maximum attainable frequency at a given voltage since it requires additional voltage (droop) margin above the nominal voltage to enable the CPU core to run at the target frequency [79, 89, 90]. An x86 implementation of CPU core power-gate leads to $<1\%$ frequency loss [93]. Our AW analytical model (Sec. 6.2) assumes 1% *frequency degradation* due to the additional CPU core power-gates (i.e., due to UFPG).

Area overhead. A power gate adds 2 – 6% extra area to the gated logic (i.e., UFPG, covering $\sim 70\%$ of core area). We conservatively use the wide overhead range (i.e., 2 – 6%) since the exact overhead depends on the specific implementation, the exact size of the gated area, the number of required isolation-cells,⁵ and technology [76, 77, 94–96]. The area overhead for the in-place *context retention* techniques of the $\sim 8\text{KB}$ core context [61, 62] is as follows: First, moving the context of a unit to ungated-power typically requires $<1\%$ of the context area, mainly due to the isolation cells [50]. Second, the use of SRPGs for components with too large or distributed context is a mature technique already used in products, e.g., the Intel Skylake [33]. Efficient SRPG designs, which use *selective* context retention, require less than 1% additional area relative to the power-gated area they control [65, 97]. Finally, including an SRAM into the ungated domain requires isolation cells that add overhead $<1\%$ of the SRAM area [50].

5.1.2. Cache Coherence and Sleep Mode (CCSM). AW implements sleep-mode for private caches similarly to the sleep-mode used for L3 caches in multiple server products [70, 72–74]. Cache sleep-mode implements P-type sleep transistors [70, 72] with seven programmable settings and local

⁴The leakage of the entire core is approximately equal to the C1 power (Table 1), which removes only dynamic power by applying clock-gating.

⁵Isolation-cells isolate the always-on units from the floating values of the power-gated units. They are typically placed on the outputs of the power-gated domains during the physical placement stage [50].

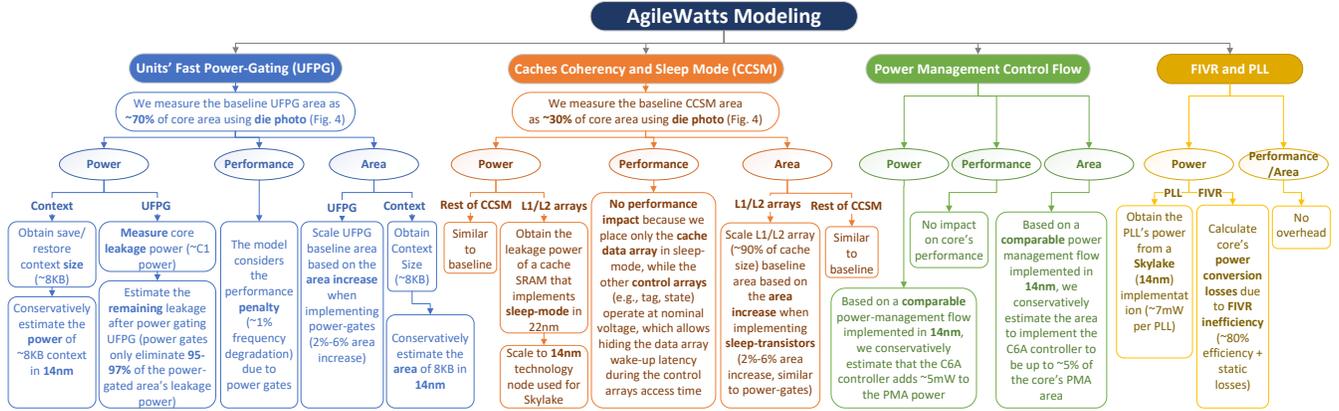


Figure 7: AgileWatts Power-Performance-Area (PPA) Modeling Methodology.

bit-line float to reduce SRAM cell leakage in the data array; it also employs word-line sleep to reduce leakage further.

Power overhead. CCSM implements sleep-mode using sleep-transistors in the L1/L2 SRAM data array; this technique is already used for efficient design of the L3 cache in multiple server processors in the market [70, 72–74]. We estimate the leakage of the L1/L2 SRAM data array when in sleep-mode, starting from the leakage of a 2.5MB SRAM L3 cache with sleep-mode that Intel implemented at 22nm [72, 98]. Based on established methodology [99], we scale⁶ this power to the cumulative L1 and L2 capacity (~1.1MB and 14nm technology node used for Skylake). The resulting leakage power estimation for the L1/L2 caches is ~55mW. We use the same method to estimate the power for the rest of the power-ungated units (controllers and tags), resulting in an additional 55mW at P1 (i.e., in C6A) voltage level. Reducing the core voltage to Pn (i.e., in C6AE) level increases the sleep transistor efficiency and reduces leakage power at Pn voltage to 40mW. This is because a sleep transistor is effectively a linear voltage regulator (LVR). The LVR power-conversion efficiency is the ratio of the desired output voltage and the input voltage; hence, the closer the input voltage to the output, the higher the power-conversion efficiency [91, 100, 101].

Performance overhead. In AW, only the data array (which accounts for more than 90% of the L1/L2 cache size) is placed in sleep-mode, while the other control arrays (e.g., tag, state) operate at nominal voltage. Doing so allows *hiding the data array wake-up latency* during the control array access time, thereby eliminating any performance degradation compared to operation without the sleep mode.

Area overhead. Implementing sleep-mode using sleep transistors for the SRAM data array of the private caches requires additional area similar to power-gates (i.e., 2–6% of the SRAM area) [71, 76, 77, 94, 95]); a recent implementation reports a 2% area overhead [96].

⁶Sec. III of [99] explains how leakage power scales with technology node size. For a dimensional scaling factor of α (i.e., $\sim 0.7\times$ when transitioning from 22nm to 14nm) and voltage scaling factor of β (varies between $\sim 0.7\times$ to a $1.0\times$; we conservatively assume no voltage scaling, i.e., $\beta = 1.0$), the leakage power scales as $\alpha\beta$ (i.e., $\sim 0.7\times$ in our case).

5.1.3. AW Power Management Control Flow. The main implementation consideration to realize the C6A flow in Fig. 6 is a mechanism to control in-rush current [26, 102]. This needs to support staggered wake-up, so as to ensure PDN stability [26, 35, 49, 55, 56, 102]. We further discuss this in Sec. 5.3. The remaining capabilities, such as clock-gating, event detection (interrupts, snoops) are all commonly supported in state-of-the-art SoCs. The C6A controller is implemented using a simple finite-state-machine (FSM) within the core’s PMA, which resides in the uncore [75] and controls clock gating/un-gating, save/restore signals, and L1/L2 entry-to/exit-from sleep-mode. The C6A snoop flow reuses the existing snoop handling mechanisms of the C1 state (shown in Fig. 3).

Power overhead. AW implements the C6A controller as an FSM within the PMA. Based on a comparable power-management flow implemented in [24], we estimate that the C6A controller adds approximately 5mW to the PMA power.

Performance overhead. The additional control circuit we add to the PMA has no direct impact on CPU core’s performance. The performance overhead is mainly due to the new features the PMA controls (described in Sec. 5.1.1 and Sec. 5.1.2).

Area overhead. Based on a comparable power-management flow implemented in [24], we estimate the additional area to implement the C6A controller to be up to 5% of the core PMA area.

5.1.4. Core PLL and FIVR. AW keeps the PLL and FIVR powered on in C6A/C6AE states. Next we describe only the power overhead of the PLL and FIVR as there is no additional performance or area overhead as compared to the baseline.

Power overhead. We estimate the C6A idle power needed by AW to keep the PLL on and locked while accounting for voltage regulator inefficiencies. The Skylake core uses an AD-PLL and a FIVR [17, 26]. The ADPLL consumes 7mW (fixed across core voltage/frequency levels [26]). The FIVR presents dynamic efficiency loss due to conduction and switching inefficiency [103], and static efficiency loss due to power consumption of the control and feedback circuits [38, 91, 103].

The static loss still applies when the FIVR output is 0V. The FIVR static loss accounts for $\sim 100\text{mW}$ per core [41, 91, 104]. The FIVR efficiency at light load is about 80% (excluding the static power losses) [41, 90, 91].

5.2. C6A and C6AE Latency

We estimate the overall transition time (i.e., entry followed by direct exit) for the C6A and C6AE states of AW to be $< 100\text{ns}$. This is three orders of magnitude faster than the $> 100\mu\text{s}$ latency of C6. Next, we explain in detail this estimation by referring to the flow in Fig. 6.

5.2.1. C6A and C6AE Entry Latency. Clock-gating all domains and keeping the PLL ON (1 in Fig. 6) typically takes 1–2 cycles in an optimized clock distribution system [105, 106]. Transitioning to P_n (required for C6AE) happens with a non-blocking parallel DVFS (i.e., P-state) flow that can take few tens of microseconds, depending on the power management architecture [107]. Since AW keeps the context in-place; saving the context to power-gate the core units (2) only requires asserting the Ret signal followed by deasserting the Pwr signal, as shown in Fig. 5(c). We estimate this process to take 3–4 cycles. Finally, placing the L1/L2 caches in sleep-mode and clock-gating them (3) takes 1–3 cycles. Hence, the overall entry flow takes < 10 cycles, i.e., less than $< 20\text{ns}$ with a power management controller clocked at 500MHz .⁷

5.2.2. C6A and C6AE Exit Latency. Clock-ungating the L1/L2 caches and exiting sleep-mode (4) takes 2 cycles [70]. Power-ungating the core units (5) takes $< 70\text{ns}$ (discussed in Sec. 5.3) and restoring the core context (i.e., deasserting the Ret signal after restoring power) takes 1 cycle. Finally, clock-ungating all domains (6) typically takes 1–2 cycles. Hence, the overall exit flow takes ~ 5 clock cycles + $< 70\text{ns}$, equivalent to $< 80\text{ns}$ when using a 500MHz clock.

5.2.3. C6A and C6AE Snoop Handling. Snoop handling latency in C6A(C6AE) is similar to that in C1(C1E). Specifically, clock-ungating the L1/L2 caches and exiting sleep-mode (a) takes 2 cycles. In the first cycle, the flow ungates the clock; in the second cycle, the snoop requests simultaneously 1) access the cache tags (power-ungated), and 2) wake-up the cache data array [70, 72–74]. Placing the L1/L2 in sleep-mode and clock-gating L1/L2 caches (c) after servicing the snoop traffic (b) takes 1–3 cycles.

5.3. Staggered Unit Wake-up

As discussed in Sec. 3, rapid wake-up of a power-gated domain can result in a sudden increase in current demand (in-rush current) [50–53], which can damage a chip. Intel Skylake core’s AVX power-gating mitigates this by staggering the AVX un-gating over $\sim 15\text{ns}$ [26][35, Sec. 5]. AW can exacerbate in-rush current effects, since during C6A / C6AE exit it wakes up

a power-gated domain (i.e., UFPG, the red shaded area in Fig. 4) that has approximately $4.5\times$ the area and capacitance of the AVX units [78]. We avoid this issue by dividing the UFPG area into five zones, each with a local power-gate controller (as in Fig. 2). Each of the five controllers has a zone sleep signal ($SlpZone_i$) that is controlled by the core PMA. The PMA sequentially wakes up the five domains using the $SlpZone_i$ signals. Since each of the five zones has a smaller area than the AVX power-gated units, staggering the wake up of each zone over $\leq 15\text{ns}$ (i.e., same as AVX units) keeps the in-rush current within limits [50, 52, 102]. Hence, waking up all five domains, which have $\sim 4.5\times$ the area and capacitance of the AVX units, takes approximately $< 70\text{ns}$ ($67.5 = 4.5 \times 15\text{ns}$).

Several prior works propose nanosecond-scale staggered power-gate wake-up for different units, including the entire core. Table 4 summarizes some of these works.

5.4. Design Complexity and Effort

AW techniques involve non-negligible front-end and back-end design complexity and effort. Even though medium-grained power-gates of UFPG are less invasive than fine-grained power-gating, they still require significant back-end (e.g., power-delivery, floor-planning, place and route) effort. Moreover, the CCSM and the C6A/C6AE control flows require careful pre-silicon verification to ensure that all the hardware flows (Fig. 6) operate according to the architectural specification. The complexity and effort can be even worse if a processor vendor chooses to have two separate designs for client and server to remove AW’s overhead from client systems.

Nonetheless, AW complexity and effort are comparable to recent techniques implemented in modern CPUs to increase energy-efficiency, such as hybrid cores [112, 113]. Therefore, once there is a strong demand from customers and/or pressure from competitors, CPU vendors can implement an architecture similar to AW to significantly increase server energy efficiency.

5.5. AW Benefits to AMD Processors

Despite having a hierarchical design, which uses chiplet dies (CCDs) and clusters of CPU cores (CCXs) within each CCD [197], AMD’s modern server processors still suffer from the same issues that we pointed out in Sec. 2. Since the latency to enter/exit a CPU core deep idle state is tens or hundreds of microseconds [197], server vendors recommend disabling the deep idle C-state (Global C-State Control in BIOS) in AMD EPYC Rome/Milan-based servers to reduce performance impact [198–200]. Therefore, despite the capability to place individual idle cores (or even a cluster of cores) in a deep low-power state, this capability is typically disabled in AMD servers running latency-critical applications, which significantly increases the energy consumption of these servers [198]. AW can mitigate this issue by providing a low-power C-state with nanosecond-scale transition latency.

⁷Typically, a power management controller of a modern SoC operates at a frequency of several hundred MHz (e.g., 500MHz [108]) to handle nanosecond-scale events, such as di/dt noise [26][35, Sec. 5].

Table 3: Area and power requirements to implement AW in an Intel Skylake-like core.

Component	Sub-Component	Area Requirement	C6A Power	C6AE Power
Units' Fast Power-Gating (UFPG)	Unit power-gates (~70% of the core)	2 – 6% of power-gated area	~30 – 50mW ^α	~18 – 30mW ^α
	Ungated context registers	<1% of ungated context registers		
	State retention power-gates (SRPG)	<1% of gated unit area	~2mW ^β	~1mW ^β
	Ungated context SRAM	<1% of SRAM area		
Cache Coherence & Sleep Mode (CCSM)	L1/L2 caches in sleep-mode	2 – 6% of private cache area	55mW ^γ	40mW ^{γδ}
	The rest of the memory subsystem	<1% of the ungated units	55mW ^γ	33mW ^γ
PMA Flow	Implemented in the uncore [75]	<5% of core PMA [24]	5mW ^ε	5mW ^ε
Core ADPLL & FIVR	ADPLL	0%	7mW [26]	7mW [26]
	Core FIVR inefficiency	0%	36mW – 41mW ^ζ	23mW – 27mW ^ζ
	FIVR static losses	0%	100mW ^η	100mW ^η
Overall		3 – 7% of the core area	290 – 315mW	227 – 243mW

^αAssuming 3 – 5% [76] of leakage power \approx C1 power. ^βPower of the $\sim 8KB$ context [24]. ^γL1+L2 size is $\sim 1.1MB$; power from [98] in 22nm scaled to 14nm based on [99]. ^δHigher sleep-transistor efficiency at V_{min} (C6AE) [91, 100, 101]. ^εBased on scaled wake-up logic power from [24]. ^ζAssuming 80% FIVR efficiency in light load [41, 90, 91]. ^ηFIVR static losses [41, 91, 104] in C6 state are $\sim 100mW$ [38].

Table 4: Comparison of Core Power-gating Schemes

Technique	Core Type	Power-gating Trigger	Power-gated Blocks	Wake-up Overhead
[109]	In-order CPU	Cache miss	Register file	5 cycles
[102]	In-order CPU	Cache miss	Core	10ns
[47]	OoO CPU	Execution unit idle	Execution units	9 cycles
[110]	OoO CPU	Register file bank idle	Register file bank	17 cycles
[111]	GPU	Register subarray unused	Register subarray	10 cycles
[35]	OoO CPU	AVX execution unit idle	Intel AVX execution unit	~ 10 -15ns
AW (This work)	OoO CPU	Core idle	Most of core units	~ 70 ns

6. Experimental Methodology

6.1. Workloads and Experimental Setup

We evaluate AW using three latency-critical applications: *Memcached*, *Apache Kafka*, and *MySQL*. Memcached [114] is a lightweight key-value store that is widely deployed as a distributed caching service to accelerate user-facing applications with stringent latency requirements [115–117]. Memcached has been the focus of numerous studies [3, 118–122], including efforts to provide low microsecond-scale tail latency [104, 115, 123–132]. Kafka [133] is a real-time event streaming platform that is used to power event-driven microservices and stream processing applications. MySQL [188] is a widely-used relational database management system.

Our baseline server is equipped with two Intel Xeon Silver 4114 [134] Skylake-based processors running at a base frequency of 2.2 GHz (minimum frequency of 0.8 GHz and maximum Turbo Boost frequency of 3 GHz), with 10 physical cores for a total of 20 hyper-threads, and with 192 GB DDR4 DRAM. We use a cluster of six server machines to run the Memcached, Kafka, and MySQL services and corresponding workload clients. For evaluating Memcached, we run a single Memcached server process on one of the server machines and run a modified version of the Mutilate load generator [122] for Memcached on the remaining five server

machines. We configure the load generator to recreate the ETC workload from Facebook [135], using one master and four workload-generator clients, each running on a separate server machine. For evaluating Apache Kafka, we run a single Kafka server process on one server machine and run the ConsumerPerformance and ProducerPerformance Kafka tools on another server machine. For evaluating MySQL, we run a single MySQL server process on one server machine and run the sysbench benchmarking tool with the OLTP test profile on another server machine. In all cases, we pin the processes to specific cores to minimize the impact of the OS scheduler.

6.2. Power and Performance Model

We model the average power of a core using the fraction of time spent at each unique C-state and its corresponding power consumption. Similar to prior works [4, 16, 28, 31, 104, 136–139], we focus on CPU power which is the single largest contributor to server power [140, 141]. Next, we describe our models for the baseline and AW.

Modeling the Baseline CPU Core. Our analytical power model estimates the average CPU core power (Avg_P) for a workload, assuming P-states/Turbo are disabled, as follows:

$$Avg_P = \sum_{i \in \{0,1,1E,6\}} P_{C_i} \times R_{C_i} \quad (2)$$

P_{C_i} denotes the core power in state C_i (reported in Table 1). R_{C_i} denotes the residency at C_i , i.e., the percentage of the total time the system spends at state C_i . We obtain C-state residency and number of transitions using processor’s residency reporting counters [142]. When executing our workloads, we use the RAPL interface [143] to measure power consumption.

Modeling the AW CPU Core. We model the power consumption of the CPU core enhanced with the two new C-states of AW (i.e., $C6A$ and $C6AE$) using 1) measured data from our baseline power model; C-state residency is scaled using our performance model (more details below), and 2) estimated power of the $C6A$ and $C6AE$, as summarized in Table 3. $C6A$ and $C6AE$ C-states of AW replace the $C1$ and $C1E$, respectively, as follows:

$$AvgP = \sum_{i \in \{0,6A,6AE,6\}} P_{C_i} \times R_{C_i} \quad (3)$$

Therefore, for a given workload, we perform the following steps. 1) We obtain the power and residency of each core C-state from the baseline. We scale the C-state residency taking into account i) how the small core frequency degradation incurred due to the power-gates (Sec. 5.1.1) affects performance by considering a workload’s frequency scalability⁸ and ii) the higher $C6A/C6AE$ transition latency (i.e., $100ns$; Sec. 5.2) compared to $C1/C1E$. 2) We replace $C1/C1E$ C-state residency (i.e., $R_{C_1}/R_{C_{1E}}$) with $C6A/C6AE$ C-state residency (i.e., $R_{C_{6A}}/R_{C_{6AE}}$). 3) We replace $C1/C1E$ power consumption (i.e., $P_{C_1}/P_{C_{1E}}$) with $C6A/C6AE$ estimated power consumption (i.e., $P_{C_{6A}}/P_{C_{6AE}}$, in Table 3). We plug in the new values to estimate the average AW CPU core power.

To estimate AW’s average power for workloads with Turbo enabled (and P-state disabled), we use the following Equation:

$$AvgP_{savings} = R_{C_1} \times (P_{C_1} - P_{C_{6A}}) + R_{C_{1E}} \times (P_{C_{1E}} - P_{C_{6AE}})$$

$$AvgP_{savings\%} = (AvgP_{savings}/AvgP_{baseline}) \times 100 \quad (4)$$

where we measure $AvgP_{baseline}$ using RAPL. Doing so allows our model to take into account power consumption variation during $C0$ active state due to Turbo transitions.

6.3. Power Model Validation

The power consumption at each processor C-state and frequency step (i.e., P1 and Pn) is collected from measurements of real systems based on the Intel Skylake CPU [36], which is shown in Table 1. To validate our model, we run four representative server workloads: SPECpower [147], Nginx [148], Spark [189], and Hive [190] at multiple CPU utilization levels. We measure average power consumption and collect core C-states residencies and transitions for each run. We use our analytical power model to estimate the average power consumption of these workloads. Then, we compare

⁸We define the frequency scalability of a workload as the change in its performance with unit change in frequency, as in [107, 144–146].

the measured vs. estimated average power. We find that the accuracy of our model is 96.1% / 95.2% / 94.4% / 94.9% for SPECpower / Nginx / Spark / Hive workloads, respectively.

7. Evaluation

We first evaluate AW using the Memcached [114] workload. In Sec. 7.4 we evaluate AW with two more workloads.

7.1. Power Savings and Overhead at Varying Load Levels

Fig. 8 shows how AW affects power consumption and request latency against the baseline with P-states disabled (i.e., frequency is set to base frequency, P1) and C-states and Turbo enabled. We expect AW to achieve significant power savings, thanks to the lower power of $C6A/C6AE$ compared to $C1/C1E$, while having a small impact on request latency because of the larger transition time ($\sim 100ns$) and the $\sim 1\%$ frequency loss (Sec. 5.1.1). While the larger transition time impacts each C-state transition, the impact of the frequency loss depends on the sensitivity of the workload to the core frequency reduction.

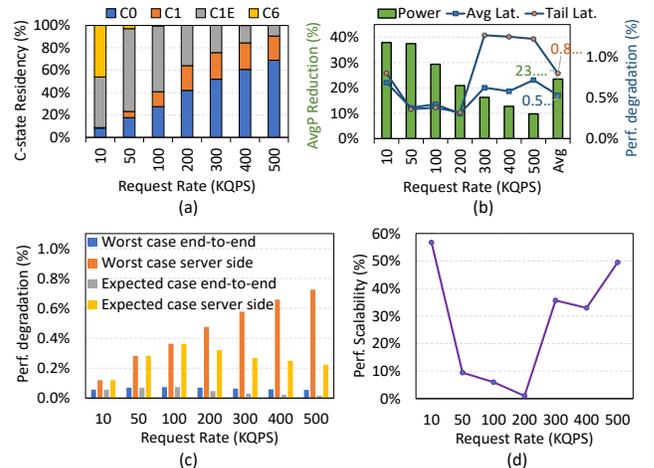


Figure 8: Comparison of AW against the baseline configuration (P-state disabled, Turbo enabled, C-state enabled) with varying request rates. (a) Residency of the baseline system at different C-states. (b) AW core average power (AvgP) reduction and average/tail latency degradation when replacing $C1/C1E$ with $C6A/C6AE$. (c) Average response time degradation. (d) Performance scalability when increasing frequency from 2 GHz to 2.2 GHz.

Fig. 8(a) shows the residency of the system in each C-state: as expected, idle time progressively reduces as load (queries per second – QPS) increases. Therefore, we expect AW to have larger power savings and lower impact on performance at low load. Indeed, Fig. 8(b) shows that AW reduces the average power consumption by up to 38% at low load, with less than 1% impact on both average and tail latency. At high load, AW still provides 10% power savings, with less than 1.3% impact on tail latency. For reference, Fig. 8(d) shows the performance scalability of Memcached to increasing core frequency from 2 GHz to 2.2 GHz (Sec. 6.2).

Fig. 8(c) further analyzes the impact of AW on average response time. We consider end-to-end (including network latency measured at 117us) and server-side response time for two cases: the worst case, where we assume a C-state transition for each query and the expected case, with the actual C-state transitions observed in the baseline. As expected, the gap between the worst and the expected case is larger at high load, since multiple queries are serviced within the same active period. We also observe that the degradation of the end-to-end response time (i.e., by client) is negligible because the (non-changing) network latency dominates the overall response time.

Google states in their paper that discusses latency-critical applications [28]: “Modern servers are not energy proportional: they operate at *peak* energy efficiency when they are fully utilized, but have much lower efficiencies at lower utilizations”. The utilization of servers running latency-critical applications is only 5%–25% to meet target tail latency requirements, as reported by multiple works from academia and industry [28, 184–187]. For example, recently, Alibaba reported that the utilization of servers running latency-critical applications is typically 10% [187]. Therefore, our AW proposal addresses the more inefficient aspect of modern servers: running latency-critical microservice-based applications at low utilization.

We conclude that AW significantly reduces core average power consumption of the Memcached service across various load levels with minimal performance overhead over the baseline when disabling P-states and enabling Turbo.

7.2. Commonly-Used Configurations

Server vendors provide recommended system configurations [149–151], such as disabling certain C-states to increase system performance or disabling Turbo Boost [75, 152] to reduce power consumption. We analyze three common configurations by modifying our baseline (which has P-states disabled and Turbo and C-states enabled) by successively disabling Turbo, C6, and C1E. Before analyzing the impact of AW on these three tuned configurations, we study them individually.

Fig. 9 reports latency (average and tail), package power consumption, and C-state residency for the three tuned configurations. We observe that NT_No_C6, No_C1E has the lowest average and tail latency, but also the highest average power across the entire range of request rates. At 500 KQPS, this configuration has ~5% and ~27% lower average and tail latency, respectively, but also has ~7% higher average package power than the other two configurations. Latency improves because disabling C1E reduces the long transition overhead of C1E (i.e., 10μs, shown in Table 1), in contrast to the other two configurations that spend significant time in C1E, as

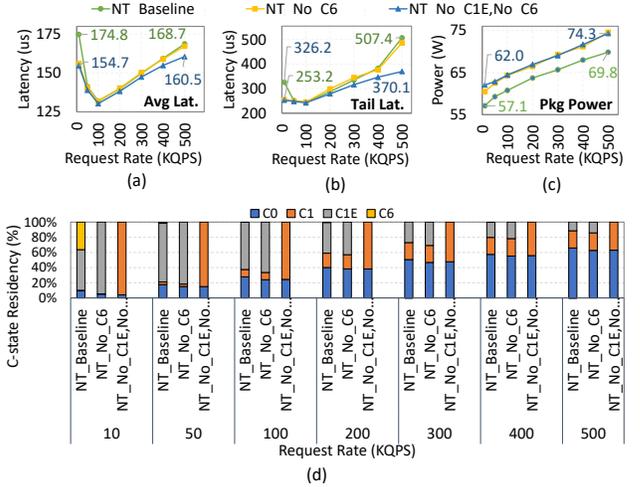


Figure 9: Analysis of three variants of the baseline configuration (NT_Baseline disables Turbo, NT_No_C6 disables Turbo and C6, NT_No_C6, No_C1E) disables Turbo, C6, and C1E) on (a) Average latency, (b) Tail latency, (c) Package power consumption, (d) C-state residency at increasing load level. All configurations have P-states disabled.

shown in Fig. 9(d).⁹ However, disabling C1E also increases average power consumption because, as shown in Fig. 9(d), the core now spends more time in C1 (the shallower C-state), which has ~63% higher power than C1E, as shown in Table 1. This analysis shows that a new C-state that consumes similar (or lower) power to C1E but with a transition time that is close to C1 can provide a low average and tail latency with reduced power consumption. Next, we show that our newly proposed C-state, C6A, achieves this balance.

Fig. 10 shows the power reduction and performance (tail and average latency) improvement of AW over the three tuned configurations. We observe that AW significantly reduces power consumption against all three tuned configurations. The reason is that, in these workloads AW replaces the time that other configurations spend in C1/C1E with the C6A/C6AE C-states, which have much lower power. Second, AW reduces average/tail latency by up to 5%/26% and 4%/24% compared to NT_Baseline and NT_No_C6, respectively, while only degrading performance by less than 1% compared to NT_No_C6, No_C1E. Based on this analysis, we conclude that AW provides average and tail latencies comparable to or better than the tuned configurations, while reducing power consumption significantly.

7.3. Analysis of Turbo Performance Improvement

To maximize performance, server vendors recommend to enable Turbo for better burst performance and disable C6 and

⁹We explain the irregular performance trends in Fig. 9 with the following observations: at low load, the cores enter C6 state, which increases the query response latency by the latency overhead required to transition from C6 to the C0 active state. As the load increases, two phenomena occur: 1) fewer transitions to C6 state and 2) queuing effects. In the mid-range load, there are fewer queuing effects and fewer transitions to C6 and that’s why the latency is lowest, whereas at high load, even though the transitions to C6 are the lowest, the latency is dominated by queuing effects.

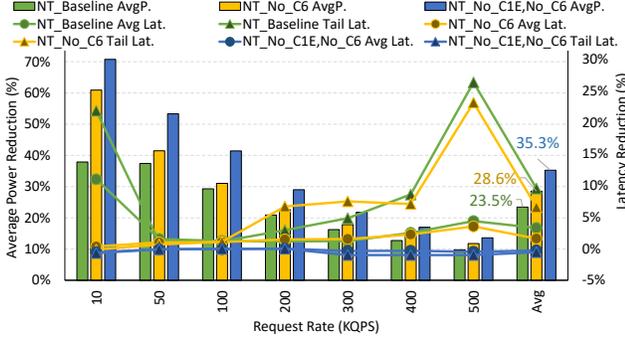


Figure 10: Power reduction and average/tail latency reduction of AW over baseline (P-state disabled, C-state enabled) with Turbo disabled (NT_Baseline), Turbo and C6 disabled (NT_No_C6), and Turbo, C6 and C1E disabled (NT_No_C6, No_C1E) across different request rates (QPS).

C1E to avoid their transition latency [149–151]. However, server vendors also note that disabling C1E can hamper performance since the processor is kept at high power, thereby not gaining enough thermal capacitance needed during Turbo Boost periods [40, 75, 151–153]. Therefore, current C-state architectures cannot benefit from removing the C1E transition overhead and enabling Turbo. In this section, we demonstrate that AW achieves high Turbo performance while eliminating the C1E performance overhead.

Fig. 11 shows the average and tail request latency for four configurations that combine enabling/disabling Turbo and the C1E and C6 C-states and highlight the effect of C-states on Turbo performance, compared to AW’s C6A state with and without Turbo.

We make **three** key observations. First, Fig. 11(a,c) show that the configuration with only Turbo and C6 disabled (i.e., NT_No_C6) increases the average/tail latency performance by up to 4%/31% over the configuration with all of Turbo, C6, and C1E disabled (i.e., NT_No_C6, No_C1E). Second, comparing Figs. 11(c) and (d) shows that enabling Turbo while disabling C1E (i.e., T_No_C6, No_C1E) does not improve performance over the same configuration with Turbo disabled (i.e., NT_No_C6, No_C1E). Third, Figs. 11(b,d) show that with Turbo enabled, only disabling C6 (i.e., T_No_C6) has the same performance as additionally disabling C1E (i.e., T_No_C6, No_C1E). The reason is that in the T_No_C6 configuration, the transition overhead of C1E on average/tail latency offsets any thermal capacitance gains and ensuing performance gains from Turbo.

We conclude that in a configuration where both C6 and C1E are disabled while Turbo is enabled, large performance benefits can be obtained by enabling C6A instead of C1, i.e., T_C6A, No_C6, No_C1E. Doing so provides larger thermal capacitance to Turbo compared to enabling C1E, and reduces the long transition latency overhead of C-states (i.e., C6 and C1E). We illustrate the potential benefits of Turbo with AW in Figs. 11(b,d) (dashed green line).

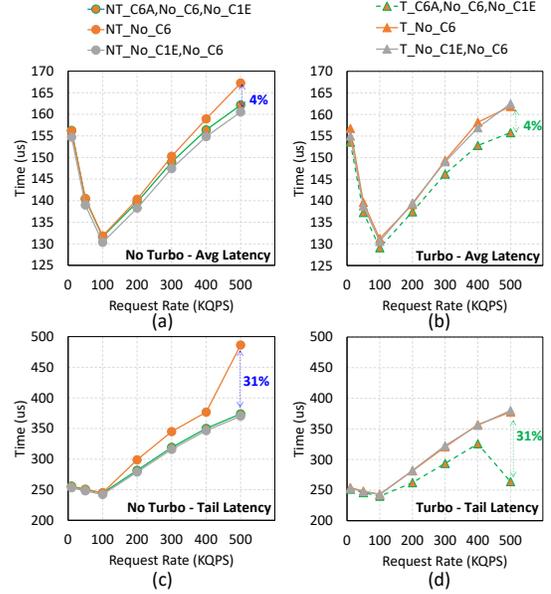


Figure 11: Average and tail latency at different request rates (QPS) for four configurations that show the effect of idle power state on Turbo performance: Turbo/No-Turbo & C6 disabled (T_No_C6/NT_No_C6), Turbo/No-Turbo & C6 & C1E disabled (T_No_C6, No_C1E/NT_No_C6, No_C1E), compared with AW: Turbo/No-Turbo & C6A enabled & C6 & C1E disabled (T_C6A, No_C6, No_C1E/NT_C6A, No_C6, No_C1E).

7.4. Analysis of Additional Workloads

Fig. 12 shows the evaluation of MySQL [188], a latency-critical workload, for three request rates (low, mid, and high). Fig. 12(a) and 12(b) show the C-state residency of the baseline configuration (P-states disabled, C1 and C6 C-states enabled) and baseline with C6 disabled, respectively.

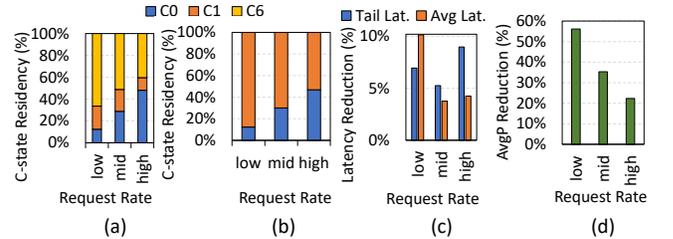


Figure 12: Evaluation of MySQL [188] for low, mid and high request rates. (a) C-state residency of baseline and (b) with disabled C6 (c) Tail and average latency reduction with C6 disabled (d) average power reduction with AW’s C6A as compared to C6 disabled.

While for all request rates the baseline has $\geq 40\%$ C6 residency, Fig. 12(c) shows that the tail and average latency is significantly (4%–10%) improved when we disable C6. Therefore, the recommended configuration is to disable C6 (Fig. 12(b)) to avoid its high transition latency. Fig. 12(d) shows significant (22%–56%) average power reduction from AW’s C6A as compared to a C6-disabled configuration (i.e., C1 residency in Fig. 12(b) mapped to C6A).

Fig. 13 shows the evaluation of Kafka [133], another latency-critical workload for two request rates (low and high).

Fig. 13(a) and 13(b) show the C-state residency of the baseline configuration (P-state disabled, C1 and C6 C-state enabled) and baseline with C6 state disabled, respectively.

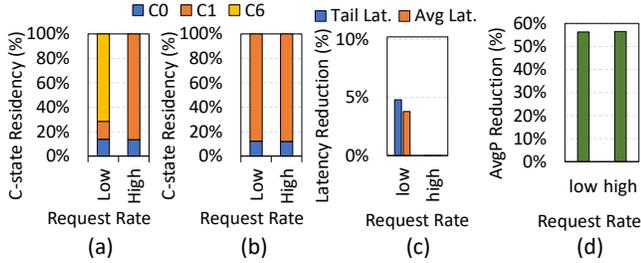


Figure 13: Evaluation of Kafka [133] for low and high request rates. (a) C-state residency of baseline and (b) disabled C6 (c) Tail and average performance improvement with disabled C6 (d) average power reduction with AW’s C6A as compared to C6 disabled.

At a low request rate, the baseline has $>60\%$ C6 residency. As shown in Fig. 13, disabling the C6 state improves the tail and average latency by 4%–5%. The high request rate point does not show a performance improvement since at high rates Kafka workload does not enter the C6 state. Fig. 13(d) shows $>56\%$ average power reduction, for both request rates, by using AW’s C6A (i.e., C1 residency is mapped to C6A) compared to having C6 disabled (shown in Fig. 13(b)).

We conclude that AW with disabled P-states and enabled Turbo significantly improves core average power for the MySQL and Kafka workloads as compared to the baseline.

7.5. Impact of High Snoop Traffic

To understand the impact of high snoop rate on AW power savings, we analyze the power consumption difference between baseline and AW while handling snoops. If a snoop arrives in baseline, then the system clock-ungates the L1/L2 subsystem (additional $\sim 50mW$ to core C1 state) and handles the snoops. In AW, L1/L2 exit the sleep mode and handle the snoops. The power difference, therefore, is mainly the L1/L2 exit from sleep mode (additional $\sim 120mW$ to C6A). To calculate an upper bound on power savings opportunity of AW compared to baseline with and without snoops, we assume a 100% idle core where the C1 (C6A) state is the only state that is enabled (i.e., $R_{C1} = R_{C6A} = 100\%$). If the core does not handle any snoop then AW power savings are $(P_{C1} - P_{C6A})/P_{C1} = 1.44 - 0.3)/1.44 = 79\%$. In case the core is handling snoops all the time during C1 (C6A) AW power savings are $(1.49 - 0.470)/1.49 = 68\%$. Therefore, in the worst case we lose an 11% power savings opportunity in case of high snoop traffic.

7.6. Data Center Cost Savings Analysis

AW enables significant power reduction even during short bursts of core idleness that are infeasible using existing core C-states. In a data-center context, all else being equal, AW power savings translate to lower operational cost since less energy

is consumed during periods that cores enter the AW idle C-states as compared to residing in the shallower legacy C-states. AW does not reduce cooling capital expenses since it does not reduce the TDP of a CPU, which can be reached during times where a CPU has high utilization and cores do not enter idle states. As a result, a data-center that employs servers with CPUs supporting AW will need to provision for the worst-case cooling needs as with CPUs with only legacy C-states. Table 5 shows AW cost savings¹⁰ from operating a CPU during a year at different load levels, assuming the CPU is running a Memcached workload. The savings range between 0.33 to 0.59 million dollars per year per 100K servers. These savings grow proportionally to the data-center PUE [195]. Besides CPU energy savings, AW’s lower idle power translates to lower time-averaged power and lower temperature that can extend a server’s lifetime (by slowing down aging) and lower maintenance costs [195]. A more detailed analysis of these aspects is beyond the scope of this work.

Table 5: AW Yearly Cost Savings (in \$M) per 100K Servers

QPS	10K	50K	100K	200K	300K	400K	500K
Savings (\$M/100K Servers)	0.33	0.59	0.58	0.53	0.47	0.41	0.34

8. Related Work

As far as we know, this is the first work to introduce a very low power processor core power-state (i.e., deep idle C-state) that provides both low transition latency and low power consumption. While low server efficiency for latency-critical workloads has been studied before, previous work proposed management and scheduling techniques to mitigate the problem, rather than addressing it directly (i.e., with a fast yet low-power processor core power state).

Modern Cloud Applications. Interactive latency-sensitive cloud applications are gradually shifting to a modular architecture based on loosely-coupled microservices to meet their software maintenance, scalability, and availability requirements [192–194]. However, the decoupled nature of microservices exacerbates the strict tail latency requirements of such applications.

Recent work [187] that characterizes large-scale deployments of microservices at Alibaba clusters shows that servicing a single user request may involve tens or even hundreds of microservices. With each microservice contributing a small amount of service time, together these can add up to a significant end-to-end service latency. Memcached appears in a significant fraction of microservices’ call graphs due to its ability to reduce the time to retrieve hot data from databases, making Memcached an important and latency critical component. The same Alibaba study also reveals that to meet the stringent tail latency requirements of microservices, Alibaba servers running latency-sensitive microservices typically operate at 10% utilization. This follows previous reports from industry

¹⁰The cost savings per server are calculated as (Average_Baseline_Power – Average_AW_Power) x Seconds_in_Year x Cost_per_Joule (assuming $\$0.125/KWh$ [196]).

and academia that the utilization of servers running latency-sensitive applications is typically 5%–20% [28, 154, 184–187]. Servers at low utilization, however, have traditionally suffered from poor energy efficiency, partly because servers running latency-sensitive tasks at low utilization also disable deep C-states to avoid the tens or hundreds of microseconds penalty of transitioning out of such deep C-states [149, 150]. This emphasizes the need for deep C-states with low transition latency and high power savings.

Fine-grained, Latency-Aware DVFS Management. Besides C-states, the other major power-management feature of modern processors is dynamic voltage and frequency scaling (DVFS). Previous work proposes fine-grained DVFS control to save power, while avoiding excessive latency degradation. Rubik [136] scales core frequency at sub-millisecond scale based on a statistical performance model to save power, while meeting a target tail latency. Swan [155] extends this idea to computational sprinting [156–159] (e.g., Intel Turbo Boost [40, 75, 152]): requests are initially served on a core operating at low frequency and, depending on the load, Swan scales up the frequency (including sprinting levels) to catch up and meet latency requirements. NMAP [160] focuses on the network stack and leverages transitions between polling and interrupt modes as a signal to drive DVFS management. The new C6A state of AW facilitates the effective use of idle states and could make a simple race-to-halt approach [8, 161–165] more attractive than complex DVFS management techniques.

Workload-Aware Idle State Management. Various proposals exist for techniques that profile incoming request streams and use that profile information to improve power management. SleepScale [166] is a runtime power management technique that selects the most efficient C-state and DVFS setting for a given QoS constraint based on workload profiling information. WASP [167] proposes a two-level power management framework; the first level tries to steer bursty request streams to a subset of servers, such that other machines can leverage deeper, longer-latency idle states; the second level adjusts local power management decisions based on workload characteristics such as job size, arrival pattern and utilization. Similarly, CARB [16] packs requests into a subset of cores, while limiting latency degradation, so that the other cores have longer quiet times and can transition to deeper C-states. The idea of packing requests into a subset of active cores, to extend idle periods on other cores is explored by work focusing on both C-state and DVFS management [4, 31, 104]. These proposals are orthogonal to AW: while C6A can provide most of the benefits of a deep idle state at a much lower latency, advanced and workload-aware sleep management techniques can still bring extra power savings by enabling cores and/or system to enter traditional deeper, higher-latency C-states [9, 29, 168–170]. Memory power management techniques [23, 171–183] have also been proposed to reduce system energy consumption and they are complementary to our work.

9. Conclusion

To our knowledge, AgileWatts (AW) is the first deep idle core power-state architecture that directly reduces the transition latency to/from very low power states, with the goal of improving the energy efficiency of servers running latency-critical datacenter workloads. Our evaluation reveals that AW realizes power savings of up to 71% per core with <1% end-to-end performance degradation. These results support the adoption of AW in future datacenter server CPUs running latency-critical applications and calls for further research into lowering the latency of deep idle states.

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