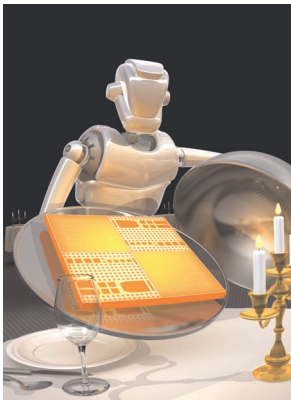


SELECTED RESEARCH FROM HOT CHIPS 24



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..... The 24th annual Hot Chips symposium was held in August 2012. As the guest editors for this special issue of *IEEE Micro*, we're pleased to introduce a selection of articles based on the best presentations from the conference program.

Hot Chips is a unique conference in all aspects. In contrast to other events that focus on academic research or marketing issues, Hot Chips focuses on technical innovations in the latest chip designs and related technologies. Companies present the chips for upcoming or recent products and discuss technical insights not easily found elsewhere. To complement the program, a select set of research groups presents prototype devices that showcase ideas ready for industrial adoption.

The 2012 program reflects three important trends in the semiconductor industry. The most pervasive trend is the widespread adoption of specialization and heterogeneity as a means for energy-efficient scaling. Ten of the 25 talks in the conference described chips with multiple types of processing engines, programmable and fixed function. The second trend is the focus on the variability challenges that arise as shrinking devices operate at low voltages in order to reduce power consumption. The final trend is the appearance of chips that take established instruction sets beyond their traditional application domains, smartphones for x86 and servers for ARM.

For this special issue, we selected five presentations that capture the first two trends and asked the authors to extend them into full articles.

Power-efficient multicore chip

In "Centip3De: A 64-Core, 3D Stacked Near-Threshold System," Ronald G. Dreslinski and his colleagues at the University of Michigan describe a prototype chip that features emerging techniques for power-efficient operation. Centip3De uses through-silicon vias for 3D integration of 128 cores with 256 Mbytes of DRAM memory.

Low-power transistor technology

In "Reducing Transistor Variability for Higher-Performance, Lower-Power Chips," Robert Rogenmoser and Lawrence T. Clark introduce deeply depleted channel (DDC) transistor technology for bulk CMOS processes. DDC technology has the potential to reduce transistor variability and achieve both power and performance gains.

Taming wide voltage ranges

In "IA-32 Processor with a Wide-Voltage-Operating Range in 32-nm CMOS," Gregory Ruhl and his colleagues at Intel discuss the design and circuit techniques necessary for chips operating in a wide voltage range. They apply these techniques to design a prototype x86 chip that operates efficiently between 280 mV and 1.2 V.

High clock frequency and new architectural features

In "IBM zEC12: The Third-Generation High-Frequency Mainframe Microprocessor," C. Kevin Shum and his colleagues at IBM present the third-generation high-frequency microprocessor for mainframe systems. The zEC12 chip operates at 5.5 GHz and features architectural innovations such as on-chip embedded DRAM caches, per-core coprocessors, and hardware support for transactional memory.

Scalable server design

In "The Oracle Sparc T5 16-Core Processor Scales to Eight Sockets," John Feehrer and his colleagues present the latest server chip from Oracle. The T5 chip includes 16 out-of-order cores and high-bandwidth links for intersocket, memory, and I/O traffic.

Space limitations prevent us from featuring more presentations in this issue. Nevertheless, the presentations from Hot Chips 24 and all previous years are available at <http://www.hotchips.org>. We encourage you to explore this exciting archive, as well as attend Hot Chips 25 this August. MICRO

Christos Kozyrakis is an associate professor of electrical engineering and computer science at Stanford University. He specializes in architectures, runtime environments, and programming models for parallel computer systems. His research focuses on improving resource efficiency in large-scale datacenters and on the design and management of energy-efficient memory and storage systems. Kozyrakis has a PhD in computer science from the University of California at Berkeley. He is a senior member of IEEE and the ACM.

Rumi Zahir leads the Intel Atom System-on-Chip (SoC) architecture team that develops low-power SoCs for handheld form factors. He was also one of the Intel Itanium Processor instruction set architects contributing to privileged instruction set, multiprocessing, memory ordering, and

interrupt architecture. Zahir has a PhD in electrical engineering from the Swiss Federal Institute of Technology in Zürich, Switzerland.

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