HOT CHIPS 26

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Welcome to the special issue of *IEEE Micro* devoted to articles about a select set of chips presented at the Hot Chips 26 conference held in August 2014. Over the years, the Hot Chips conference has been a premier venue for presenting technical details about the latest chips being built by a diverse set of companies—established leaders with a large portfolio as well as newer companies with more concentrated chip portfolios. The diversity of hot chips presented at the conference over the years, and included in the associated special issue, has provided an early look at computing trends in the industry.

The 2014 conference was packed full of presentations on a variety of chips and upcoming chip technologies. From this set, the program committee carefully selected several presentations for which we invited the authors to write a paper. The papers then went through the customary review process, and the net result was the seven articles that are included in this special issue. These articles describe chips that range from high-end servers to those customized for emerging applications. The chips that are described are excellent examples of the old English proverb: "Where there's a will, there's a way." Seemingly complex designs that were considered impractical in the initial years of the Hot Chips conference are now considered routine, practical, and desirable.

In this issue

"Sparc64 XIfx: Fujitsu's Next-Generation Processor for High-Performance Computing" by Toshio Yoshida et al. describes Fujitsu's newest high-end chip, which is intended for large supercomputer systems. The chip contains 32 regular general-purpose processing cores as well as two assistant cores that carry out select OS activity to avoid the interference (especially cache interference) that occurs when both computational and OS activity are carried out on the same core.

In "Ivy Bridge Server: A Converged Design," Irma Esmer Papazian et al. describe Intel's latest chip, which is intended for enterprise servers and high-end desktops. In particular, the article emphasizes the attention given to scalability for higher core and socket counts with a modular architecture, which enables cost-effective variants tailored to the market segments.

Targeting a different part of the server market, often called microservers, which address low-power, cost-sensitive Web hosting applications, "Intel Atom C2000 Processor Family: Power-Efficient Datacenter Processing" by Bradley Burres et al. demonstrates some impressive gains in performance per watt and integration in this space. The next-generation Silvermont core significantly advances the Atom architecture, and the integration of a wide range of USB, SATA, PCI Express, and Ethernet I/O capabilities make this a compelling play for this emerging market segment.

"M7: Oracle's Next-Generation Sparc Processor" by Kathirgamar Aingaran et al. describes Oracle's M7, a Sparc-ISA chip with 32 cores and a total of 256 hardware threads, intended for Oracle's high-end workloads. Such workloads have diverse resource demands, and the article provides a description of these demands and how the overall microarchitecture of the M7 can respond to and service these demands.

In "Denver: Nvidia's First 64-bit ARM Processor," Darrell Boggs et al. describe Nvidia's new processor microarchitecture, which

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is intended for high-end mobile devices. A key technology deployed in Denver is dynamic code optimization, and the article describes the mechanisms to support and exploit this technology.

The article "Always-on Vision Processing Unit for Mobile Applications" by Brendan Barry et al. describes the Myriad 2 processor from Movidius. Myriad 2 is intended for vision applications, a class of applications that are very important for many other technologies (such as autonomous vehicles). The article describes how several concepts in computer architecture are employed to create a low-power, high-performance chip for such applications.

Finally, in "Goldstrike 1: CoinTerra's First-Generation Cryptocurrency Mining Processor for Bitcoin," Javed Barkatullah and Timo Hanke describe an unusual application processor: a custom ASIC intended for systems that do bitcoin mining. In addition to technical challenges such as performance and energy consumption, such applications face significant time-to-market pressures: time is literally money. The article discusses how CoinTerra addressed these challenges.

Space limitations prevent us from including more articles derived from the conference presentations. Nevertheless, the presentations from Hot Chips 26 and all previous years are available at www.hotchips.org. We encourage you to explore this fascinating archive, as well as to attend Hot Chips 27 this August. MICRO

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