Guest Editors' Introduction

Emerging Memory Technologies

Yuan Xie
University of Californian, Santa Barbara

Yishen Zhao
University of California, San Diego

Technology scaling of traditional memory technologies, such as SRAM and DRAM, is increasingly constrained by fundamental technology limits. The recent research progress of various emerging memory device technologies, such as three-dimensional integrated memory, phase-change RAM, spin-transfer-torque magnetoresistive RAM, and resistive RAM, has drawn tremendous attentions from both academy and industry. These technologies bring many research opportunities and challenges for novel architectures, systems, applications, design tools, compilers, and programming models and languages. As these emerging memory technologies are maturing, it is important for us to understand their pros and cons for improving the performance, power, reliability, and scalability of future computer systems.

To better understand the opportunities, challenges, and experiences that are driving the emerging memory technology research, this special issue includes six invited position statements from a group of memory system and architecture experts (see the "Expert Opinion" column). The experts point to promising workload domains, including deep neural networks (Yiran Chen and Egin Ipek), high-performance computing (Yan Solihin), and storage systems (Sam H. Noh and Steven Swanson). Multiple statements argue for rethinking the memory and storage hierarchy organizations to unlock of full potential of emerging memory technologies (Moin Qureshi; Sam; Yiran). Most experts also point out the challenges of software support and new program abstractions (Sam; Steven; Yan) that are required to ease the adoption of emerging memory technologies.

This special issue also features two peer-reviewed articles and three invited papers that address various aspects of architecture and system research problems with emerging memory technologies.

In "Performance Assessment of Emerging Memories Through FPGA Emulation," Maya Gokhale, Abhishek Jain, and Scott Lloyd investigate performance of parallel applications on CPUs whose main memories sweep over a wide range of latencies within a bandwidth cap by employing an FPGA emulator. The experimental study highlights the performance impact of higher latency on concurrent applications and identifies conditions under which future high-latency memories can effectively be used as main memory.

Mimi Xie and her colleagues from the University of Pittsburgh, Tsinghua University, and City University of Hong Kong present "A Novel STT-RAM-Based Hybrid Cache for Intermittently Powered Processors in IoT Devices." This paper describes a STT-RAM-based hybrid cache tailored for intermittently powered IoT systems.

Yeseong Kim, Mohsen Imani, and Rosing, Tajana present "Image Recognition Accelerator Design Using In-Memory Processing." This paper describes a hardware accelerator design that processes object recognition tasks inside emerging nonvolatile memory. The proposed design accelerates key subtasks of image recognition, including text, face, pedestrian, and vehicle recognition.

Digital Object Identifier 10.1109/MM.2019.2892165
Date of current version 21 February 2019.

Published by the IEEE Computer Society

In "CONCEPT: A Column Oriented Memory Controller for Efficient Memory and PIM Operations in RRAM," Nishil Talati and his colleagues from Technion Israel Institute of Technology and Stanford University present a memory controller design optimized to exploit unique properties of RRAM to enhance its performance and energy efficiency as well as exploiting RRAM's processing-in-memory capability.

Pengfei Zuo and his colleagues from Huazhong University of Science and Technology present "Write Deduplication and Hash Mode Encryption for Secure Non-Volatile Main Memory." This paper proposes a line-level write reduction technique to enhance the endurance and performance of secure nonvolatile main memory systems.

It is our hope that this special issue provides a broad perspective on the research efforts and visions with emerging memory technologies, and encourages future research efforts on realizing the full potential of these technologies.

We would like to thank all those who submitted manuscripts to this special issue and all the reviewers who helped us to select the articles. Many thanks to the authors of the "Expert Opinion" column for their valuable perspectives on this topic. Finally, a special thanks to Lieven Eeckhout and Lizy John for their guidance throughout the process.

Yuan Xie is a Professor at the University of California, Santa Barbara. Contact him at yuanxie@ece.ucsb.edu.

Jishen Zhao is an Assistant Professor at the University of California, San Diego. Contact her at jzhao@ucsd.edu.