Column: From the Editor-in-Chief

Secure Architectures

Lizy Kurian John
The University of Texas at Austin

Welcome to the July/August 2019 issue of *IEEE Micro*, which presents to you a selection of articles on secure architectures and a few articles on other topics.

Computer security is becoming increasingly important due to the increased use of computers and the internet in our day-to-day lives. Attacks on computer systems are becoming very commonplace. Many recent attacks demonstrated security vulnerabilities in commodity hardware, pointing to the importance of secure hardware architectures. This special issue presents four articles on secure computer architectures. The topics discussed range from defense against cache timing channel attacks to asserting security properties of a processor at runtime.

This special issue presents four articles on secure computer architectures. The topics discussed range from defense against cache timing channel attacks to asserting security properties of a processor at runtime.

Prof. Simha Sethumadhavan of Columbia University and Prof. Mohit Tiwari of the University of Texas at Austin served as guest editors for the special issue. A comprehensive article written by Professors Sethumadhavan and Tiwari serves as an excellent introduction to the compendium on secure architectures.

The four articles from the secure architecture theme are accompanied very appropriately by a Micro Economics column related to computer security by Shane Greenstein. In the article titled "The Aftermath of the Dyn DDOS Attack," Greenstein writes about the October 2016 series of distributed denial-of-service (DDOS) attacks causing many services and platforms to be unavailable for large segments of users in North America and Europe. The attacker targeted systems operated by the nameserver resolution provider Dyn, who performs approximately 10% of the nameserver services in the United States. Since nameserver resolution is essential for many businesses to operate, the attack affected a range of businesses including Netflix, CNBC, Twitter, Airbnb, and Etsy. Greenstein provides details on the market share of domain name system providers and alerts the readers to an important vulnerability in today's internet, viz. many internet services are concentrated in a few providers. His article draws attention to the lack of redundancy in internet service providers.

In addition to the special issue articles on computer security, there are two other articles in this issue. The first one, "RASSA: Resistive Pre-Alignment Accelerator for Approximate DNA Long Read Mapping" by Kaplan *et al.*, presents an in-memory parallel architecture for similarity search for genomic sequences. As personalized medicine based on gene mapping is emerging, hardware architectures to support sequence searches are increasingly relevant. One challenge in mapping long sequences is determining the optimal mapping location of every

Digital Object Identifier 10.1109/MM.2019.2924711
Date of current version 23 July 2019.

Published by the IEEE Computer Society

read on to the reference sequence. In this article, Kaplan *et al.* present hardware acceleration of genomic mapping by using resistive memories (memristors) which are elements that store information by modulating the resistance of the nanoscale storage elements. Memristor arrays facilitate simultaneous compare and mapping and result in a highly parallel compute accelerator.

The second regular channel article is "The Queuing-First Approach for Tail Management of Interactive Services" by Mirhosseini and Wenisch. Cloud services are increasingly becoming popular, however, service latencies in the cloud are heavy-tailed. Some requests can take 100 times more time than the average. This article presents two solutions to mitigate this important problem, server pooling, and common-case service acceleration.

I am also proud to write about a new Best Paper award for *IEEE Micro*. Starting this year, the best paper award will be given for articles published in *IEEE Micro*. IEEE Computer Society has recently started a best paper award program to acknowledge and reward the best articles in each of the Transactions and Magazines sponsored by the Computer Society. Articles based on a conference paper are ineligible and hence the MICRO TopPicks articles would be ineligible for this award. The intent of the award is to recognize outstanding regular papers. The first award will be announced in a couple of months.

IEEE Micro is interested in submissions on any aspect of chip/system design or architecture.

Please consider submitting articles to *IEEE Micro* and remember, all regular articles will be eligible for the best paper award.

Hope you enjoy the secure architectures as well as other articles presented in this issue. Happy reading!

Lizy Kurian John is a Cullen Trust for Higher Education Endowed Professor with the Electrical and Computer Engineering Department, the University of Texas at Austin, Austin, TX, USA. Contact her at ljohn@ece.utexas.edu.