From the Memory Lane! Microprocessor Stories From Deep Within!

Lizy Kurian John, *The University of Texas at Austin, Austin, 78712, TX, USA*

Many of our readers wrote passionately about their memories on topics ranging from the coolest microprocessor feature to their personal journeys through these eventful decades. These entries were solicited using a Call for Contributions on the *IEEE Micro* website and by announcements during a panel at the International Symposium on Computer Architecture (ISCA) 2021. We received many entries from experienced designers to passionate users of microprocessors.

In this article, memories from Linley Gwennap (Editor-in-Chief of *Microprocessor Report*), Kathy Papermaster (IBM veteran of 26 years), Kunle Olukuton (Stanford Professor), Kathryn McKinley (Google Principal Research Scientist), and Timothy Pinkston (University of Southern California Professor) are presented.

What I Learned From the DEC Alpha 21164

Linley Gwennap, Microprocessor Report

In 1996, we celebrated the 25th anniversary of the microprocessor, and the coolest processor was the Alpha 21164 from Digital Equipment Corporation (DEC). Alpha was one of the new-fangled RISC architectures of the day, back when RISC versus CISC was a big deal. It was the fastest processor on the planet, and not by a little: at an incredible 500 MHz, it blazed at more than twice the speed of any competing CPU. This speed wasn't just for show, as the 21164 led the industry on benchmarks such as SPECint95 as well. Like a Lamborghini with gullwing doors, it had all the processor geeks drooling.

But like that Lamborghini, the Alpha processor wasn't particularly practical. The high clock speed made interfacing with the rest of the system difficult, and the chip required extra cooling as well. DEC charged a premium price for its powerful processor, restricting it to high-end systems. The software ecosystem was also quite limited; in those pre-Linux days, the DEC Alpha systems ran a proprietary Unix OS. Microsoft released Windows NT on Alpha, along with MIPS and PowerPC, but few software vendors ported their applications to the RISC architecture. Even after DEC cut Alpha prices in half, it attracted little interest. In 1998, Compaq acquired DEC and quickly killed the Alpha line. As a young processor geek, I thought the 21164 would quickly take over the microprocessor industry, given its superb design and amazing performance. But after seeing what happened to Alpha, I realized there is more to a processor than speed; system design, price, and particularly software support are essential components to success. Since then, I've heard many companies promise to deliver 2x better performance, but few delivered, and even fewer put together a complete package to challenge the market leaders. That's why Arm, Intel, and NVIDIA are so hard to knock off their lofty perches.

LINLEY GWENNAP was the President of The Linley Group and principal analyst, focusing on processors for servers, mobile, and deep learning. He is publisher and Editor-in-Chief of *Microprocessor Report*, a technical newsletter covering the semiconductor industry.

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Memories on Early Adoption of Design Automation Tools and More

Kathy Papermaster, IBM

My favorite microprocessor to work on was the PowerPC 604 (and its derivatives), which was one of the PowerPC processors jointly developed by IBM and Motorola for Apple and IBM systems in the 1990s. There were 300 engineers from both companies in a brand-new building working on the 603, 604, and 620 processors. We started from scratch, creating a design methodology using both IBM and vendor tools that was specific for the PowerPC chips. The design data went to both IBM and Motorola fabs. I was the integration lead for the 604 derivatives in a team of about 100 people. Nothing beat the thrill of working with my small integration team taping out (sending the design to the fab) in the middle of the night on schedule! In addition to working intensely, the management team did a great job recognizing the teams with fun social events to break up the rigor of the schedule.

My most memorable project was the Cell processor that was designed by Sony, Toshiba, and IBM for the Playstation 3. By then, I had been in management a while and was the director for the final three years of the project. Working alongside Japanese engineers on assignment in Austin was a unique experience. In addition to the technology challenges, we had cultural differences. At executive program reviews, extensive time and thought was done to make sure the messaging was not misinterpreted due to language differences. I also had the honor of taking the project end of life and ensuring all contractual obligations were met. Overall, this was a very unique and memorable experience.

I would like to add that the evolution of the processor could never happen without the innovation in fabrication technology and design automation throughout the years. When I first started with IBM's General Technology Division in Burlington, VT, in 1983, the huge advancement was the launch of CMOS! Design tools for IBM designs were done in-house, and I loved being an early adopter to help find flaws in the tools to make them better. I will never forget my manager asking me why I was using a tool when it was much faster to write the test code by hand! Without early adopters and someone to work with the tool developers in a noncontroversial manner, we'd never be where we are today.

KATHY PAPERMASTER was with IBM for 26 years. She held many research and development leadership roles that culminated in an executive role driving the delivery of the Cell processor for Playstation 3.

Coolest Thing That Happened in the History of the Microprocessor: Alpha 21364's Integration of an On-Chip Router

Timothy Mark Pinkston, University of Southern California

The integration of a fully functional router on the Alpha 21364 (EV7) microprocessor chip for supporting high-performance, scalable, and reliable communication in NUMA-based multiprocessor systems (such as HP's Marvel family of AlphaServer systems) was really cool and, in many ways, precedent setting. The EV7 network architecture was remarkably robust and cutting-edge, scalable to up to 128-processor configurations. It featured competitively low-latency (pin-to-pin) and high-bandwidth (peak and sustained) packet transport, both of which were superior to contemporaneous off-chip routers. It did so with a fully pipelined router implementation that allowed the router to operate at the processor core's clock speed and with virtual

cut-through adaptive routing along minimal paths of a 2-D torus network topology that allowed bypassing of network hot-spots and congestion mitigation. It provided support for directory-based cache coherence and network deadlock avoidance by implementing separate virtual channels for different coherence protocol packet classes and its routing algorithm logical networks. It also provided reliability and fault tolerance support with SECDED error recovery and first-hop misrouting, to circumvent error-prone or broken interconnection network links. As one of the first—if not the first—microprocessor designs to integrate a fully functional on-chip router, the EV7 helped to usher in the era of on-chip networks (also known as, networks-on-chip or NoCs) for supporting efficient data movement in multicore/manycore processor chips that soon followed and, now, are prevalent across diverse computing systems.

TIMOTHY MARK PINKSTON is a George Pfleger Chair in electrical and computer engineering, and a Professor of electrical and computer engineering with the University of Southern California.

Sun Niagara 1 (UltraSPARC T1)—A Special Processor for Me

Kunle Olukotun, Stanford University

I was an early proponent of exploiting thread-level parallelism (TLP) on-chip using chip multiprocessor (CMP) architectures. In the mid-1990s, the Stanford Hydra research project was initiated to investigate the design of CMPs. This project bucked the prevailing microprocessor design direction of speeding up a single thread by exploiting ILP using complex out-of-order execution techniques. A seminal 1996 paper, "The Case for a Single-Chip Multiprocessor," explained the performance and cost advantages of CMPs, but there were many who were still skeptical about the viability of the CMP approach. In 2000, Afara WebSystems was founded to commercialize the ideas developed under the Hydra project. The goal was to design a power-efficient, high-performance microprocessor called Niagara 1 for throughput-orientated commercial server applications such as web servers, application servers, and database servers. This is known as high-throughput server computing design. Server applications are characterized by lots of threads, low ILP, and huge memory footprints. The Afara microprocessor design took the Hydra CMP design philosophy to the extreme to match these application characteristics: focus on TLP at the expense of ILP.

Niagara 1 has eight, in-order, single-issue CPU cores each of which supports four threads for a total of 32 hardware threads sharing a 3-MB secondary cache on a single chip. Coupled to the compute resources are enough directly connected DRAM memory channels to satisfy the high memory bandwidth requirements of highly threaded commercial applications. Afara WebSystems was acquired by Sun Microsystems and Niagara 1 microprocessor was officially released as the UltraSPARC T1 in 2005. Niagara-based systems achieved significant (factor of 3–5x) performance gains on server applications compared to systems powered by contemporary microprocessors and the performance per watt improvements were even more impressive (factor of 5–8x). David Patterson of the University of California Berkeley calls Niagara 1 a "landmark chip" as it represents a radical departure from contemporary server-processor design. The architecture ideas that were developed in the Niagara 1 design have led to eight generations of throughput-oriented microprocessors that were designed initially at Sun and later at Oracle.

KUNLE OLUKOTUN is the Cadence Design Systems Professor with the School of Engineering and Professor of Electrical Engineering and Computer Science at Stanford University. He founded Afara Websystems to develop high-throughput, low-power multicore processors for server systems. The Afara multicore processor, called Niagara, was acquired by Sun Microsystems.

A Primitive Batch Queuing System

Kathryn McKinley, Google

As an undergraduate at Rice University, we used a VAX for the advanced programming, compiler, and OS classes before the series added virtual memory. In the lab, the students invented the "coke can" batch queuing system, where we kept a sign up, and then when it was your turn, you put a coke can (three was the maximum, if memory serves me right) on your desktop and then could compile and run your program. This system kept the machine from exhausting its physical memory and crashing. The Rice honor system at work. My current favorite is RISC-V Rocket, as I look to the future of microprocessor innovation.

KATHRYN MCKINLEY is a principal Research Scientist at Google. She was on the faculty at the University of Texas from 2001 to 2013. McKinley received a Ph.D. degree from Rice University.

These articles provide additional insight into the engineering challenges, team dynamics, stiff competition, personal aspirations, shattered ambitions, and other perspectives that are often not widely reported.

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