FROM THE EDITOR-IN-CHIEF

Special Issue on Cool Chips and Hot Interconnects

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Welcome to the March/April issue of *IEEE Micro* for 2022! This special issue brings to *IEEE Micro's* readership the best from two interesting conferences—Cool Chips 2021 and Hot Interconnects 2021. Cool Chips is a conference that focuses on the research on state-of-the-art low-power, high-speed chips and challenges facing researchers to simultaneously achieve low power consumption and high chip performance. The past couple of years have seen a flurry of research in low-power high-speed chips in artificial intelligence (AI), Internet of Things (IoT), consumer electronics, etc., and several of these were presented at the Cool Chips conference. Three selected papers from Cool Chips are presented in this issue.

This special issue also presents a collection of articles on interconnect technologies based on the Hot Interconnect Conference of August 2021. Hot Interconnects is a conference that brings to light state of the art in interconnect technology. In modern systems on chip and large-scale computer systems, many processing components are being interconnected and the larger system's performance and energy consumption significantly depends on the interconnect. Five selected articles from Hot Interconnects are presented in this issue.

Under the Cool Chips theme, the presented articles are on CNN acceleration describing quantization with a learnable parameter soft-clipping, on DNN training focusing on bit-sliced level fine-grained sparsity, and the Fugaku Supercomputer from Japan which has 158,976 nodes with 7.6 million cores on an architecture designed by Riken and Fujitsu based on the Armv8 instruction set. Special issue guest editors Makoto Ikeda and Fumio Arakawa of the University of Tokyo have written an introduction to the Cool Chips special theme that discusses the three articles that were selected from the Cool Chips conference.

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Under the Hot Interconnects theme, the presented articles are on low-latency low-power PCI Express 6.0 PHY; the Intel PIUMA system that allows logical collective topologies to be directly embedded into the network and support pipelined embeddings for high throughput computation; offloading DL training phases on the latest Nvidia Bluefield-2 DPUs, which combine the capabilities of traditional application-specific integrated-circuit (ASIC)-based network adapters with an array of ARM processors; an adaptive nonminimal hop-by-hop mechanism called the polarized routing algorithm; and accelerating deep learning on multi-GPU systems by awareness of intra-node interconnects, such as NVLink and PCIe. Special issue guest editors Sayan Ghosh of Pacific Northwest National Laboratory, Ryan E. Grant of Queen's University (Canada), and Min Si of Meta have written an introduction to the Hot Interconnects theme and provide a preview of the five articles.

THIS SPECIAL ISSUE BRINGS TO IEEE MICRO'S *READERSHIP THE BEST FROM TWO INTERESTING CONFERENCES—COOL CHIPS 2021 AND HOT INTERCONNECTS 2021.*

I would like to express my special gratitude to guest editors Ikeda and Arakawa of Cool Chips, and Ghosh, Grant, and Si of Hot Interconnects, who worked hard on identifying the top papers from the respective conferences and took them through a rigorous review/revision process, which resulted in the excellent articles that you are presented with.

The eight articles from the Cool Chips and Hot Interconnects themes are accompanied by a Micro Law article from Joshua Yi and a Micro Economics column by Shane Greenstein. In the Micro Law article, "Review of Patents Issued to Computer Architecture Companies in 2021," Joshua Yi analyzes the patents that were issued to 18 computer architecture companies in 2021. Yi also compares the

distribution of those patents across different patent classes. In addition, Yi highlights one patent from each company that may be particularly notable. Due to the length of the article, it is broken into two parts, and the first part is presented in this issue. The second part can be expected in the next issue.

COOL CHIPS AND HOT INTERCONNECTS ARE HELPING THE WORLD TO CARRY ON BUSINESS THROUGH THE ONGOING PANDEMIC. ENJOY THESE ARTICLES!

In the Micro Economics article, "Time for a Change in U.S. Antitrust for Technology?," Shane Greenstein discusses the basic principles behind the current U.S. antitrust policies, and their strengths and weaknesses. He describes some of the events surrounding the Microsoft antitrust case to hint at the course of events for the ongoing Alphabet case.

Readers of *IEEE Micro* will continue to get articles on emerging chip technologies and architectures as we go into 2022. This issue will be followed by the Special Issue on Hot Chips in May/June. The subsequent special issue themes will be top picks from architecture conferences, compiling for accelerators, AI on the edge, and environmentally sustainable computing. Please check out the Call for Papers for the upcoming Special Issue on Environmentally Sustainable Computing at https://www.computer.org/digital-library/magazines/mi/call-for-papers-special-issue-on-environmentally-sustainable-computing.

In addition to the special issue articles, *IEEE Micro* is always interested in submissions on any aspect of chip/system design or architecture. Please consider submitting articles to *IEEE Micro* and remember, these articles are eligible for the Best Paper Award, which will be given annually.

Cool Chips and Hot Interconnects are helping the world to carry on business through the ongoing pandemic. Enjoy these articles!

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