Special Issue on Hot Interconnects 29

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Welcome to the *IEEE Micro* Special Issue dedicated to the 29th IEEE Hot Interconnects Symposium (Hot Interconnects 29). Each year Hot Interconnects presents cutting-edge research from industry and academia on the design and implementation of high-performance interconnects. The program of this year's symposium included invited speakers, panels, tutorials, and peer-reviewer article.

The theme of this year's symposium was: disaggregation leading to reaggregation. Recent technology trends offer the opportunity to rethink current approaches to system architecture. Processors, storage, memory, interconnects, and accelerators have traditionally been considered as monolithic systems. However, new and emerging technologies make it possible to evaluate opportunities to organize these resources as modular components, fostering novel ways of designing new architectures by recombining resource modules for new benefits. The program included a panel on this theme and invited speakers from Ayar Labs, Blue Cheetah Analog Design, HPE, Intel, IBM, and NVIDIA.

Each day of the symposium featured a keynote speaker. The first day's keynote, titled "The Evolution of Interconnects in the Brave New Quantum World!," was presented by Andrew Lord, a Senior Manager of Optical Research from BT. He discussed the challenges of building a new, commercial quantum network. The second day's keynote, titled "Wait, How Many Networks Did I Just Cross? Interconnects, Accelerators, and Disaggregation at TACC," was presented by Dan Stanzione, the Executive Director of the Texas Advanced Computing Center (TACC). He discussed experiences with disaggregation at TACC and how new and emerging interconnect technologies might affect the future of disaggregation.

Our program also included articles peer-reviewed by the members of our Program Committee. This special issue features extended versions of four of the best articles presented at this year's symposium.

In the first article in this special issue [A1], Das Sharma describes the design and operation of CXL 3.0. The article includes a representative microarchitecture implementing the standard and an analysis of the realizable bandwidth for the three supported CXL protocols (CXL.io, CXL.mem, and CXL.cache).

EACH YEAR HOT INTERCONNECTS PRESENTS CUTTING-EDGE RESEARCH FROM INDUSTRY AND ACADEMIA ON THE DESIGN AND IMPLEMENTATION OF HIGH-PERFORMANCE INTERCONNECTS.

In the second article in this special issue [A2], Xin et al. present a design of an updateable field-programmable gate array (FPGA)-based packet classifier. By using a multicore architecture instead of a traditional pipeline architecture, the authors show that their approach is able to support dynamic rule updates while still achieving high classification throughput and low classification latency.

In the third article in this special issue [A3], Cascajo et al. propose a lightweight platform monitoring tool (LIMITLESS) for gathering dynamic information about congestion within InfiniBand networks. The availability of this information enables the congestion response of the InfiniBand network to be tuned based on where the congestion originated.

In the fourth article in this special issue [A4], Suresh et al. leverage the scatter–gather functionality of InfiniBand host channel adapters to enable noncontiguous transfers from graphics processing unit (GPU) memory without requiring the use of kernels to pack or unpack the data. Using microbenchmarks and computational workloads, they show that their approach outperforms existing state-of-the-art GPU-aware message passing interface libraries that rely on pack and unpack kernels.

In addition to the four articles published in this special issue, the entire proceedings of the symposium are available in IEEE Xplore (https://ieeexplore.ieee.org/xpl/conhome/9912439/proceeding). Video recordings of many of the sessions are also available on the Hot Interconnects YouTube channel (https://www.youtube.com/@hoti-hotinterconnectssympo5358).

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Additional details on this and future symposia are available at: http://www.hoti.org.

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APPENDIX: RELATED ARTICLES

[A1] D. D. Sharma, "Compute Express Link (CXL): Enabling heterogeneous data-centric computing with heterogeneous memory hierarchy," *IEEE Micro*, vol. 43, no. 2, pp. 99–109, Mar./Apr. 2023, doi: 10.1109/MM.2022.3228561.

[A2] Y. Zin, W. Li, G. Xie, Y. Xu, and Y. Peng, "A parallel and updatable architecture for FPGA-based packet classification with large-scale rule sets," *IEEE Micro*, vol. 43, no. 2, pp. 110–119, Mar./Apr. 2023, doi: 10.1109/MM.2023.3238012.

[A3] A. Cascajo et al., "Monitoring InfiniBand networks to react efficiently to congestion," *IEEE Micro*, vol. 43, no. 2, pp. 120–130, Mar./Apr. 2023, doi: 10.1109/MM.2023.3241840.

[A4] K.K. Suresh et al., "Network-assisted noncontiguous transfers for GPU-aware MPI libraries," *IEEE Micro*, vol. 43, no. 2, pp. 131–139, Mar./Apr. 2023, doi: 10.1109/MM.2023.3241133.

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