A Bipolar Output Voltage Pulse Transformer Boost Converter with Charge Pump Assisted Shunt Regulator for Thermoelectric Energy Harvesting

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***Abstract*—This work first generates ±1 V output via the self-startup pulse transformer boost converter. Another on-chip single-stage voltage tripler then generates 3 V output from the extra output power of boost converter, which is shunted otherwise. Higher voltage headroom is instrumental for sensor, analog and RF circuits. Charge pump clock frequency is adaptively tracking the input voltage, which is sensed using power-saving time-domain digital technique. Based on a standard CMOS 0.13-µm technology, chip measurement verified the standalone boost converter and simulation confirmed the overall system operations. The system requires minimum startup input voltage of 36 mV and input power of 5.8 µW.**

Keywords—Bipolar output; boost converter; charge pump; CMOS energy harvesting; transformer

I. INTRODUCTION

Thermoelectric energy harvesting is interesting due to the omnipresence and continuous operation that is time independent. The output voltage of thermoelectric generator (TEG) is in proportion to the temperature difference between its two junctions. Typically TEG is modelled as ideal voltage source (V_{TEG}) with fixed source resistance (R_{TEG}). State-of-the-art thin-film TEG [1] has much smaller area size than conventional TEGs [2][3]. Besides being compact, thin-film TEG also allows higher power to be generated per device area, which enables further miniaturization of the entire system size. Despite the newer TEG has higher output voltage than conventional TEGs, the internal resistance is higher (400 ohms vs. less than 10 ohms) and smaller output current as trade-offs. Performances of different TEGs are summarized in Table I.

TABLE I. COMPARISONS OF DIFFERENT TEGS AT ΔT=10°C

TEG type	V_{oc}	I_{sc}	P_{match_load}	Device Area	Power/Area
Micropelt MPG-D751 [1]	1.68V	3.74mA	1.42mW	4.2mm x 3.3mm	102.5µW/mm^2
Tellurex G2-30-0313 [2]	0.22V	29mA	1.58mW	30mm x 30mm	1.75µW/mm^2
Marlow Technology TG12-2.5 [3]	0.55V	83mA	11.4mW	30mm x 30mm	12.67µW/mm^2

Recent works [4][5] designed for low voltage TEG using miniature transformers have minimum self-startup input voltage down to 20 mV, but the high input current requirement is not suitable for high R_{TEG} TEG such as [1]. To reduce the minimum input current, [6] proposes a 1:1 pulse transformer instead of high turns-ratio (at least 1:50) transformers required by [4][5]. This work modified the topology of [6] as first stage converter to harvest TEG power. The output voltage is regulated at ±1 V using shunt regulator. While 1 V output is sufficient for low power, supply voltage insensitive digital circuits, sensitive circuits such as external sensors, ADC and RF transceivers in wireless sensor network (WSN) applications, additional voltage headroom is desired for better linearity, gain and resolution [7]. Installing another inductor boost converter in addition to existing transformer-based boost converter not only increases cost, but also has potential electromagnetic interference (EMI) due to the presence of multiple inductors. Since charge pump can be fully integrated on-chip and has no EMI issue, this paper explores cross-coupled charge pump topology to extract extra power from the first stage storage capacitor. By applying bipolar (±1 V) clock pulses to drive the charge pump; 3 V output can be generated. To optimize the charge extraction capability, the charge pump clock frequency is designed to track the input voltage. TEG output power can be determined by measuring the turn-on period of the self-running boost converter, using digital static logic cells only, avoiding power hungry voltage domain ADC. Minimal overhead power is required by the sensing and control circuits since a time-domain fully digital approach is employed. With leakage suppression technique, digital static logic can be scaled, with V_{DD} down to 62 mV [8].

This paper is organized as follows. The proposed system architecture is first explained in Section II. Section III elaborates the principle of bipolar output pulse transformer boost converter and shunt regulator. In Section IV the voltage tripler charge pump and the negative voltage enhanced clock driver is explained. Measurement and simulation results using a standard CMOS 0.13-µm technology are then presented in Section V. Finally Section VI concludes this paper.

II. SYSTEM ARCHITECTURE AND OPERATIONS

The proposed system architecture is shown in Fig. 1. Incoming power from TEG will first power up the bipolar output pulse transformer boost converter and generates ±1V, which will be stored in C_{POS} and C_{NEG} respectively. Once V_{DD}

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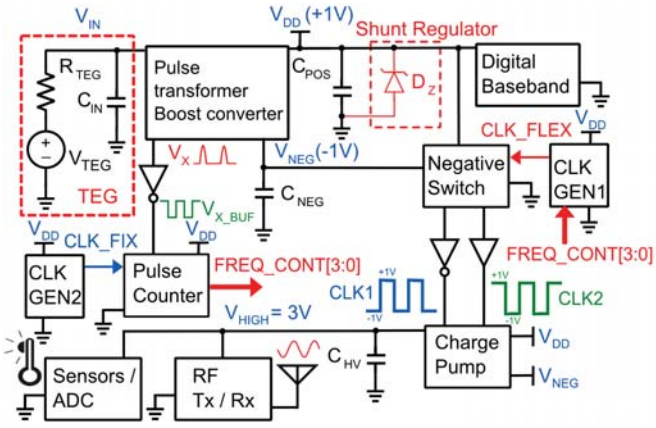

Fig. 1. Proposed system architecture to power a wireless sensor node

reaches 1 V, the secondary charge pump will be activated. Both on-chip clock sources (CLK_FIX and CLK_FLEX) are designed based on current-starved inverter-based ring oscillator. Using inverter and negative level shifter switch driver, CLK_FLEX will be converted into two complementary phase bipolar clock pulses (CLK1 and CLK2), which swing between +1 V and –1 V. These clocks will drive a conventional cross-coupled pair charge pump (will be shown in Section IV). Due to the enhanced voltage swing, the charge pump circuit becomes a voltage tripler instead of the usual voltage doubler. To sense the input voltage, conventional approach requires voltage domain analog-to-digital-converter (ADC), which consumes significant amount of power. Since the turn-on period of boost converter varies based on input voltage (will be further explained in Section III), a pulse counter driven by a fixed frequency clock (CLK_FIX) will measure this duration to determine the input voltage indirectly. A 4-bit digital control word (FREQ_CONT) will represent the duration measured.

When input voltage becomes higher, charge pump will be driven at a higher clock rate, in order to accelerate charge extraction rate. The charge pump is only activated during turn-on period of boost converter cycle (V_X node of boost converter becomes high) to avoid loading down storage capacitor C_{POS} at idle state. Based on the detected V_X turn-on period, clock frequency (CLK_FLEX) driving the charge pump will be hopping between 100 kHz and 800 kHz, within 16 different clock rates, adjusted by the 4-bit FREQ_CONT digital code.

III. Bipolar Output Voltage Pulse Transformer Boost Converter with Shunt Regulator

The boost converter used in this work is shown in Fig. 2. The origin of this circuit is motivated and derived from a single stage Meat Grinder [9] where Meat Grinder is an inductive energy transfer circuit which is used to supply high-current pulsed power applications such as electromagnetic propulsion, using coupled inductors of 1:1 turn ratio. Circuit dynamics of this circuit is shown in Fig. 3. When a TEG is connected to the V_{IN} terminal, current first flows through inductor branch L_0, establishing biasing voltage across N_{BOOST} gate. Positive V_G will turn on transistor N_{BOOST} and allows drain current I_{L1} to flow through secondary inductor L_1. The secondary inductor current I_{L1} rising rate is determined by the $(V_{IN}-V_X)/L_1$ ratio.

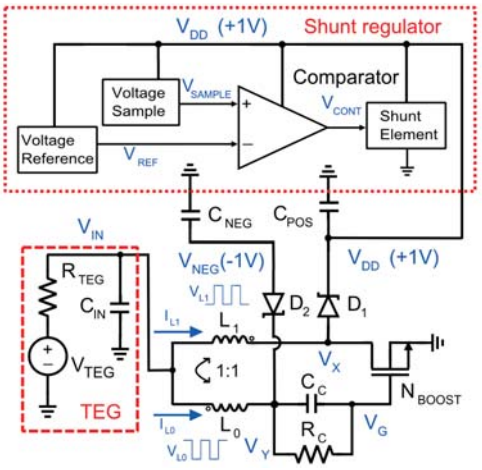

Fig. 2. Bipolar output voltage pulse transformer boost converter circuit with shunt regulator

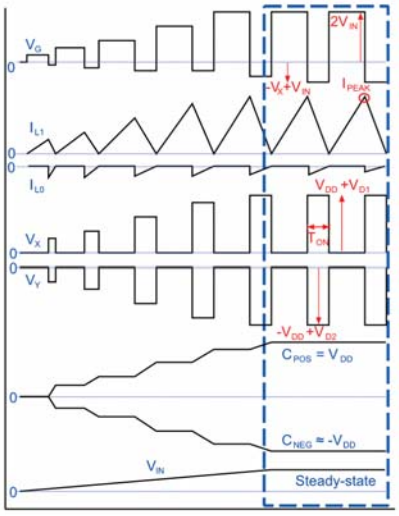

Fig. 3. Conceptual startup waveforms of bipolar output voltage pulse transformer boost converter with output regulated by shunt regulator

I_{L1} current will continue to rise until the transistor N_{BOOST} becomes completely saturated ($I_{PEAK}=I_{DSAT}$), at this point, drain current of N_{BOOST} no longer increases and a voltage pulse V_X is induced across secondary inductor L_1 due to this change. V_X goes up and this marks the beginning of turn-on period (T_{ON}). When V_X raises, inductor current I_{L1} will be in decreasing trend. I_{L1} flows through diode D_1 and goes into C_{POS}. Since L_0 and L_1 is mutually coupled and has identical inductance, similar voltage at the opposite polarity is induced across L_0. This negative voltage is then reflected on N_{BOOST} gate, which will turn off N_{BOOST} and effectively suppresses N_{BOOST} off-state leakage current. Negative voltage generated across L_0 is also stored on C_{NEG}, with V_{NEG} tracking V_{DD} closely. T_{ON} ends when I_{L1} reaches zero. At this point, all energy previously stored in L_1 ($0.5I_{PEAK}^2L_1$) is now transferred to C_{POS} and C_{NEG}. At this point the boost conversion cycle repeats itself again.

It can be shown that T_{ON} is governed by the formula:

$$T_{ON} = \frac{I_{PEAK}\, L_1}{V_{DD} + V_{D1} - V_{IN}} \quad (1)$$

Based on (1), whenever input voltage V_{IN} increases (indicating more input power), the duration of T_{ON} will also increase. Using this property, we can determine the input voltage (power) by just measuring the duration of T_{ON}.

Without the presence of shunt regulator, this boost converter will continue to increase V_{DD} as input voltage increases. This scenario is potentially deleterious as V_{DD} generated might exceed the breakdown voltage of transistor N_{BOOST}. Since the nominal voltage of CMOS 0.13-µm process is 1.2 V, a shunt regulator with output voltage of 1 V (to allow some safety margin), is designed based on the circuit blocks shown in Fig. 2. The key element is a temperature and supply invariant voltage reference, which can be realized either using bandgap reference [10] or threshold voltage difference [11].

IV. Cross Coupled Voltage Tripler Charge Pump and Bipolar Clock Driver

Conventional cross-coupled pair charge pump [12] used is shown in Fig. 4(a). N_A and N_B are thick oxide triple-well NMOS (bulk nodes tied to V_{NEG}), P_A and P_B are thick oxide PMOS (laid in separate N-wells and bulk nodes tied to V_{HIGH}), pumping capacitors C_1 and C_2 are 5 pF. Charge pump output voltage (V_{HIGH}) across secondary storage capacitor C_{HV} at no-load condition is 3 V. Recent works [13] implemented this topology using CMOS 0.18-µm process, showing 77% efficiency when converting 0.9 V to 1.7 V. Moreover, with adaptive dead-time technique proposed by [14], such charge pump topologies is shown to be compatible with supply voltage down to 0.15 V. Using negative voltage ($-V_{DD}$) instead of ground (0 V) to drive the bottom supply rail of charge pump, the output voltage level can be further increased [15]. Since the boost converter at earlier stage already generated the negative supply required, no extra auxiliary charge pump is necessary to generate negative voltage, which is usually necessary as shown in [14][16]. The unipolar clock generated on-chip needs to be converted to bipolar voltage level. To perform the necessary level shifting i.e. from (0V↔1V) to (-1V↔+1V), a bootstrapping negative switch driver [16] is used in this work; where the topology is shown in Fig. 4(b).

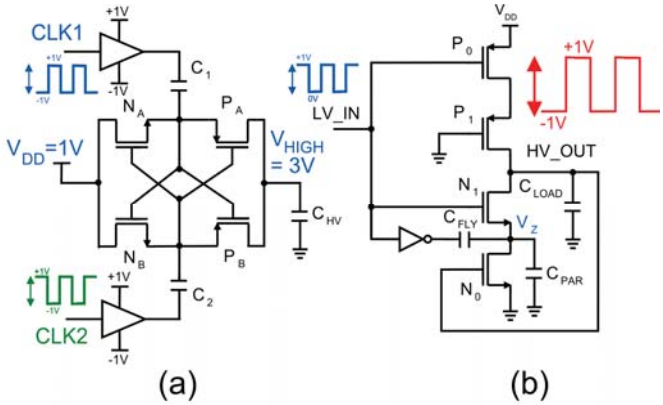

Fig. 4. (a) Cross-coupled charge pump (b) bootstrapping negative switch

P_0, P_1 and N_1 form a CMOS inverter to switch the output node HV_OUT. C_{FLY} is the bootstrapping capacitor and N_0 is the pre-charge transistor. N_1 and N_2 are triple-well NMOS transistors and are isolated from other NMOS transistors since their bulk node (tied to V_Z) is unstable during transient operation. Parasitic capacitance C_{PAR} is formed between the P-well and deep N-well. C_{LOAD} is the load capacitance seen by the output node HV_OUT. The proper C_{FLY} value (pF range) must be selected in order to achieve the required voltage level. Cascode transistor P_1 with gate shorted to ground will reduce the V_{GD} overstress of P_0. The node voltage V_Z is given by:

$$V_Z = -V_{DD} \times \frac{C_{FLY}}{C_{FLY} + C_{LOAD} + C_{PAR}} \quad (2)$$

V. Measurement and Simulation Results

The core converter i.e. bipolar output voltage pulse transformer boost converter using various types of transistor types and shunt regulator is successfully taped out and tested. To test the boost converter capability, an input voltage source is set up to emulate TEG [1] which has R_{TEG} of 400 Ω. Transformer used is a pulse transformer with 1:1 turn ratio, 10 mH primary inductance, 0.86 µH leakage inductance, DC coil resistance of 1.3 Ω and occupies less than 1 cm^2 of PCB area. D_1 and D_2 are off-chip Schottky diodes with turn-on voltage V_D of 50 mV (@I_D = 500 nA). C_C and R_C is 10 pF and 300 kΩ respectively.

Measured oscilloscope waveforms of the boost converter with the lowest input voltage are shown in Fig. 5. Various transistor types available in the CMOS 0.13-µm process are tested. Table II summarizes the measured minimum input voltage and input power required to achieve self startup and ±1 V output. It is noted that the proposed boost converter topology does not depend on particular type of transistor.

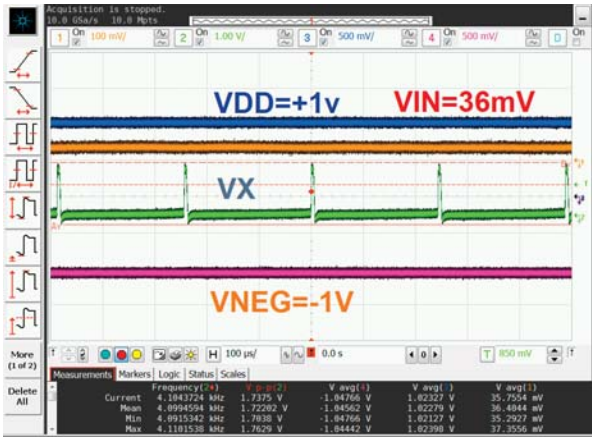

Fig. 5. Measured oscilloscope waveforms showing minimum input voltage, ±1 V output and V_X using 1.2 V Low V_{TH} NMOS

TABLE II. Startup Characterisitcs Using Different Transistors

Transistor type	V_{IN_MIN}	P_{IN_MIN}	Switching frequency (F_{SW})
1.2 V Low V_{TH} NMOS	36 mV	5.8 µW	4.1 kHz
1.2 V Zero V_{TH} NMOS	49 mV	3.2 µW	10.9 kHz
3.3 V Low V_{TH} NMOS	89 mV	2.5 µW	20.6 kHz

The simulated full system operations under varying input voltage (V_{IN}) are shown in Fig. 6. With lower V_{IN}, charge pump is running at lower frequency. As V_{IN} increases, the

system senses the voltage change and will speed up the charge pump clock frequency accordingly. Finally, the proposed energy harvesting scheme is compared against another three state-of-the-art TEG-powered boost converter in Table III. All works are realized in standard CMOS 0.13-µm process except [4]. Having the highest efficiency, [17] is a single inductor boost converter without self-startup function. For [4], [5] and this work, the fully electrical self-startup function is realized using transformer (coupled inductors pair) built-in feedback mechanism i.e. mutual inductance. For transformer-based boost converter, there is at least 14% additional power conversion efficiency trade-off against single inductor system.

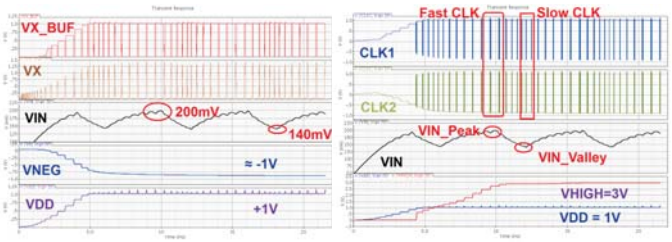

Fig. 6. Simulated full system operations under varying input voltage

TABLE III. PERFORMANCE COMPARISONS WITH RELATED WORKS

References	JSSC 2010 [17]	LTC3108 [4]	JSSC 2012 [5]	This work
CMOS Process	0.13-µm	N/A	0.13-µm	0.13-µm
Start-up mechanism	External battery	1:100 Transformer	1:60 Transformer	1:1 Transformer
Minimum self-startup voltage	650 mV	**20 mV**	40 mV	36 mV
Regulated output voltage	1 V	**2.35 – 5 V**	2 V	±1 V, 3 V
Peak efficiency	**75%**	40%	61%	57% (V_{OUT} = ±1 V, measured) 46% (V_{OUT} = 3 V, simulated)
Maximum output power	175 µW	600 µW	**2.7 mW**	1.5 mW
Maximum power point tracking?	No	No	Yes	No

VI. CONCLUSIONS

A thermoelectric energy harvesting scheme offering both 1 V and 3 V output voltages is proposed. Negative voltage generated by the pulse transformer boost converter is used to enhance the charge pump driving clock, which essentially turns a conventional cross coupled voltage doubler into a voltage tripler. Increased voltage headroom to 3 V is particularly useful for analog, RF and external sensor interfacing. Incoming power level from TEG can be sensed from boost converter cycle using time domain approach, which favorably avoids power hungry voltage domain ADC. Adaptively clocked on-chip charge pump based on sensed input voltage can effectively supplement a shunt regulator to extract excess power harvested by the first stage converter to secondary storage capacitor, without EMI concerns. Most importantly, the proposed architecture is able to scale along with the advancement of CMOS processes.

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