

Machine Learning Based Image Calibration for a Twofold Time-Interleaved High Speed DAC

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Abstract—In this paper, we propose a novel image calibration algorithm for a twofold time-interleaved DAC (TIDAC). The algorithm is based on simulated annealing, which is often used in the field of machine learning to solve derivative-free optimization (DFO) problems. The digital-to-analog converter (DAC) under consideration is part of a digital transceiver core that contains a high speed analog-to-digital converter (ADC), microcontroller, and digital control via a Serial Peripheral Interface (SPI). These are used as tools for designing an algorithm which suppresses the interleave image to the noise floor. The algorithm is supported with experimental results in silicon on a 10-bit twofold TIDAC operating at a sample rate of 50 GS/s in 14nm CMOS technology.

I. INTRODUCTION

Conventional radio-frequency (RF) front-ends are typically composed of several mixers, local oscillators and analog filters. These components are a sizeable expense in terms of cost, area, and power, especially when implemented in phased array systems with several radiating antenna elements [1]. Fortunately, integrated circuit technology has advanced to such a degree that conventional RF front-end solutions are being replaced with high speed ADCs, DACs and digital signal processing (DSP) which perform frequency conversion and filtering operations in the digital domain [2]. This allows data converters to be placed closer to the antenna, thereby significantly reducing system cost and power consumption. In addition, high speed converters have their thermal and quantization noise power spread across a wide Nyquist zone, which enhances dynamic range after processing gain. In order for data converters to achieve multi-GS/s rates, it is common to time-interleave several low speed converters [3], [4]. The high speed of the TIDAC coupled with the area efficiency inherent in 14nm CMOS presents an ideal use case for phased array systems such as next generation radar and 5G. However, the inevitable timing errors and mismatch among the low speed converter slices results in images, or spectral replicas, which corrupt the converter output spectrum. Therefore, image calibration schemes are often necessary in order to avoid considerable loss of dynamic range.

The authors in [4] consider a 20 GS/s 6-bit DAC with no calibration scheme in place. As a result, the spurious-free dynamic range (SFDR) is limited to 40 dB at output frequencies near 9 GHz. The authors in [5] consider a twofold delta sigma TIDAC operating at an aggregate sample rate of

10 GS/s. The clock duty cycle error is understood to be the limiting impairment regarding dynamic range, and calibration schemes are proposed. However, the recommended solution involves digital pre-filtering, which is essentially equivalent to increasing the DAC resolution and tightening matching requirements. Although an analog post-correction scheme is proposed, an accurate measurement of clock duty cycle is required, and this proves to be increasingly challenging at higher sample rates.

In [6], the issue of the interleave image is recognized as a limiting factor in high speed TIDAC performance. A self-calibration circuit is proposed, but it is only functional for sample rates below 200 MS/s. Calibration schemes above this rate are left as an opportunity for future research.

The authors in [7] provide a duty-cycle calibration algorithm for a twofold TIDAC, but assume that the sub-DAC slices are balanced in terms of gain. Practically, this is not a valid assumption for an RF DAC in deep sub-micron processes. In fact, even minor mismatch in sub-DAC gain can exacerbate the interleave image, leading to major loss of dynamic range. This is shown in Section II.

In this paper, we consider a 10-bit twofold TIDAC with current steering architecture operating at an aggregate rate of 50 GS/s using two 25 GS/s sub-DAC slices in 14nm CMOS technology. The DAC is part of a digital transceiver core from Jariet Technologies that contains an on-chip high speed ADC, microcontroller, and digital control via an SPI interface. For the DAC under consideration, there is an image which appears at half of the aggregate sample rate. As far as we know, calibration schemes for DACs at sample rates this high have not been reported. As shown in Section II, the impairments which exacerbate this image are clock duty cycle error, mismatch in sub-DAC analog gain, and clock and data misalignment.

We use the closed-loop configuration shown in Fig. 1 to design an algorithm which suppresses the interleave image to the noise floor. This ensures that dynamic range does not suffer due to interleaving effects. Note that although the authors in [7] use a similar configuration to Fig. 1, the algorithm proposed herein does not assume the sub-DACs are balanced in terms of gain. In addition, the configuration in Fig. 1 does not rely on any bandwidth limited circuitry as in [6], and does not tighten matching requirements as in [5].

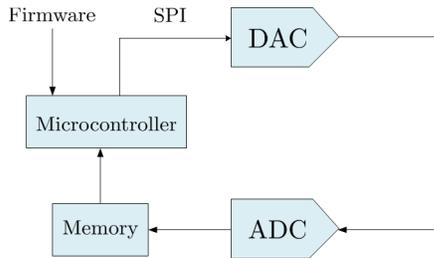


Fig. 1: Block diagram of the TIDAC in a closed loop configuration.

In Section II, we provide some background information on twofold TIDACs. Using Fourier analysis, we explicitly show how specific impairments can cause an undesired image at half of the aggregate sample rate. In Section III, we concretely define the problem at hand in an integer programming framework, and a novel solution is proposed based on simulated annealing. In Section IV, we apply this solution to a 50 GS/s DAC in 14nm CMOS and provide experimental results which highlight its efficacy in terms of image suppression. We conclude in Section V by summarizing the key results and providing some direction for future research.

II. TWOFOLD TIME-INTERLEAVED DAC

The block diagram for the general M -bit TIDAC operating at a sample rate of f_s is illustrated in Fig. 2.

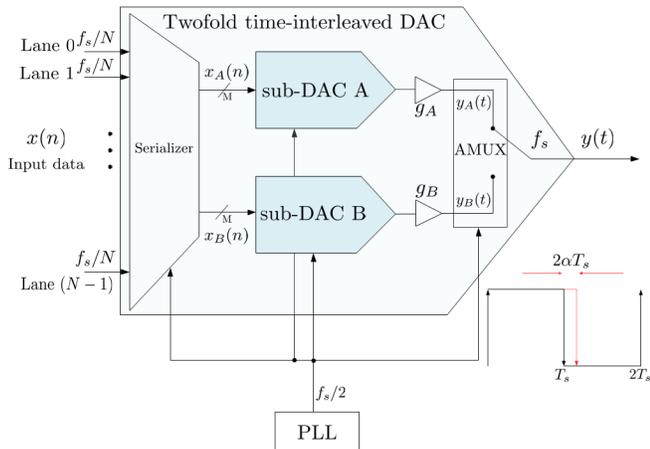


Fig. 2: Simplified block diagram of the TIDAC, the fractional timing error, α , shown in lower right.

A phase locked loop (PLL) generates a clock at frequency $f_s/2$ which is distributed to the blocks denoted by serializer, sub-DAC A, sub-DAC B, and AMUX. The serializer contains a clock tree with several 2-to-1 multiplexers that serialize the N low speed parallel lanes into two high speed ones at the $f_s/2$ rate. The sub-DAC slices employ current drivers for each bit to convert the M -bit code presented at the input to an analog output current. The drivers are composed of binary weighted current sources and clock driven switches. When the switches are active, current is driven to the output, and when

they are inactive, current is dumped to a dummy node which is not shown in the diagram. This is controlled by the analog multiplexer (AMUX).

Ideally, in this ping-pong like configuration, each sub-DAC drives current to the output for 50% of the half-rate clock period. However, this is generally not the case due to unavoidable clock duty cycle error. In Fig. 2, we include a fractional timing offset factor $\alpha \in [-1, 1]$ in order to account for this. Note that $\alpha = 0$ corresponds to the ideal case of 50% duty cycle. In this section, we show that this impairment causes an image in the frequency domain which is located at $f_s/2$. Also shown in Fig. 2 are the sub-DAC analog gains, g_A and g_B . Note that in general, $g_A \neq g_B$ mainly due to current source imbalance between the sub-DACs, and this also causes an image at $f_s/2$. We refer to the architecture illustrated in Fig. 2 as a current steering twofold TIDAC. We proceed by computing $Y(f)$, which is the Fourier transform of the DAC output $y(t)$. Throughout the paper, we denote the Fourier transform of a time-domain signal $y(t)$ by

$$Y(f) = \int_{-\infty}^{\infty} y(t) e^{-j2\pi ft} dt. \quad (1)$$

Note that

$$y(t) = y_A(t) + y_B(t), \quad (2)$$

so we can compute the Fourier transform of the individual sub-DACs and then simply add the result to obtain $Y(f)$ by linearity of the Fourier transform. Without loss of generality, assume that sub-DAC A is driving current to the output at time $t = 0$. Note that $y_A(t)$ can be modeled as a sum of phase shifted return-to-zero (RZ) pulses whose amplitude is determined by the discrete-time sequence $x_A(n) = x(2nT_s)$, where $x(t)$ is the continuous-time representation of the input. In particular, we have

$$y_A(t) = g_A \Pi \left(\frac{t - \frac{T_s}{2}(1 + 2\alpha)}{T_s(1 + 2\alpha)} \right) * \left(x(t) \cdot \sum_{k=-\infty}^{\infty} \delta(t - 2kT_s) \right) \quad (3)$$

where

$$\Pi(t) := \begin{cases} 0 & \text{if } |t| > \frac{1}{2} \\ 1 & \text{if } |t| = \frac{1}{2} \\ 1 & \text{if } |t| < \frac{1}{2} \end{cases} \quad (4)$$

$\delta(t)$ is the Dirac delta function, and $*$ denotes the convolution operator. It is clear that (3) is a sum of phase shifted RZ pulses, as it is the convolution of a rectangular function with an impulse train. Taking the Fourier transform of (3), we have

$$Y_A(f) = \frac{g_A}{2} (1 + 2\alpha) \text{sinc}(fT_s(1 + 2\alpha)) e^{-j\pi fT_s(1 + 2\alpha)} * \sum_{k=-\infty}^{\infty} X \left(f - k \frac{f_s}{2} \right) \quad (5)$$

where $\text{sinc}(x) := \sin(\pi x)/(\pi x)$, and we use the fact that convolution in the time domain becomes multiplication in the frequency domain and vice-versa. The Fourier transform of $y_B(t)$ is obtained similarly, and is given by

$$Y_B(f) = \frac{g_B}{2} (1 - 2\alpha) \text{sinc}(fT_s(1 - 2\alpha)) e^{-j\pi fT_s(1-2\alpha)} \times \sum_{k=-\infty}^{\infty} X\left(f - k\frac{f_s}{2}\right) e^{-j\pi k(1+2\alpha)} \quad (6)$$

Note the additional complex exponential factor in the sum of (6) compared to (5) due to the assumption that sub-DAC A is aligned at $t = 0$. Using (2), the Fourier transform of the DAC output $y(t)$ is

$$Y(f) = Y_A(f) + Y_B(f) \quad (7)$$

where $Y_A(f)$ and $Y_B(f)$ are given by (5) and (6) respectively. Note that if $\alpha = 0$, the complex exponential in the sum of (6) is -1 for k odd and will cancel the corresponding term in (5) if and only if $g_A = g_B$. As mentioned in the introduction, clock and data misalignment also exacerbates the $f_s/2$ image.

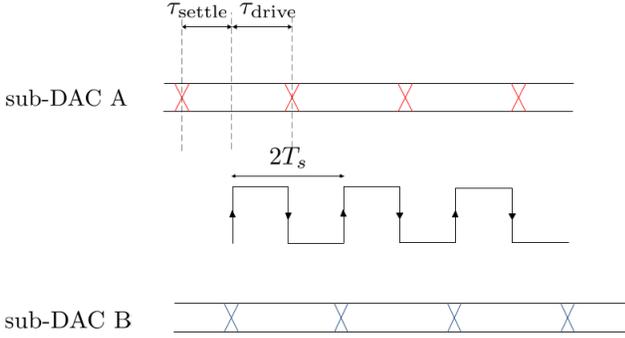


Fig. 3: Illustration of clock and data alignment for a twofold TIDAC.

When sub-DAC A undergoes a data transition, there is a settling window of τ_{settle} as shown in Fig. 3. During this time, sub-DAC A is dumping current to the dummy node while sub-DAC B is driving current to the output. The ideal scenario corresponds to the case where the clock edges are equidistant from the data transitions as illustrated in Fig. 3. In any other scenario, one sub-DAC has a longer (or shorter) τ_{drive} than the other. It is this timing imbalance which exacerbates the image at $f_s/2$ in a manner similar to that of clock duty cycle error. For the chip under consideration in Section IV, there is an algorithm that performs coarse clock and data alignment, but that is beyond the scope of this paper.

Consider a twofold TIDAC for the case in which the ideal output is a sinusoid at frequency f_{out} . From inspection of (7), there is an interleave spur which appears at $f_s/2 - f_{\text{out}}$. The contour plots in Fig. 4 illustrate the -50 dBc level curves of the interleave spur magnitude for various values of f_{out} . These are obtained using (7). If the gain and duty cycle errors are contained within these contours on the lower left region of Fig. 4, then we guarantee the image spur is less than -50 dBc, which is reasonable from an SFDR perspective for a wideband

RF DAC. From Fig. 4 it is clear that extremely small gain and duty cycle errors are required for reasonable DAC SFDR performance.

In Section III, we propose a machine learning based algorithm which uses digital control to suppress the interleave spur to the noise floor.

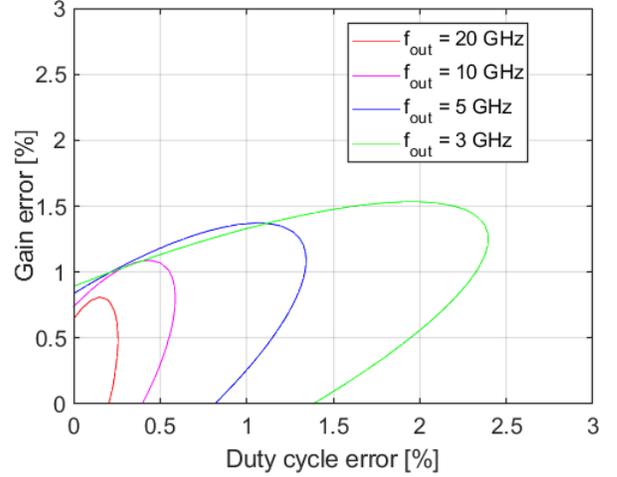


Fig. 4: -50 dBc level curves of interleave image magnitude when the ideal output is a sinusoid at frequency f_{out} .

III. SIMULATED ANNEALING ALGORITHM

As mentioned in the introduction, the DAC under consideration is part of a digital transceiver core that contains a high speed ADC and digital control via a microcontroller and SPI interface. There are several controls which remedy the impairments discussed in Section II. Table I outlines these controls along with their corresponding objectives. Note that the chip under consideration in Section IV has these controls split into six different control registers, each of which has a wide range of discrete settings. Therefore, we begin by defining a state vector $\mathbf{s} \in \mathcal{S} \subset \mathbb{R}^6$ whose entries are composed of the digital control settings. In order to find the optimal control settings, we require the ability to measure the interleave spur power. Consider a TIDAC with sample rate f_s and sinusoidal output with frequency f_{out} . Again, by inspection of (7), we observe that an interleave spur appears at $f_s/2 - f_{\text{out}}$. Using the on-chip ADC, we then sample the DAC output, compute the fast Fourier Transform (FFT), and monitor the bin corresponding to $f_s/2 - f_{\text{out}}$. The energy in this FFT bin then defines a cost function $C : \mathcal{S} \rightarrow \mathbb{R}$. The objective is to then choose a vector $\mathbf{s}^* \in \mathcal{S}$ such that

$$\mathbf{s}^* = \arg \min_{\mathbf{s}} C(\mathbf{s}) \quad (8)$$

The objective defined by (8) is an integer programming problem. There are a couple of key items worth mentioning. First, note that we do not have an expression for the cost function $C(\mathbf{s})$, so optimization via relaxation and differentiation is not an option. In addition, the solution space is

Digital control	Objective
sub-DAC output current	$g_A \rightarrow g_B$
$f_s/2$ clock duty cycle	$\alpha \rightarrow 0$
Phase rotator	$\tau_{\text{settle}} \approx \tau_{\text{drive}}$ for both sub-DACs

TABLE I: List of digital controls with corresponding objectives.

large, as the state vector lies in six-dimensional space and each entry has a wide range of discrete values. A suitable algorithm which promotes global optimum convergence in this scenario is known as simulated annealing [8]. The pseudocode for simulated annealing is outlined in Algorithm 1.

Algorithm 1: Simulated annealing.

Input: $s_0, T_{\max}, T_{\min}, \gamma, \beta, K$

Output: s^*

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1  $s \leftarrow s_0$ 
2  $s^* \leftarrow s$ 
3  $T \leftarrow T_{\max}$ 
4 while  $T > T_{\min}$  do
5   for  $k \leftarrow 0$  to  $K - 1$  do
6      $s' \leftarrow n(s)$ 
7      $\Delta E \leftarrow C(s') - C(s)$ 
8     if  $\Delta E \leq 0$  then
9        $s \leftarrow s'$ 
10      if  $C(s) < C(s^*)$  then
11         $s^* \leftarrow s$ 
12      else if  $\text{rand}(0,1) < \exp(-\beta \frac{\Delta E}{T})$  then
13         $s \leftarrow s'$ 
14    $T \leftarrow \gamma T$ 

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Algorithm 1 has a temperature parameter T which starts high at T_{\max} and gradually reduces to T_{\min} exponentially with factor γ . At each value of T , we perform K iterations which involve a cost comparison of the current state s with a neighboring state $s' = n(s)$. Note that states s' whose cost is less than or equal to the current state s are always accepted (i.e. $\Delta E \leq 0$). If a neighbor is accepted under the criteria $\Delta E \leq 0$, then we check whether or not it has a lower cost than the optimal state s^* . However, states with higher cost (i.e. $\Delta E > 0$) are not necessarily rejected. In fact, the acceptance of higher cost states is controlled by the temperature T in a probabilistic manner. Note that the term $\exp(-\beta \frac{\Delta E}{T}) \rightarrow 1$ as $T \rightarrow \infty$ where $\beta > 0$ is a hyperparameter. This implies that the state space is explored aggressively when T is large since the acceptance of higher cost states becomes more probable. A key component of Algorithm 1 involves constructing the neighboring state function $n(s)$. In our case, this process first involves choosing a number from the discrete uniform distribution $\mathcal{U}\{1,6\}$ which corresponds to one of the six digital controls. We then choose another number uniformly at random over a range which covers the selected control setting.

The neighbor state is found by simply substituting the new control setting into a copy of the previous state.

IV. EXPERIMENTAL RESULTS

In this section, we use the Agilent N9030A spectrum analyzer to apply Algorithm 1 to a 10-bit twofold 50 GS/s TIDAC in 14nm CMOS. Note that the spectrum analyzer samples the DAC output which effectively emulates the on-chip ADC.

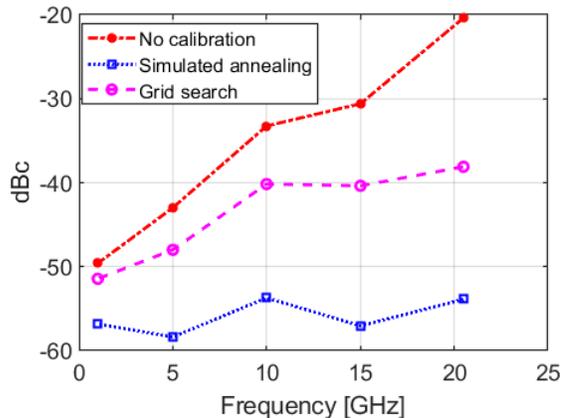


Fig. 5: Interleave spur performance over Nyquist.

The plot in Fig. 5 demonstrates the efficacy of Algorithm 1 over Nyquist and compares it to a simple grid search over the state space. Note that Algorithm 1 keeps the interleave spur well below -50 dBc. After starting Algorithm 1 with control registers in their initial states, convergence occurs after an average of 160 interleave spur measurements, and grid search was performed with 280 measurements. Note that at high frequency, simulated annealing has a 15 dB improvement over grid search while requiring nearly half as many measurements. The parameters used as input to Algorithm 1 were $\gamma = 0.8$, $K = 30$, and $\beta = 50$. These experiments were conducted using an Altera FPGA which serves as a bridge between the PC and the SPI interface. The test board and chip are shown in Fig. 6.

V. CONCLUSION

In this paper, a novel image calibration algorithm for a twofold TIDAC is proposed and verified in silicon on a 10-bit 50 GS/s DAC in 14nm CMOS. The algorithm does not exacerbate matching requirements as in [5], and does not assume the sub-DAC gains are balanced as in [7]. Furthermore, bandwidth limited calibration circuitry is not required as in [6]. Although an on-chip high speed ADC is assumed, this is becoming much more practical with the use of low power deep sub-micron processes like 14nm CMOS. Future work involves repeating the measurements in Section IV using the on-chip DAC to ADC loopback path. Beyond interleave impairments, high speed data converters have harmonic distortion. Using machine learning for harmonic suppression would be another interesting and fruitful research opportunity.

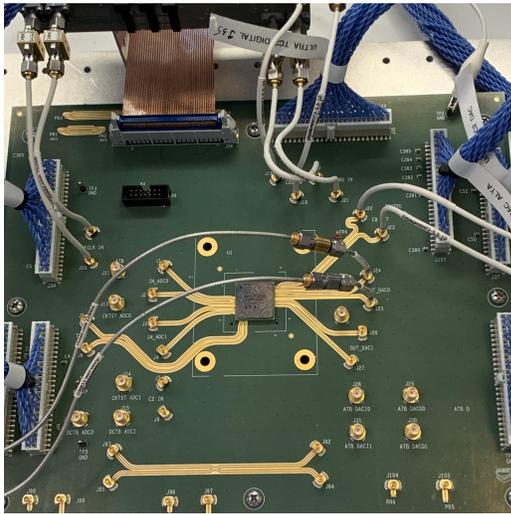


Fig. 6: Test board with digital transceiver chip containing a 50 GS/s TIDAC.

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