# DIGITAL RF-OVER-FIBER LINKS BASED ON CONTINUOUS-TIME DELTA SIGMA MODULATION

by

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**Digital RF-over-Fiber Links Based on Continuous-Time Delta Sigma Modulation**

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*Dedicated to my advisor professor, Soumyajit Mandal, who taught me useful IC design knowledge and shared his rich and precious circuit experience with me.*
*Dedicated to my mother, Chunlian Liu, who gives me endless love and support.*
*Dedicated to my friend, Jifu Liang, who gave me detailed and patient explanations to my academic questions.*

# Table of Contents

# List of Tables

# List of Figures

# Acknowledgements

## 0.1 Acknowledgements

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# Abstract

Digital RF-over-Fiber Links Based on Continuous-Time Delta Sigma Modulation

Abstract

by

XI GAO

## 0.2 Abstract

RF-over-fiber systems, in which RF signals modulate the intensity of a light source that is then transmitted over optical fiber to a remote unit, are attracting an increasing amount of attention. Such links have several advantages, including i) relatively low installation and maintenance costs; ii) immunity to the harsh RF and electromagnetic interference (RFI/EMI) often found in industrial environments; and iii) greatly improved physical-layer security compared to over-the-air wireless links. However, the dynamic range (DR) of a conventional analog RF-over-fiber link suffers from the limited linearity of electrical-to-optical (E/O) converters, and deteriorates further as its length increases. A solution to this problem is to digitize the analog RF signal before transmission over the optical fiber. Delta-sigma modulators (DSMs) are attractive for such digitization because of their low circuit complexity and scalability to advanced process nodes. Moreover, DSM-based RF-over-fiber links do not require a DAC at the receiver because signal reconstruction can be easily performed by an analog or digital low-pass filter, which

in turn simplifies the receiver design and enables direct interfacing to legacy data acquisition equipment designed to process analog inputs. Continuous-time DSMs (CT-DSMs) are particularly attractive because of their inherent anti-aliasing properties, relaxed speed requirements for the active elements, resistive input impedance, and low power consumption compared to discrete-time equivalents.

This thesis describes the design of a novel high-performance CT-DSM using in digital RF-over-fiber links that transmit high-DR RF signals in noisy environments, such as those generated by magnetic resonance imaging (MRI) coils. The CT-DSM uses a fourth-order design with one-bit digital-to-analog converter (DAC). An op-amp assistant circuit and chopping techniques are used to optimize system performance. The proposed modulator was designed and implemented in the TSMC 180 nm CMOS process. Simulation results show a maximum signal-to-noise-and-distortion ratio (SNDR) of 89.3 dB for a sampling frequency of 100 MHz, a chopping frequency of 50 MHz, and an oversampling ratio (OSR) of 100, resulting in a Walden figure of merit (FoM) of 360 fJ/bit. Preliminary measurement results confirm the functionality of the proposed CT-DSM design.

# 1 Introduction

## 1.1 Research Background and Objective

Magnetic resonance imaging (MRI) is an imaging method that uses powerful magnets, radio waves, and a computer to make detailed pictures of the scanned body. Based on this technique, MRI Machines are widely used to assist in medical procedures and researches. Conventional electrical connections inside the MRI machine, as shown in Figure 1.1, use bundles of coaxial cables, which have some disadvantages like i) wastage of space, ii) radio frequency interference (RFI) from the transmit coils and gradients, iii) Physical limits including rigidity, weight and so on.


Figure 1.1. MRI machine with its zoomed-in connections inside.

Correspondingly transmission of radio frequency (RF) signals over optical fiber (shown in Figure 1.1) is beginning to attract attention because of cost effectiveness, extremely broad bandwidth, and robustness to external RF interference (RFI) as compared to conventional links based on coaxial cables. Analog optical links have been investigated due to their relatively simple RF circuit structure and minimum modification to the MRI system. A good deal of studies have been conducted to investigate the feasibility of analog optical links[2–7]. However, existing versions of such optical links based on transmitting

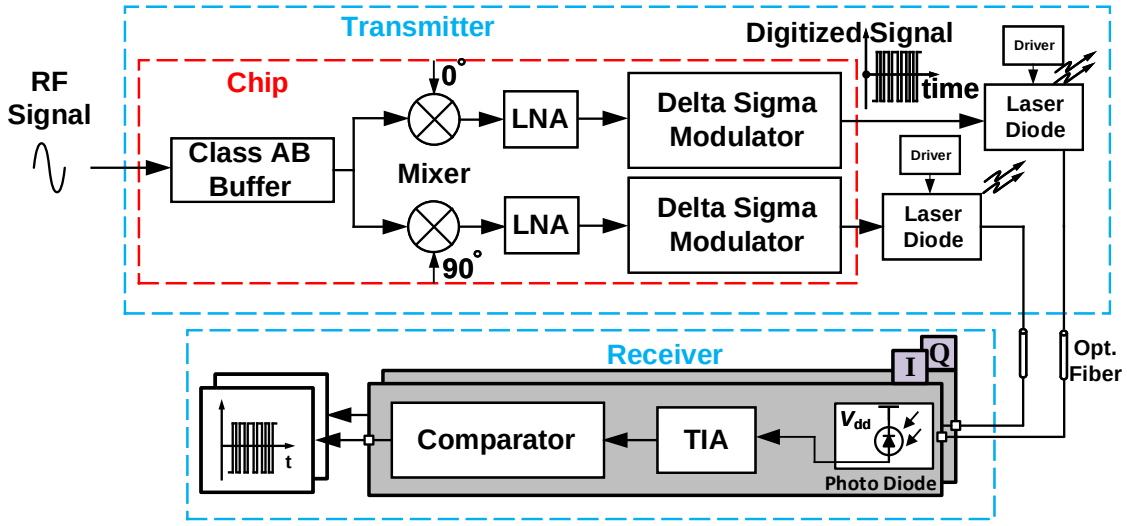


Figure 1.2. Block diagram of the complete digital RF-over-fiber system.

analog waveforms result in limited dynamic range (DR) due to the nonlinear behavior of the electro-optic (E/O) converters (e.g., Mach-Zehnder modulators (MZMs)-external modulators and photodiodes) and degradation of noise figure. Then digital RF-over-fiber transmission system based on delta-sigma modulation (DSM) has been developed as a way to overcome these issues. In this project, the RF signal comes from a 3T MRI scanner, whose bandwidth is typically ±500kHz centered around 123.3 MHz. For this

kind of narrow band signal, Delta sigma modulator (DSM) is a good choice as the analog-to digital converter, which achieves high signal-to-noise and distortion ratio (SNDR) by low-resolution quantization at a much higher sampling rate compared with the Nyquist frequency. In addition, reconstruction of the analog signal after a DSM does not require a DAC. It can be performed simply by applying a low-pass filter to the quantized signal.

This research project is developing such a digital RF-over-fiber links to overcome these issues, thus enabling the transmission of high-dynamic (DR) RF signals in noisy environments, such as those generated by magnetic resonance imaging (MRI) coils. A novel high-performance continuous-time (CT) delta-sigma modulator (DSM) is used to digitize the input waveform, as shown in Figure 1.2. On the transmitter side, the RF input is fed to an on-chip class AB buffer with impedance matching and then down-converted to the baseband with a quadrature mixer. In particular, a continuous-time delta sigma modulator (CT DSM) design is selected because of its inherent anti-aliasing and relaxed speed requirements as compared to discrete-time equivalents. So two proposed CT-DSMs are utilized to digitize the baseband I/Q signals with high SNDR, and the digitized signals are then transmitted over the optical fibers using low-linearity E/O converters, thus resulting in greatly reduced distortion compared to an analog link. On the receiver side, a photodiode converts the optical signal coming from fiber links back to current, which is then amplified and converted to voltage by a transimpedance amplifier (TIA). The output is then digitized again by a comparator, and the generated signal can be fed directly to digital platforms for further processing.

## 1.2 Literature Review

RF-over-fiber transmission systems, in which RF signal modulates the intensity of a light source and are then transmitted over optical fiber to a remote unit, are attracting an increasing amount of attention[8–10]. Such links have several advantages, including i) relatively low installation and maintenance costs; ii) immunity to the harsh RF and electromagnetic interference (RFI/EMI) often found in industrial environments; and ii) greatly improved physical-layer security compared to over-the-air wireless links.

At the beginning of the development of the RF-over-fiber, the analog RF signal is directly used to modulate the electrical-optical converter (EOC), e.g., photodiode. Then its analog form is transmitted through the optical fiber and received by the optical-electrical converter (OEC) on the receiver side. The block diagram of analog RF-over fiber link is shown as Figure 1.3. However, this transmission link based on analog signal suffers from inter-modulation distortions followed with the nonlinearity of the optical components. In addition, the dynamic range of a conventional analog RF-over-fiber link suffers from the limited linearity of E/O converters and deteriorates further as the optical fiber link's length increases[11,12]. Furthermore, even though the external modulator such as Mach-Zehnder modulator (MZM) is used to compensate, the extra nonlinearity from the MZM brings another limiting factor. Circuit complexity and reduced cost-effectiveness of the optical link arise.

A solution to this problem is to digitize the analog RF signal before transmission over the optical fiber[13–15]. The block diagram of digital RF-over-fiber link is shown in Figure 1.3. Among several candidates for digitizing analog signals, delta sigma modulators have recently drawn attention because of their low circuit complexity and scalability to advanced process nodes[16,17]. Moreover, DSM-based digitized RF-over-fiber links do not

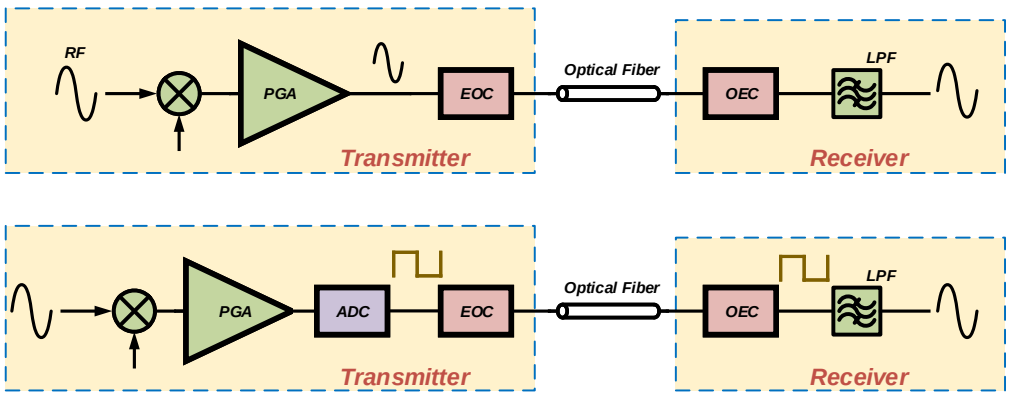


Figure 1.3. Block diagram of analog and digital RF-over-fiber link.

require a digital-to-analog converter (DAC) at the receiver because signal reconstruction can be easily performed by a low-pass filter through the digital platform, which in turn simplifies receiver design and enables direct interfacing to legacy equipment.

There are mainly two types of delta sigma modulator: discrete-time one and continuous-time one. Discrete-time (DT) DSM implementing switched-capacitor circuits has been the designer's choice for the last few decades. Recently, continuous-time (CT) DSM is particularly attractive because of their inherent anti-aliasing properties, relaxed speed requirements for the active elements, and low power consumption compared to discrete-time equivalents[18–20].

Figure 1.4 shows the signal chain of the DT DSM and CT DSM. In the DT DSM, the input signal is sampled prior to the loop filter, which is a discrete time loop filter implemented with switched-capacitor integrator circuits. The key difference between the DT DSM and CT DSM is the sampling operation's location in the signal chain. For the CT DSM, input sampling occurs before the quantizer and its loop filter is implemented with continuous-time circuits, often RC or $g_m$/C integrators. We know aliasing takes place where the sampling occurs. The sampling operation for the CT DSM is behind of

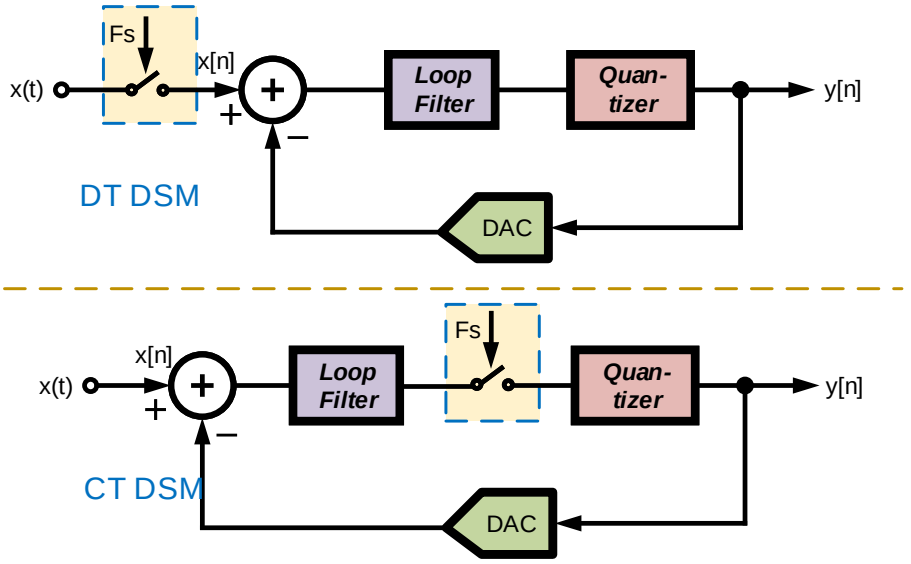


Figure 1.4. Signal chains of the DT-DSM and CT-DSM.

feedback with the injected quantization noise, which means aliasing is attenuated by the same operation as to the quantization noise. That's the CT DSM's inherently anti-aliasing property, which simplified the necessity for extra anti-aliasing filter used in DT DSM. In addition, CT DSM implemented continuous-time DAC in their feedback has reduced power consumption and enable high-speed operation. However, employing a switched-capacitor DAC in the CT DSM can relax the jitter requirements on the clock significantly.

## 1.3 Basic Knowledge of Delta Sigma Modulator

Computational and signal processing are now mainly performed by digital signals, which is robust in signal transmission, easier to achieve with simple digital circuits structure and can be combined to obtain very complicated, accurate and high-speed systems. In this case, analog to digital converter (ADC), which translates an analog signal into a digital signal for data processing, plays an essential role for the signal processing. There are

mainly two kinds of data converters: Nyquist-rate converters and oversampling converters. The performance of Nyquist-rate converter is more dependent on its matching of the analog components including resisters, current sources and capacitors. Furthermore, for higher linearity and resolution ($N$), Nyquist-rete converter requires at least $2^N$ clock period to complete a single-bit's conversion, which takes too much time for most signal processing application. Whereas, oversampling data converter operates much faster than the Nyquist rate and the accuracy requirements on the analog components are relaxed compared to Nyquist-rate converters[1].

This section gives basic operation of the oversampling converter - delta sigma modulator (DSM). Because the decimation part after DSM can be taken over by some digital platform, there is no discussion about this part. For better understand the operation of DSM, the first-order delta sigma modulator is be discussed here.

### 1.3.1 Oversampling and Quantization

The input signal's bandwidth is $B$, we know that $Nyquist frequency$, which is defined as $f_{Nyquist} = 2f_B$, is the minimum sampling frequency that prevents aliasing's occurrence. When a signal is sampled at a higher rate than $2f_B$, the number that compares the actual sample frequency $f_s$ to the Nyquist frequency $2f_B$ is called oversampling frequency ratio (OSR), and is defined as

$$OSR = \frac{f_s}{2f_B} \tag{1.1}$$

The benefit of oversampling is to improve the resolution and signal-to-noise ratio of the data converter. In addition, it can help to avoid aliasing and phase distortion by

relaxing the design of the anti-aliasing filter. Moreover, a high OSR acts a crucial role in reducing base-band quantization noise, which will be mentioned soon.

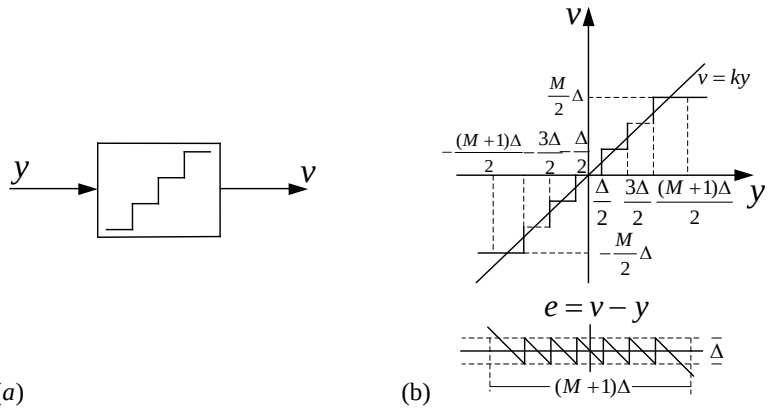


Figure 1.5. (a) Quantizer symbol. (b) Transfer functions and error curves for a symmetric bipolar $M$-step mid-tread quantizer with fixed spacing $\Delta = 2$, $k = 1$.

Quantization is the process of mapping input values from a large set (often a continuous set) to output values in a countable set in mathematics. Rounding and truncation are typical examples of quantization process. if we say sampling makes signals discrete in time, then quantization achieves signals discrete in amplitude. Quantization symbol is shown in Fig. 1.5.The difference ($e$) between the input value ($y$) and its quantized value ($v$) is called $quantization\ \ error$ or $quantization\ \ noise$, as $e = v - y$. For a N-bit quantizer, its signal to $quantization\ noise\ ratio$ $(SQNR)$ is given by

$$SQNR = 6.02N + 1.76dB \tag{1.2}$$

There are some simplifying assumptions: 1) $e$ is assumed to be independent of y; 2) $e$ is assumed to be uniformly distributed in [-1,1], namely $e$ is white noise. In this case, when the input signal $y(t)$ is sampled by the Nyquist frequency, and the spectrum of

$y[n]$ extends from $[-\pi, pi]$. After quantization, $y$ is corrupted by $e$, whose double-side spectral density is flat and equal to $\Delta^2/(24\pi))$., as shown in Fig. 1.6.

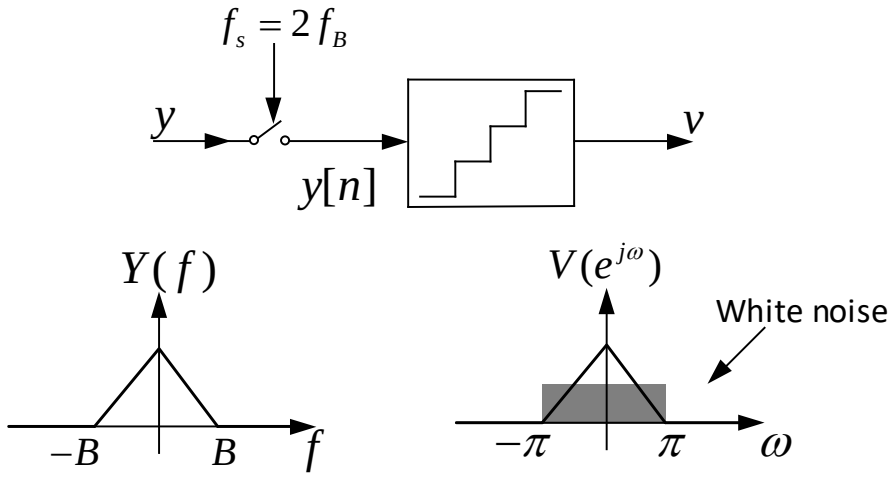


Figure 1.6. Spectral view of the quantization noise assumption. Sampling frequency is Nyquist frequency.

When a band limited signal is sampled by a higher frequency ($OSR \gg 1$), and then the digital sequence is quantized, and filtered by an ideal low-pass filter with a cutoff frequency $\pi/OSR$, the in-band quantization noise can be reduced by a factor of OSR. The double-side spectral density of the data converter system with a higher OSR. quantizer is shown in Fig. 1.7. Of course, there is no free lunch. The trade-off of increasing oversampling rate is that the requirement of the high-speed digital processing should be improved.

In this thesis, a single-bit quantizer is applies at default. Since one-bit DAC does not introduce distortion and is inherently linear.

### 1.3.2 Noise-Shaping Technique

A discrete-time feedback loop with a one-bit quantizer is shown as Fig. 1.8. The quantization noise $e$ comes from the quantizer and a one-sample delay $z^-1$ is inserted for

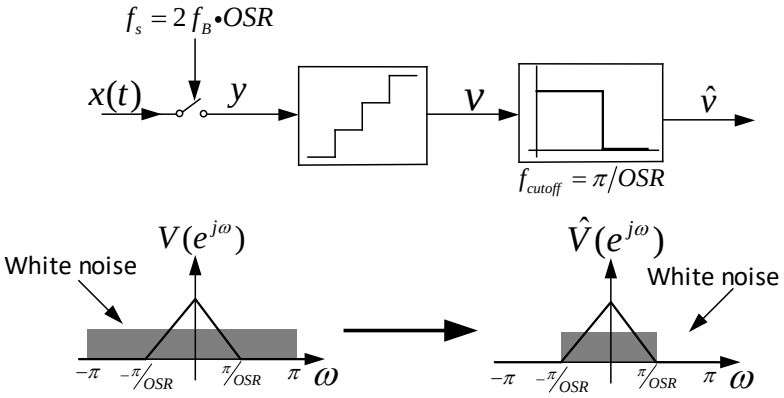


Figure 1.7. Spectral view of oversampling to reduce quantization noise.

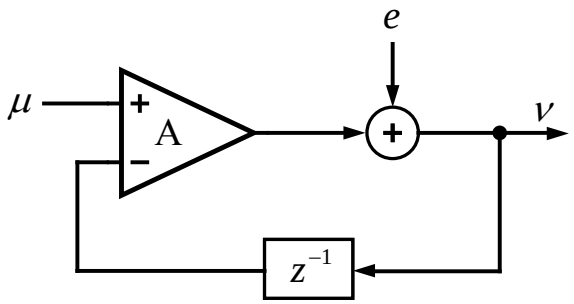


Figure 1.8. A negative feedback loop with a one-bit quantizer.

the loop-filter because the amplifier can only deal with the quantizer's output in next sample. The transfer function of the Fig. 1.8 i the $z$ domain is

$$V(z) = \left(\frac{A}{1 + Az^{-1}}\right) \cdot U(Z) + \left(\frac{1}{1 + Az^{-1}}\right) \cdot E(z) \tag{1.3}$$

In equation 1.3, $\frac{A}{1+Az^{-1}}$ is the signal transfer function (STF) and $\frac{1}{1+Az^{-1}}$ is the noise transfer function (NTF). We want to achieve the maximum SQNR, which requires $A \rightarrow \infty$, such that i) the STF approaches unity, and ii) the NTF is close to zero. On the other hand, the stability of a discrete-time system demands that all its poles should be located in the unit circle in the complex plane, which means $|A| < 1$. In the view of this trade-off,

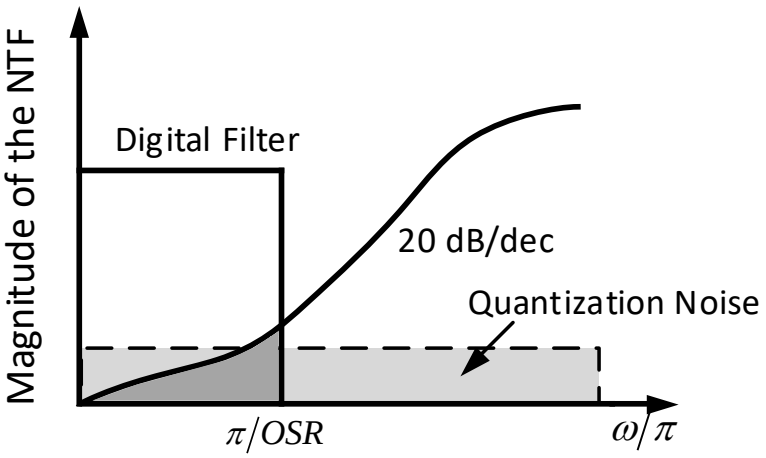


Figure 1.9. Magnitude of the NTF.

an integrating amplifier is applied to the feedback loop since it performs the mathematical operation of integration, which implies $A = \frac{a}{1-z^{-1}}$. As a result, the transfer function becomes

$$V(z) = 1 \cdot U(z) + (1 - z^{-1}) \cdot E(z)) \tag{1.4}$$

Equation 1.4 shows that the STF is unity and the NTF is a first-order high-pass response with a zero of transmission at DC[1]. The magnitude of the NTF is shown in Fig. 1.9.

This gives a infinite gain at DC for the forward amplifier, which helps to compress the quantization noise at the in-band frequency. And then the rest of the quantization noise is high-pass filtered or shaped out of the base-band. This is the noise shaping technique. For a one-bit quantizer, the peak SQNR under the oversampling rate is given by

$$SQNR = \frac{9 \cdot OSR^3}{2\pi^2} \tag{1.5}$$

From the equation 1.5, increasing the OSR quickly improves SQNR.

### 1.3.3 Choice of Order and Structure for the Delta-Sigma Modulator

Another way to increase the SQNR or resolution of the ΔΣ modulator is to apply a high-order loop filter instead of a single integrator, which helps to compress the in-band noise through dividing noise by a large cascaded loop-gain. In principle, by cascading multiple integrators with feedback loops, a high order NTF can be obtained. For an Nth-order loop filter, the in-band noise is approximately

$$q_{rms}^2 = \frac{\pi^{2N} e_{rms}^2}{(2N+1)OSR^{2N+1}} \tag{1.6}$$

Another possible approach to increase the SQNR is to reduce the number of quantizer levels. The 1-bit quantizer that just has two levels is a good choice because of its inherent linearity[1] and simple structure. Furthermore, the 1-bit quantizer's output is just the sign of its input, so it follows that the loop filter's output can be scaled without affecting the modulator's output. It turns out that this can potentially simplify the design of the op-amp used in the integrators of the loop filter[1]. Fig. 1.10 shows the achievable peak SQNR for an Nth order modulator implementing a 1-bit quantizer. This plot shows that $OSR \approx 40$ is sufficient to get SQNR= 90 dB if we pick a fourth-order modulator ($N = 4$).

## 1.4 Structure of the Thesis

In this research, a novel high performance CT-DSM is proposed to overcome design difficulties on speed, noise, and power, thus enabling its use in digital RF-over-fiber links for transmission of high-DR RF signals in noisy environments, such as those generated

[1]This is because a 1-bit quantizer implies two output levels, and these two points then define a single straight line as the transfer function.

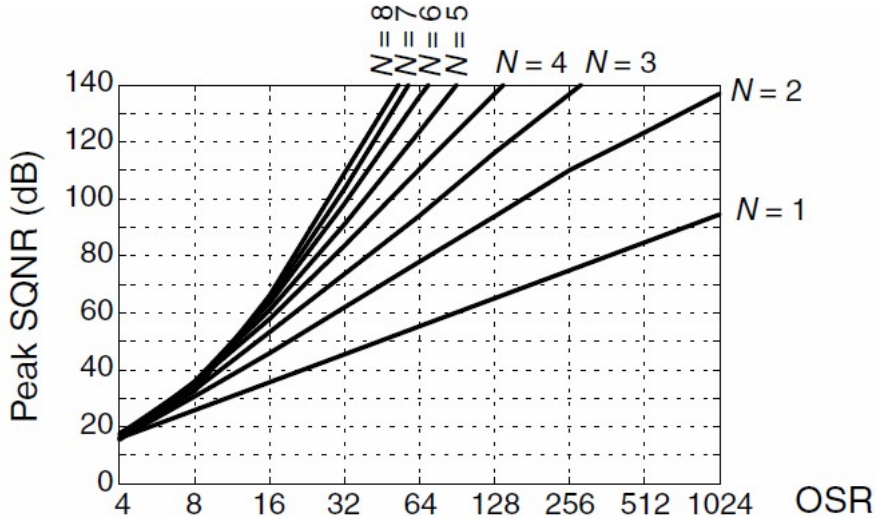


Figure 1.10. Empirical SQNR limits for a 1-bit modulator of order N[1].

by magnetic resonance imaging (MRI) coils. The rest of this thesis is organized as follows: Chapter 2 presents the test of RF-over-fiber links based on a discrete-time delta sigma modulator (commercial chip) to verify the reliability of the transmission. Chapter 3 gives detailed circuits-level description of the proposed CT-DSM (custom chip) and shows simulation results from separate blocks to the whole system using the Cadence IC design suite. Test results and analysis for the custom chip are presented in Chapter 4, while Chapter 5 concludes the thesis and Chapter 6 proposes future work.

# 2 Discrete-Time Delta-Sigma Modulator Test

For this chapter, I would like to thank Mingdong Fan For his work on setting-up and testing the whole link. I also thank David Ariando for his help with programming the Arduino microcontroller for the direct digital synthesizer (DDS).

## 2.1 RF-over-Fiber Transmission Link based on Discrete-Time Delta-Sigma Modulator

To verify the feasibility of the whole RF-over-fiber transmission idea, a transmission link of the digitized MRI signal based on a discrete-time delta sigma modulator (commercial chip) was designed and implemented. The block diagram of the complete RF-over-fiber system is shown as Fig. 2.1. The radio-frequency (RF) signal, which is typically ±500 kHz centered around the carrier frequency of 123.3 MHz coming from a 3 T magnetic resonance image (MRI) scanner, is firstly down-converted to the baseband signal IF by the mixer. The mixer's local frequency (LO) is generated by a programmable direct digital synthesizer (DDS) that is programmed by an Arduino microcontroller. Then the IF signal is amplified to the desired value and fed into the discrete-time delta sigma modulator, which is mainly responsible for digitizing the analog IF signal to a digital sequence with

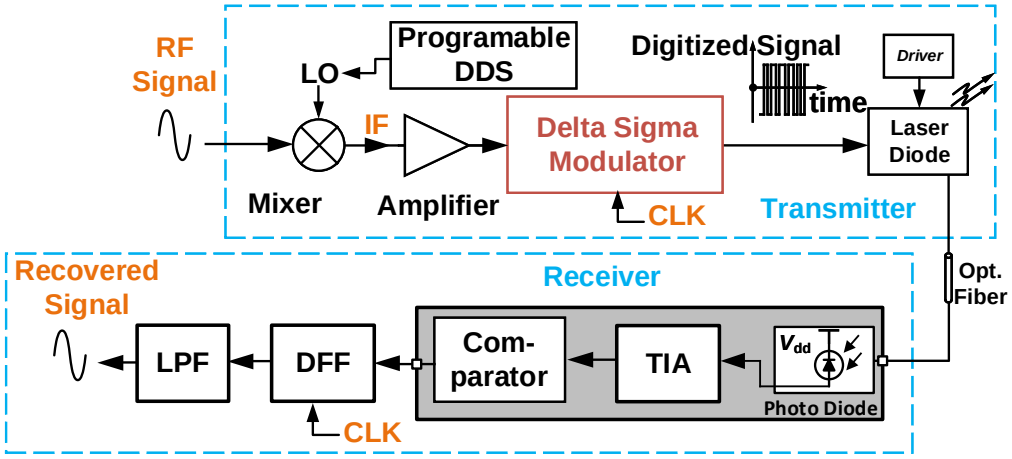


Figure 2.1. Block diagram of the RF-over-fiber transmission line based on a discrete-time delta sigma modulator.

a high-frequency sample clock. This digital sequence will act as the control signal for the NMOS switch and then modulate the laser diode (LD) to generated a corresponding optical signal. After being transmitted over the optical fiber, the optical signal is received by a PIN photodiode which converts the optical signal into a current signal, then this current signal is amplified and converted back to voltage by a trans-impedance amplifier (TIA). The TIA's output is quantized by a comparator and resampled by a D-type flip-flop targeting to remove any accumulated timing jitter. This digital signal is then low-pass filtered to recover the analog baseband signal.

The test board that implements the architecture above are shown in Fig. 2.2 as a proof-of-concept demonstration. A commercial second-order discrete-time delta sigma modulator (AD7403, Analog Devices) is used as the core data converter. The input signal is a 200 kHz sinusoid wave (this limited bandwidth is chosen due to the sampling rate limitations of the commercial chip) generated by a benchtop function generator (Rigol) as the baseband IF signal. The sample frequency is set to 20 MHz, resulting in a over sampling rate (OSR) of 50. A 1310 nm Fabry-Perot laser diode with 30 mA driving current

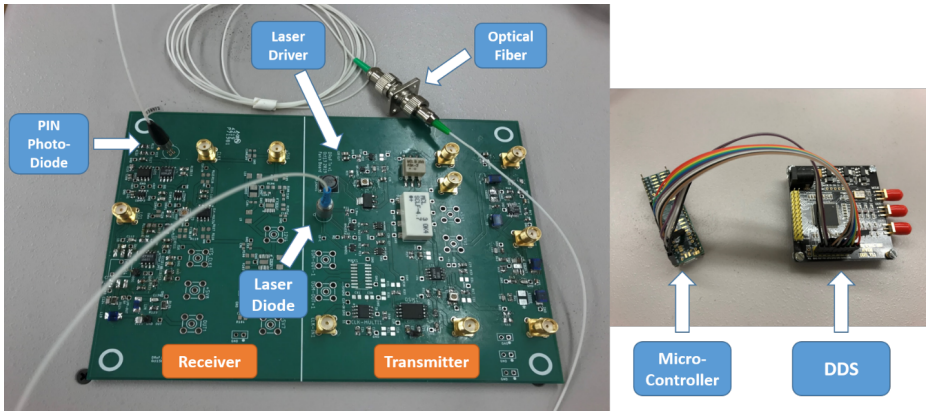


Figure 2.2. Experimental setup of the RF-over-fiber transmission system based on a discrete-time delta sigma modulator.

and a high performance InGaAs PIN photodiode with 0.5 mA driving current are chosen. An active LPF with a cutoff frequency of 300 kHz is used on the receiver side to recover the signal.

## 2.2 Test Results

The test parameters are listed in the Table 2.1. We give an input voltage sweep from 50 mV to 250 mV for the input signal; the peak SNDR was found at 150 mV. The power spectrum density (PSD) of the signal getting the peak SNDR of 55 dB is shown in Fig. 2.3(a). It is obvious that the noise is compressed at low frequency and shaped out from the integrated band to the high frequency domain. For the whole link's transmission, a comparison of the SNDR of the output signal from the DSM, laser diode, and comparator on the receiver side is shown in Fig. 2.3(b). The three plots are close to each other, which verifies the reliability and feasibility of the digitized RF-over-fiber transmission link.

Fig. 2.4(a) presents typical measured baseband signal at the input (before DSM quantization) and output of the optical link, which is a comparation between the input signal and the recovered analog signal from the receiver.

Table 2.1. Test Parameters

| Input Frequency | Input Range | Sample Frequency | OSR | Peak SNDR |
|---|---|---|---|---|
| 200 kHz | 50 mV~250 mV | 20 MHz | 50 | 55 |

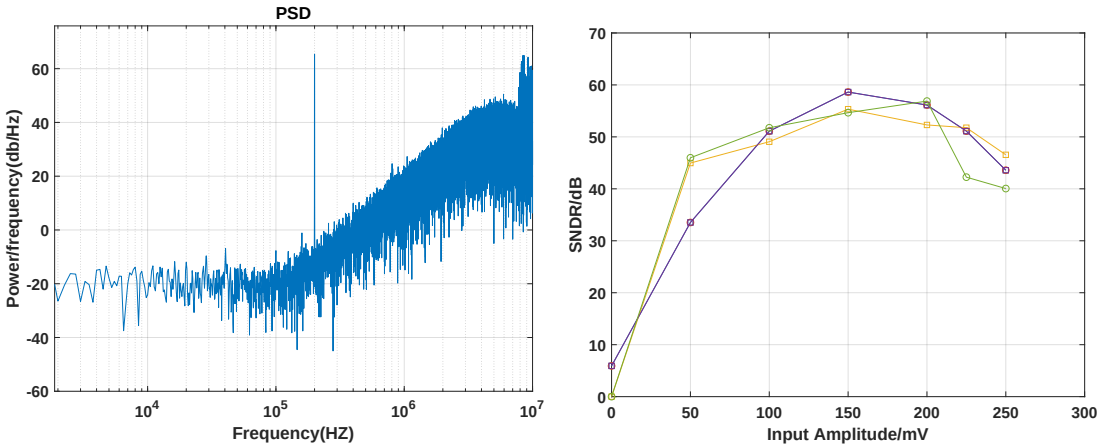


Figure 2.3. (a) PSD of the peak measured SNDR; (b) comparison of the measured SNDR on the transmitter and receiver sides.

Fig. 2.4(b) presents the measured relationship between the RF input power level and the baseband output power for baseband frequencies of 100 kHz and 200 kHz. The linear region for the 200 kHz signal is about 50 dB, from −42 dB to 8 dBm. The curve plateaus near −42 dB mainly because of noise in the measurement system (a digital oscilloscope). The linear region for the 100 kHz signal exceeds 64 dB, from −56 dB to 8 dB, due to the lower signal bandwidth (and thus measurement noise). Repetitions of these experiments with a more sensitive measurement device (an Agilent spectrum analyzer) confirmed a linear range > 60 dB in both cases.

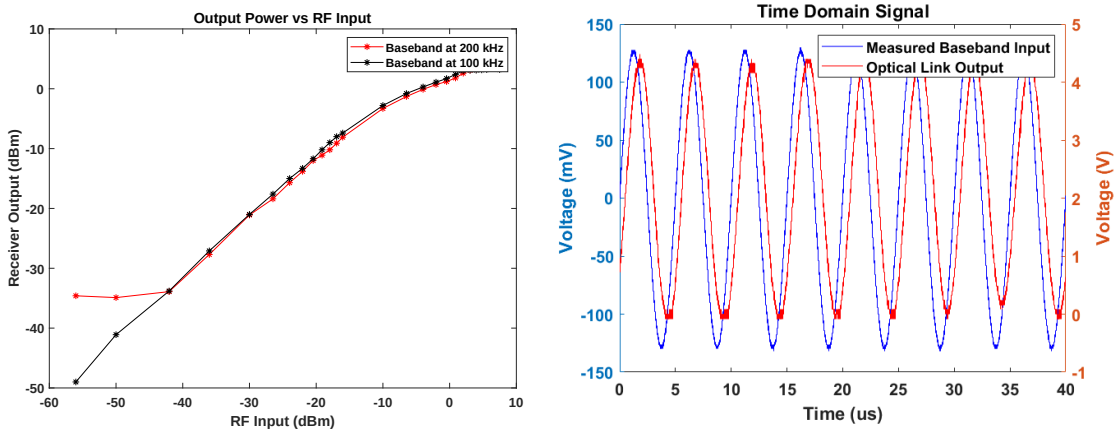


Figure 2.4. (a) Comparison between recovered signal and input signal; (b) the measured linear range for 100 kHz and 200 kHz input signals.

## 2.3 Discussion and Conclusion

A digitized RF-over-fiber transmission link based on discrete time delta sigma modulator (DSM) was constructed as a proof-of-concept. Because the optical fiber's transmission link has robust immunity to the RF interference (RFI), the performance of the transmission is highly dependent on the capability of the DSM. Shown as Fig. 2.4(b), the importance of the DSM's sampling rate in improving the dynamic range was demonstrated.

To further improve the SNDR of the transmitted signal, a higher order and continuous-time integrator is chosen following with the high sampling rate. Compared to the discrete-time DSM, the continuous-time DSM has several advantages, including i) inherent anti-aliasing; ii) less power consumption because of its non-switched integrator; iii) relaxed bandwidth requirement on the first integrator. Correspondingly, a custom chip that implements a fourth-order continuous-time DSM is called for in this application.

# 3 Continuous-Time Delta Sigma Modulator Design

The project focuses on RF-over-fiber links for transmitting signals acquired by MRI receiver coils. The signals are narrow-band, with the center frequency and bandwidth for a typical 3 T scanner being 123.3 MHz and 500 kHz, respectively. We select a sampling frequency of 100 MHz, resulting in OSR = 100. The DSM's SNDR should exceed the expected dynamic range (DR) at its inputs in order to maintain signal integrity, in this case, we need ~90 dB to cover the expected dynamic range (DR) of the signal without significant performance degradation. A fourth-order CT-DSM with the cascade of integrators feedforward (CIFF) structure shown in Fig. 3.1 is designed for this purpose. The CIFF structure is preferred because it only needs two feedback DACs (one for the first integrator, and another to compensate for time delay in the loop). Using an idealized MATLAB model, the expected signal-to-quantization noise (SQNR) of this structure is 96 dB for OSR = 100, which exceeds the target SNDR.

The circuit was realized in the TSMC 180 nm CMOS process. A fully-differential structure is used to minimize even-order distortion. Four cascaded OTA-RC integrator stages are implemented as popular used structure for continuous-time circuits, with

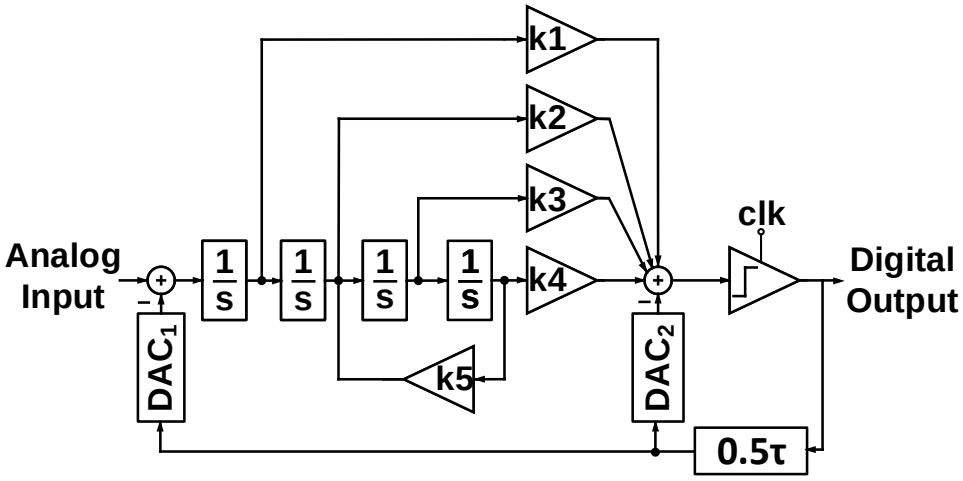


Figure 3.1. Block diagram of the proposed fourth-order CT-DSM with CIFF structure.

the fifth op-amp acting as the summing amplifier. Resistive feedback DACs are implemented in the first integrator and the summing amplifier stages to achieve the desired noise transfer function (NTF) and compensate for time delay in the loop. The performance of the first integrator stage, which usually limits the performance of the modulator, is improved using several methods, including i) feedforward compensation to increase op-amp bandwidth; ii) an assistant circuit based on an operational transconductance amplifier (OTA) and DAC that steers currents from the feedback DAC and input signal to the first-stage output, thus reducing the output current requirements of the first op-amp[21]; and iii) chopping to minimize $1/f$ noise and offset.

## 3.1 Model-Building and Performance Simulation in Simulink

To achieve the circuit design for the proposed CT DSM system, a Simulink model using the Delta-Sigma Modulator (DSM) Toolbox is built with MATLAB. Fig. 3.2 shows a fourth order CT-DSM implementing the CIFF structure in Simulink. The frequency of the input

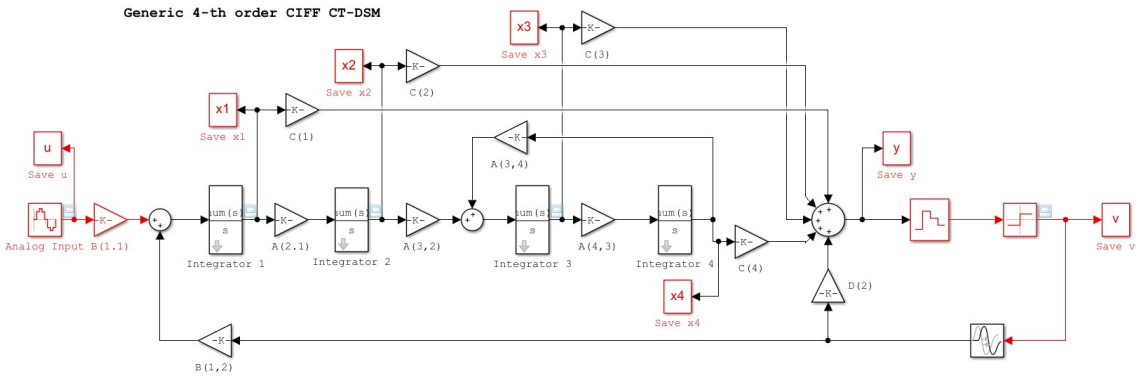


Figure 3.2. Simulink model of a 4th order continuous-time delta sigma modulator with CIFF structure.

signal is set to 500 kHz and the sampling frequency is chosen as 100 MHz, which leads to the desired over-sampling ratio (OSR) of 100. With the help of the DSM Toolbox, the parameters in the model are optimized according to the target signal transfer function and noise transfer function. The simulated performances of the proposed model are shown in Fig. 3.3. Fig. 3.3(a) is the impulse response of the loop filter , which verifies that the sampled pulse response of the CT loop filter matches the impulse response of the DT prototype. Fig. 3.3(b) shows the simulated outputs of each stage, which are scaled to lie within a limited range to avoid large internal swings and prevent premature saturation of internal states. The peak SNQR occurs when the input voltage is 500 mV, and its peak value is 96 dB. The optimization code and the circuits parameters calculation are attached in the Appendix.

## 3.2 Circuit Design of the Fourth-Order Continuous-Time Delta Sigma Modulator

This section mainly gives circuit details of the proposed CT-DSM, including the circuit architecture, operation principle, and simulation performance.

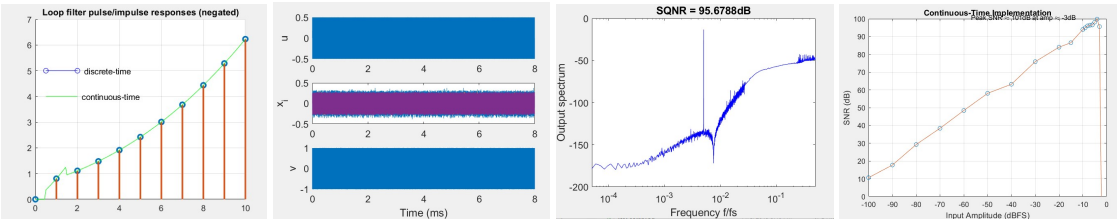


Figure 3.3. (a) Loop filter impulse response; (b) scaled output; (c) simulated peak power spectrum density (PSD) of the whole system; (d) SQNR of the continuous-time implementation as a function of the input amplitude.

### 3.2.1 Fully-Differential Op-Amp Design with Feed-Forward Compensation

The block diagram of the feedforward compensated op-amp used in the first integrator is shown in Fig. 3.4(a). The OTAs $G_{m1}$ and $G_{m2}$ are cascaded to achieve high DC gain, while the OTA $G_{m3}$ provides a high-speed compensation path. Compared to Miller compensation, feedforward compensation is more power efficient because no compensation capacitor needs to be charged and discharged. Meantime, The $G_{m3}$ branch introduces a positive phase shift (due to an LHP zero) to compensate the negative phase shift due to the poles.

The schematic of the complete op-amp is shown in Fig. 3.4(b). In the first stage, long channel transistors $M_{1-2}$ and $M_{7-8}$ are used in the input pair and mirrors to reduce $1/f$ noise; they are cascoded by $M_{3-6}$. Transistors $M_{12-14}$, which are minimum-length to reduce parasitics, form a common-mode feedback (CMFB) circuit that sets the desired output common-mode (CM) voltage for the first stage. The CMFB takes a third of the tail current in the first stage, and it does not degrade the DC gain since transistors rather than resistors are used to detect the CM output voltage. Since $M_{12-13}$ and $M_{17-18}$ share the same $V_{GS}$, it is easy to control the bias current used in the second stage by proper device sizing. To push the second op-amp pole associated with the second stage to higher

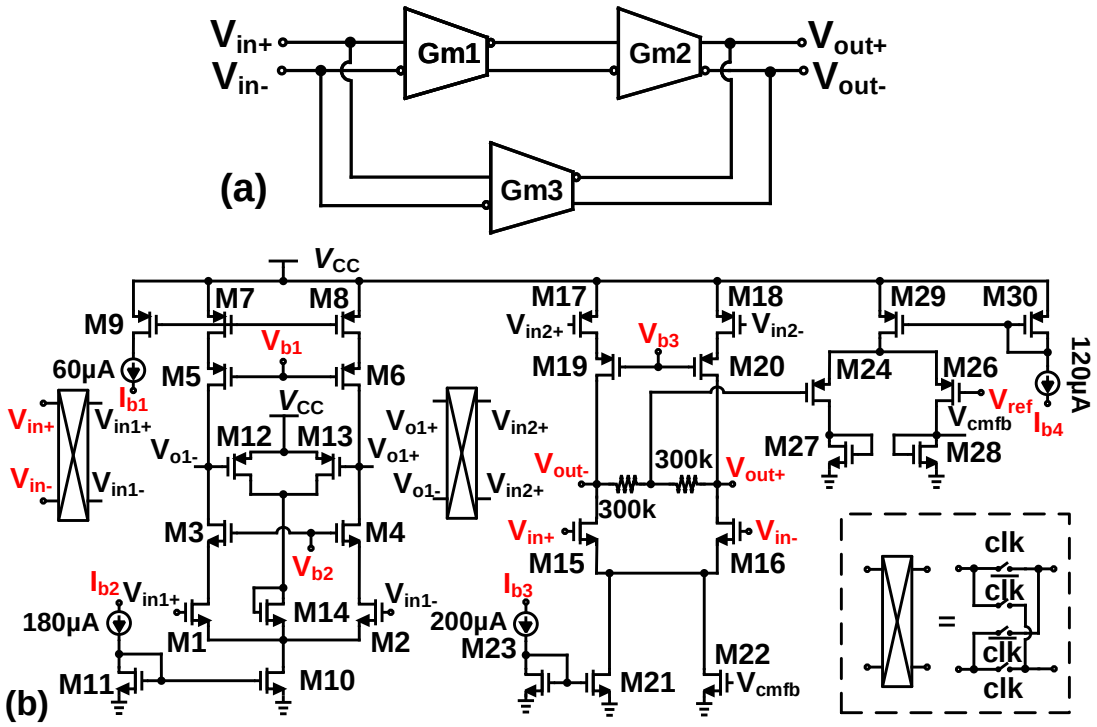


Figure 3.4. (a) Block diagram, and (b) schematic of the proposed feedforward-compensated op-amp. The first-stage OTA (denoted by $G_{m1}$) is chopped.

frequencies, the bias current at the second stage is set larger (150 $\mu$A) compared to the first stage (60 $\mu$A). Transistors $M_{15-16}$ are used for feedforward compensation, and they reuse the bias current of the second stage to save power. The op-amp's output CM voltage is set by another CMFB circuit, with two resistors detecting the CM voltage, and an error amplifier setting the desired DC output value. The tail current is broken into two parts ($M_{21}$ and $M_{22}$) with a 2:1 ratio to ensure the current sourced by the PMOS transistors equals the current sunk by the NMOS transistors; this also reduces the CMFB loop gain and therefore makes the CMFB loop more stable. Simulations of the proposed op-amp using foundry-supplied device models show a DC gain (open-loop) of 76 dB and the corresponding phase margin (PM) of 80°, a unity-gain frequency of 2 GHz, and the

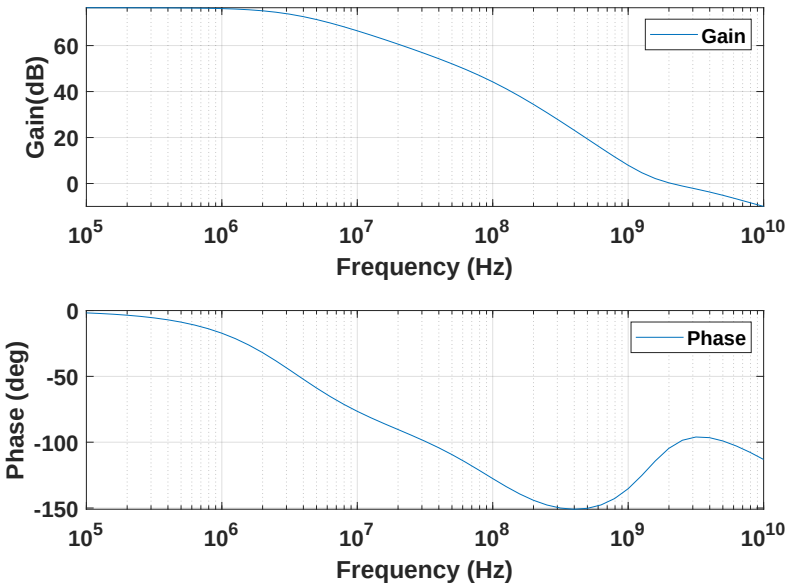


Figure 3.5. The AC simulation results of the proposed op-amp: Open-loop gain arrives at 76 dB, gain-bandwidth product is 2 GHz, and the corresponding phase margin is 80°.

gain-bandwidth product is 2 GHz. The AC simulation results are shown as Fig. 3.5. In addition, close-loop simulation with unity-gain feedback was implemented. The input amplitude was swept to find the total harmonic distortion (THD); the input linear range is 550 mV for < 2% THD.

### 3.2.2 Feedback DAC - Resistive DAC

The feedback block plays an significant role in the closed-loop transfer function of a negative feedback system. In this case, the performance of the proposed CT-DSM is dependent on the noise and linearity of the feedback DAC. This thesis implements a resistive DAC as the feedback, shown as Fig. 3.6. When the Vref,p is equal to Vdd, and switch D is equal to 0, the injecting current is fed into the integrator; conversely, when the Vref,m is equal to 0 and switch D is equal to 1, the current is fed to ground.

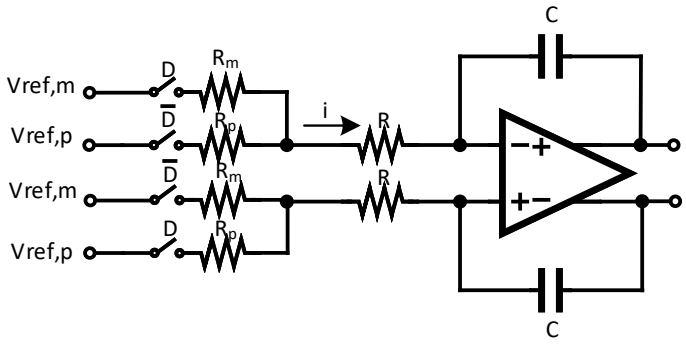


Figure 3.6. The schematic of the resistive DAC used to provide feedback to the loop filter.

### 3.2.3 Assisted Circuits and Chopping Technique for the First Integrator

The proposed CT-DSM uses a clock frequency of $f_s$ = 100 MHz clock to provide enough OSR and SQNR, as mentioned above. The difficulties in using such a high clock frequency to obtain the desired NTF include i) large currents in the feedback DAC; and ii) large currents through the input resistor, since these must be sized to be relatively small in order to minimize the modulator's input-referred noise. Such large currents ultimately need to be sunk/sourced by the input op-amp, which puts stringent slew-rate requirements on the op-amp design and can strongly affect the linearity of the first integrator. A common technique to address this issue is to add a class-AB buffer as a third stage in the op-amp; however, the extra circuitry consumes power and can degrade stability by creating additional high-frequency poles. Instead, the proposed CT-DSM uses an extra "assistant" circuit to reduce the op-amp's current source/sink requirements[?]. This circuit, which includes an assistant DAC and an assistant OTA, is connected to the output of the first integrator, as shown within the dashed box in Fig. 3.1. The assistant DAC is a replica of the modulator feedback DAC, but is biased with a larger current in order to compensate for the current flowing through the parasitic capacitances at the

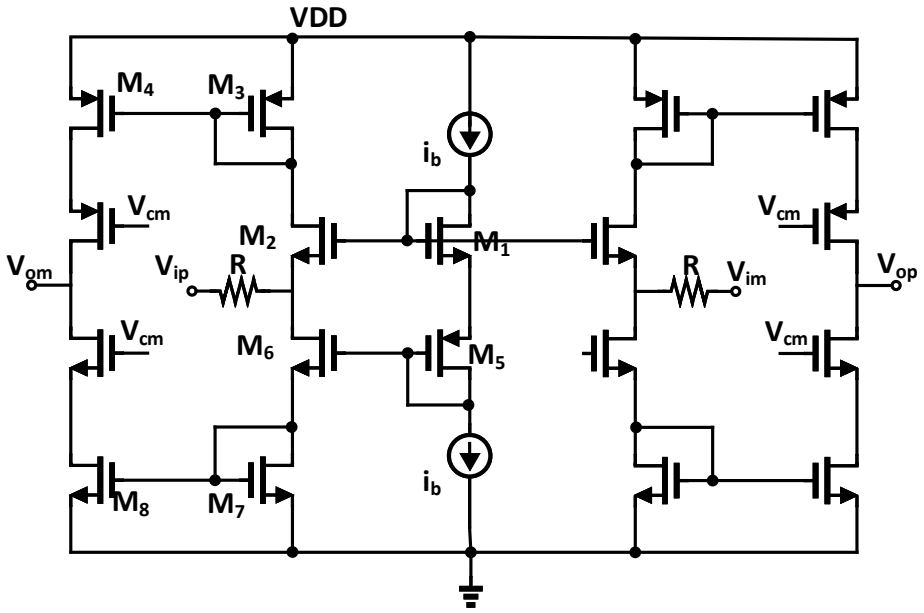


Figure 3.7. The schematic of the assisted OTA for the first integrator

op-amp output terminal. The assistant OTA is biased such that $G_{m,asstd} = 1/R_1$; this ensures that the current flowing through the input resistor $R_1$ is entirely supplied by the assistant OTA. The OTA's schematic is shown in fig. 3.7. As a result, the op-amp behaves nearly ideally even under large-signal conditions.

The conventional method for reducing the input-referred $1/f$ noise and DC offset of the first amplifier is to increase the size of the devices in the input pair, but this increases parasitic capacitance, which in turn creates an additional pole in the op-amp transfer function and thus reduces its phase margin. Instead, we use chopping to decrease the modulator's $1/f$ noise, offset, and sensitivity to temperature changes, aging, and other sources of low-frequency drift. As shown in Fig. 3.4(a), only the first-stage OTA $G_{m1}$ is chopped. This is because flicker noise generated by $G_{m2}$ and $G_{m3}$ is divided by the gain of $G_{m1}$ when referred to the input, making it negligible in the signal band. However, chopping within CT-DSMs comes with two main disadvantages[?]. The first is that

aliasing of high-frequency-shaped quantization noise into the signal bandwidth tends to degrade the modulator's SNDR. The second is that switches in the chopping circuit combine with parasitic capacitances $C_p$ to form switched-capacitor resistors that degrade the gain of the first-stage OTA by loading its outputs. To minimize these issues, a chopping frequency $f_c = f_s/2$ is chosen, where $f_s$ is the DSM's clock frequency, because this eliminates in-band noise due to aliasing[?] . In addition, i) chopping clock edges are set to the middle of the DSM sampling clock phase in order to maximize available settling time, and ii) minimum-sized transmission gates are used in the chopping circuit to reduce charge injection.

### 3.2.4 High-Speed Comparator and Access Delay with D Flip-flop

The proposed CT-DSM uses a StrongARM comparator (shown in Fig. 3.8) as a single-bit quantizer. When $clk$ is low, the comparator is in its reset state, with the differential pair turned off and all nodes above the differential pair pulled to $V_{dd}$. When $clk$ is high, the current in the differential pair activates $M_3$ and $M_4$, and the current imbalance from the differential input is amplified by $M_6$ and $M_7$ until either $\overline{R}$ or $\overline{S}$ goes low, therefore setting the RS latch to the result of the comparison. To improve the speed of the comparator, the input pair $M_1$ and $M_2$ are minimized to get a high slew rate. The impulse response of the comparator is shown as fig. 3.9. The settling time is 0.2 ns, which is much less than half of the sample clock cycle.

In reality the comparator needs a non-zero time to resolve its analog inputs, so the output sequence of the modulator is only available after a delay. The delay $t_d$ of the DAC clock with respect to that of the comparator should be large enough to compensate for such comparator delay. Because of the existence of this time delay $t_d$ (here we use

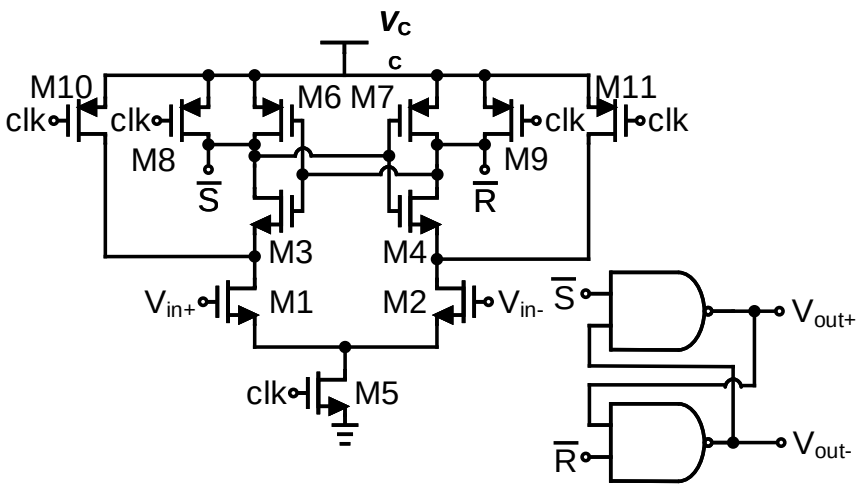


Figure 3.8. Schematic of the StrongARM comparator.

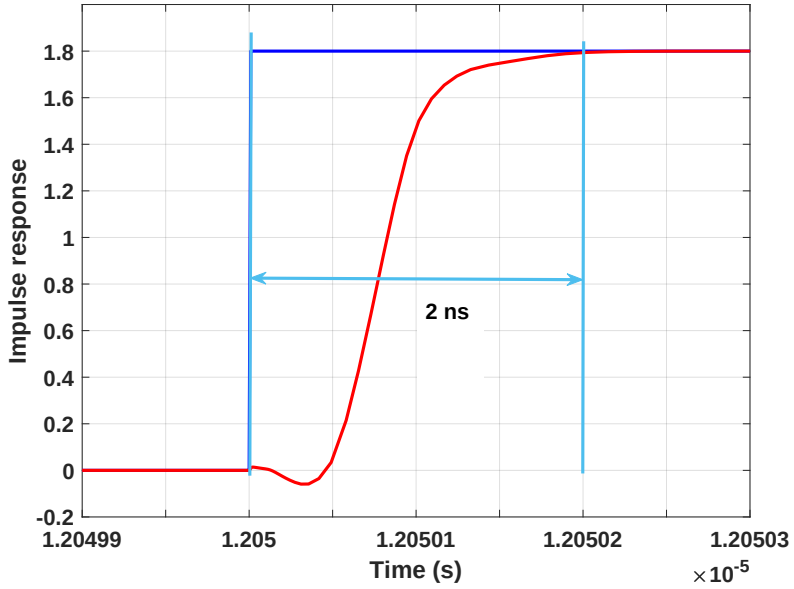


Figure 3.9. Impulse response of the comparator: settling time is 0.2 ns.

$t_d = \tau/2$, where $\tau = 1/f_s$ is the clock period), excess phase shift is generated in the closed-loop and the system becomes more unstable. An easy way to address this issue is to add a feedback path directly across the quantizer to restore the loop's NTF. This additional path (denoted by $DAC_2$ in Fig. 3.1(a)) adds a zero to the loop gain, thus stabilizing the system. Our modulator design thus uses two one-bit non-return-to-zero (NRZ) resistive

DACs: the first one feeds into the first integrator to achieve the desired NTF, while the second one feeds into the summing amplifier to compensate for loop delay. Note that our choice of a one-bit CT-DSM simplifies the design by eliminating the need for multi-bit DACs with additional mismatch shaping circuitry.

## 3.3 Front-End Circuits Design

The radio-frequency (RF) signal, which comes from a 3T MRI scanner, is typically ±500 kHz centered around the carrier frequency 123.3 MHz. So a mixer circuit is necessary to do the down-conversion operation and generate a baseband signal. The down-conversion operation of a mixer is shown as Fig. 3.10. When the radio frequency $f_{RF}$ is fed into the mixer, a local oscillator provides a close frequency $f_{LO}$, then the output is the intermediate frequency $f_{IF}$, which is defined as $f_{IF} = \left| f_{LO} - f_{RF} \right|$. The amplitude of the RF signal in the MRI scanner is 0 dBm, which corresponds to a voltage of about 600 mV peak-to-peak in a 50 Ω load. Passive mixers are widely used for high-linearity applications because of their simplicity, good intermodulation distortion (IMD) and better isolation between the signal ports. Given the high linearity requirement of this design, a passive single-balanced mixer is chosen, as shown as Fig. 3.11. The transmission gate switch is controlled by $f_{LO}$ and a capacitor is applied as load. When the switch is turned off, the output voltage IF is held on the load capacitors instead of letting them fall to zero. In addition, the switch-on resistance $R_{on}$ can be calculated from the simulation, and then the capacitor value can be optimized according to the desired cut-off frequency. Meantime, the mixer can also convert the signal from single-ended to its differential counterpart. An off-chip programmable gain amplifier (PGA) based on a commercial op-amp is

added following the mixer to adjust the output amplitude that will be fed into the delta sigma modulator as its input signal.

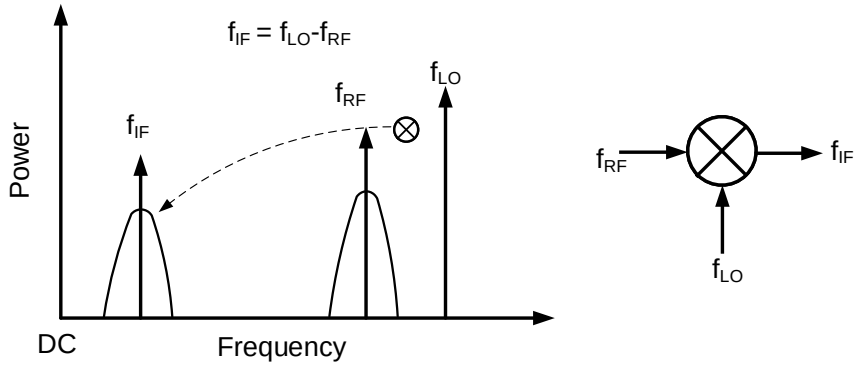


Figure 3.10. Down-conversion operation of the mixer.

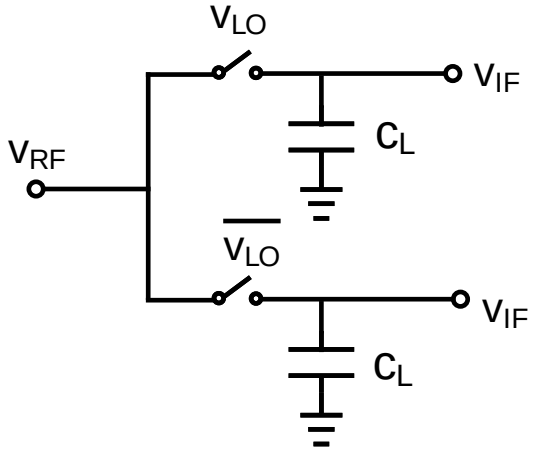


Figure 3.11. Schematic of the passive single-balanced mixer.

## 3.4 Serial Peripheral Interface (SPI) control for the feedback capacitor DACs of the integrators and clock system

Considering the significance of the RC constant to achieve the ideal signal transfer function and the effect of the process variation and mismatching between devices, the feedback capacitor is made of a fixed main value capacitor and six variable unit value capacitors with programmable switches, which are controlled over a standard serial peripheral interface (SPI) bus. The unit switched-capacitor value is set by the standard deviation value of Gaussian distribution of the capacitor, which comes from the Monte Carlo simulation.

The SPI control block with address and the signal's timing diagram are shown in Fig. 3.12. The four input signals can be generated by an off-chip microcontroller such as an Arduino. The first block is a 25-bit shift register, which includes 24 data bits and 1 address bit. Its D-flip flops are triggered by the rising clock edges, and the latch is enabled by a high voltage level on the EN pin. A three-bit shift register circuit is shown in Fig. 3.13(a). The second and third blocks are programming circuits for two different channels with different addresses. The address bit is set to low level for channel 1 and high level for channel 2. When the shift register output sequence is fed in, the 25th bit is first compared with the two channel's addresses. If they match, the digital comparator's output goes high, thus generating the enable signal for the latches. As a result, the 24 data bits can be transferred using the serial clock $CLK$ and stored in the correct latches. A three-bit programming circuit is shown in Fig. 3.13(b).

There are two clocks in this delta sigma modulator system: sampling clock (100 MHz) and chopping clock which is the half of the sampling frequency. To synchronize these

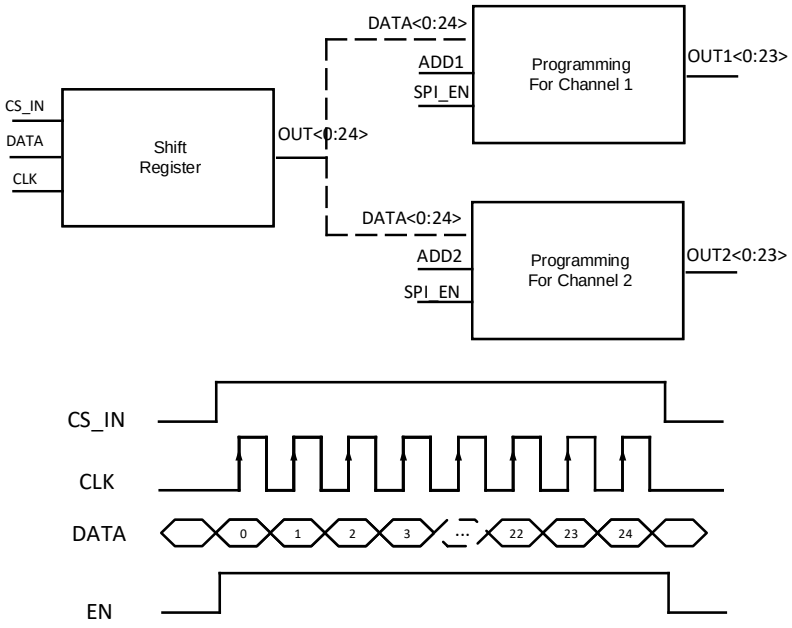


Figure 3.12. SPI control block and timing diagram.

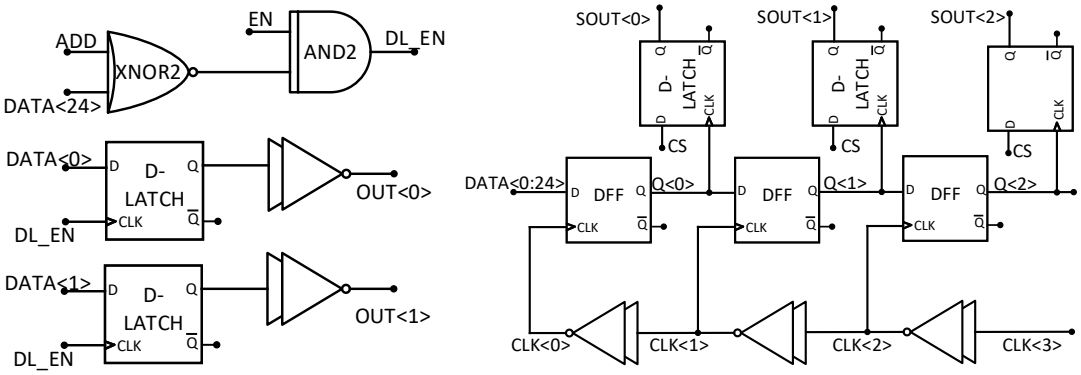


Figure 3.13. SPI control circuits:(a) Three-bits shift register circuit;(b) Three-bits programming circuits for one channel.

two clocks, a clock generator circuit is designed shown as Fig. 3.14. A popular frequency division structure is chosen.

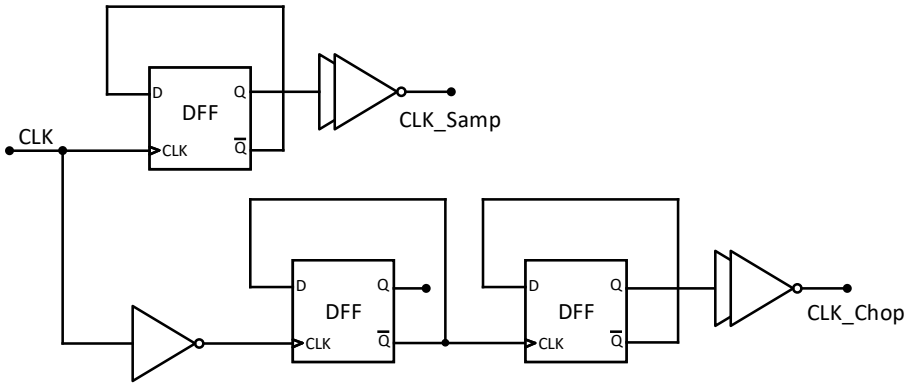


Figure 3.14. Clock system and timing diagram for the delta sigma modulator

## 3.5 Simulation Performance of the Whole System

The high-level schematic of the whole circuit is shown in Fig. 3.15. Simulated op-amp performance with/without chopping is compared in Table. 3.1 and Fig. 3.16. Both simulations used the same open-loop op-amp test bench but with the chopping clocks enabled/disabled, respectively. Fig. 3.16(a) shows that chopping greatly reduces the input-referred noise at low frequencies as expected, with the $1/f$ corner frequency decreasing from 1 MHz (without chopping) to 2 kHz (with chopping). Although chopping is beneficial for noise performance, the DC gain of the op-amp suffers because of the switched-capacitor resistor load formed by the transmission gate switches in the demodulator and parasitic capacitance $C_p$ present at the output of the first OTA. Fig. 3.16(b) shows a DC gain loss of 20 dB when the chopping frequency $f_c$ is set to its default value of 50 MHz. Reducing $f_c$ increases the switched-capacitor resistor value $1/\left(f_s C_p\right)$ and therefore improves the op-amp's open-loop gain. However, at such low values of $f_c$, aliasing of shaped-noise into the passband affects the modulator's noise floor, and complicated DAC structures (e.g., finite input response [FIR] DACs) are required in order to recover SNDR.

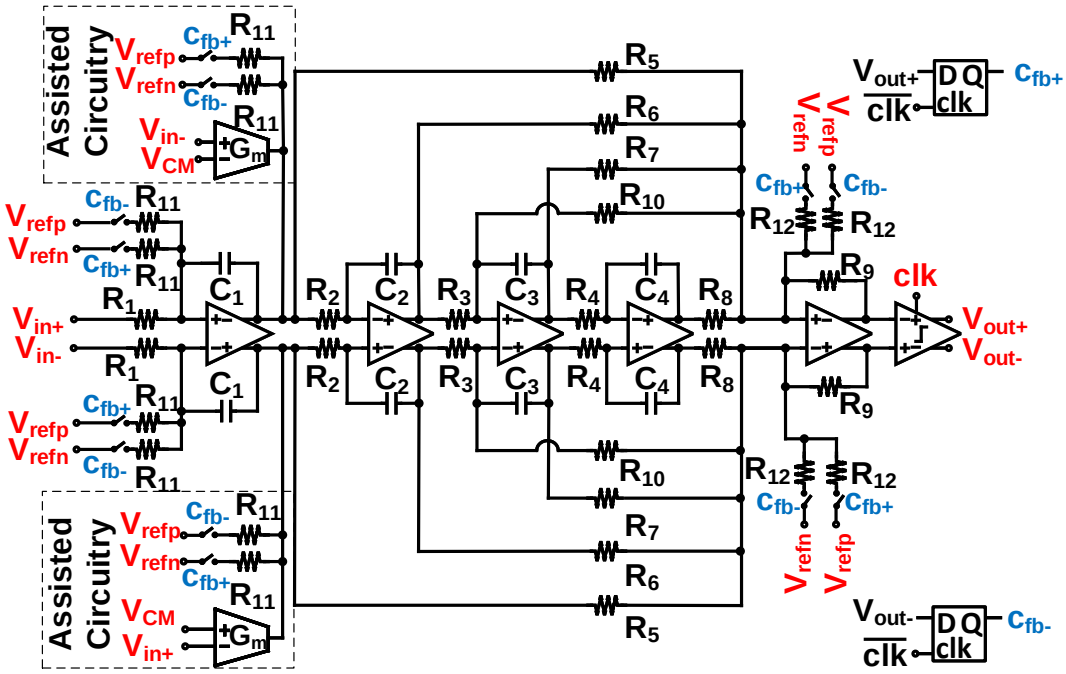


Figure 3.15. High-level schematic of the whole circuit.

Table 3.1. Op-amp performance comparison with/without chopping

| | Gain | Unity-gain frequency | Corner frequency | Peak SNDR | Power |
|---|---|---|---|---|---|
| Chopping | 74 dB | 1 GHz | 2 kHz | 89.3 dB | 1.7 mW |
| No chopping | 94 dB | 3 GHz | 1 MHz | 85 dB | 1.7 mW |

Fig. 3.17(a) shows the simulated SNDR of the proposed CT-DSM versus input amplitude for sinusoidal inputs with chopping enabled. Transient noise was enabled during the simulations in order to capture the effects of both thermal and $1/f$ noise. The maximum SNDR of 89.3 dB is obtained at an input amplitude of $-2.2$ dBFS, corresponding to an effective number of bits (ENOB) of 14.5. The total power consumption is 8.8 mW, resulting in a Walden figure of merit (FoM) of 360 fJ/bit. The simulated SNDR is also in excellent agreement with the idealized system in MATLAB, which was designed to have maximum SQNR = 96 dB and SNDR = 89 dB.

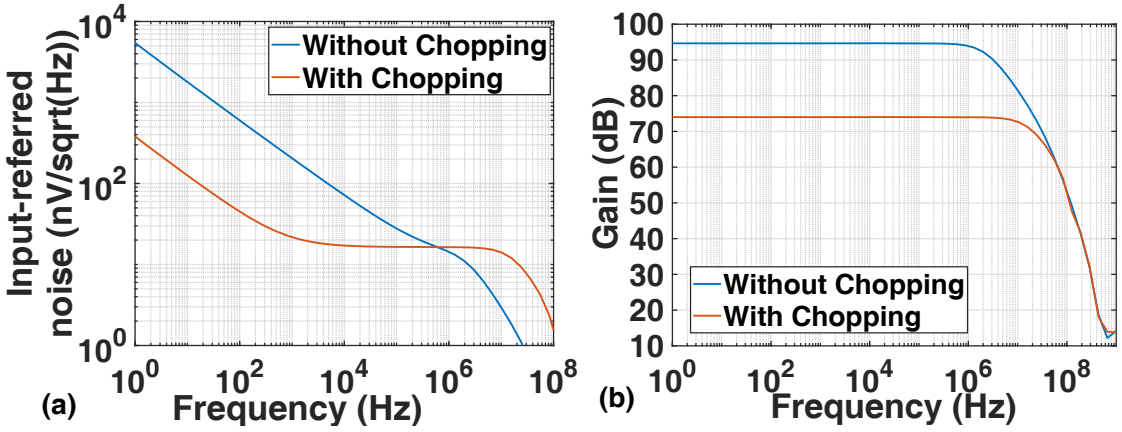


Figure 3.16. (a) Noise comparison for op-amp with/without chopping technique. The flicker noise corner is significantly reduced. (b) Reduced DC gain for op-amp with/without chopping technique.

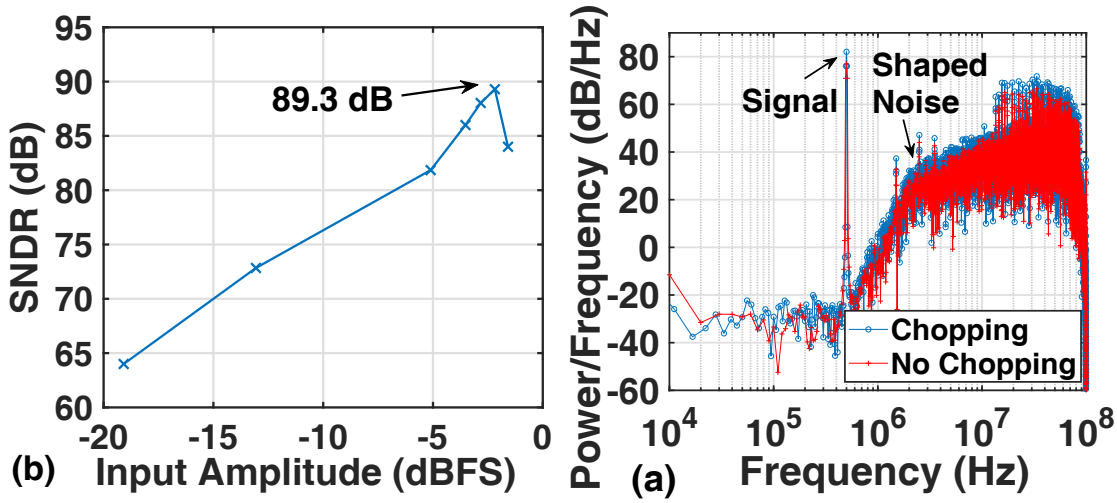


Figure 3.17. (a) Simulated SNDR of the modulator versus input amplitude with chopping enabled; the maximum occurs at −2.2 dBFS. (b) Simulated output PSD with a −2.2 dBFS sinusoidal input. Peak SNDR values of 89.3 dB (with chopping) and 85 dB (without chopping) are obtained.

Example output spectra for a −2.2 dBFS sinusoid input with and without chopping are shown in Fig. 3.17(b). The noise is clearly shaped out of the passband with a slope of 80 dB/decade, which confirms the functionality of the fourth-order noise-shaping structure. The SNDR with and without chopping is 89.3 dB and 85 dB, respectively. Thus,

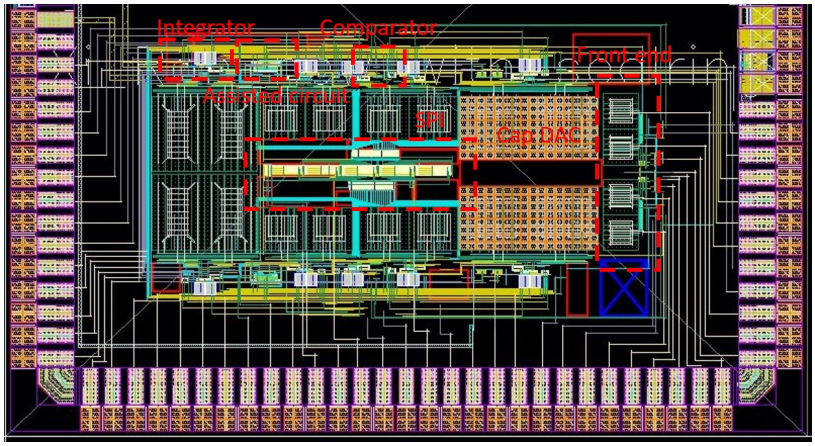


Figure 3.18. The top-level layout of the custom CT-DSM chip.

SNDR improves by 4.3 dB due to chopping, i.e., chopping slightly reduces the total in-band noise floor. The relatively small improvement implies that input-referred $1/f$ noise and thermal noise terms are comparable. In fact, it is easily verified that the thermal noise of the input resistive network (power spectral density (PSD) of 7.2 nV/Hz$^{1/2}$) is 5 $\mu$V total noise over the 500 kHz bandwidth, which is comparable to the op-amp's total input-referred noise (before chopping) of 5.6 $\mu$V over the same bandwidth. However, in reality it is important to minimize low-frequency drift due to temperature fluctuations and aging, so chopping is valuable for improving CT-DSM performance.

The layout of the whole circuit in the TSMC 180 nm CMOS process is shown in Fig. 3.18.

# 4 Experimental Results

This chapter mainly discusses the test performance of the chip. The chip was fabricated in TSMC 180 nm CMOS process by Muse Semiconductor. The microscope-photograph of the whole die is shown in Fig. 4.1, which has an active area of 2486 $\mu$m x 1514 $\mu$m. The die is wire-bonded by Quik-Pak using a 120L 14 × 14 LQFP package.

The custom printed circuit board (PCB) as the chip testbench is shown in Fig. 4.2, which was designed in Altium Designer. The detailed schematic and layout of the PCB can be found in the appendix. All DC bias currents and voltages are provided by the potentiometers, which are located to the custom chip closely. Two different value bypass capacitors are added to all routing of DC sources to bypass AC noise and provide a stable

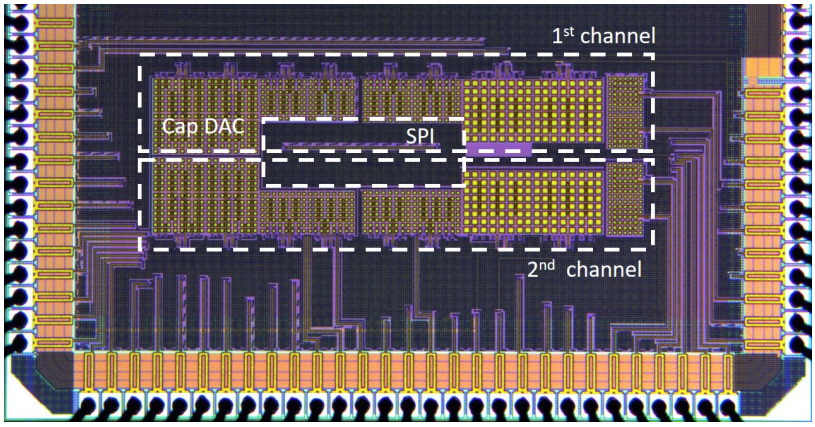


Figure 4.1. Die photograph of the custom chip.

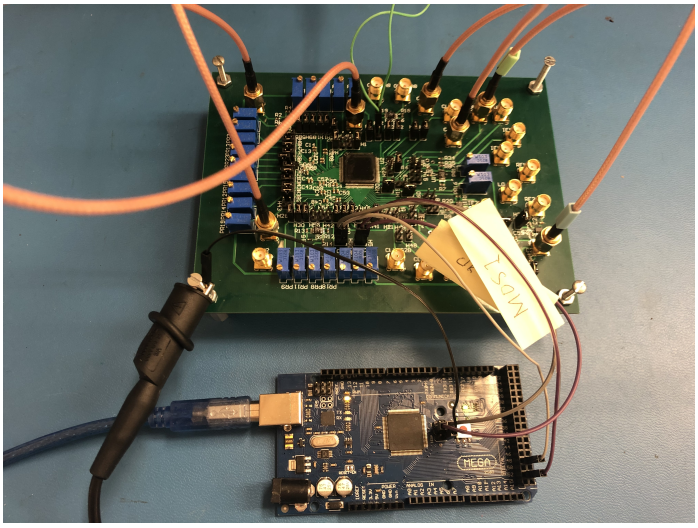

Figure 4.2. Test board setup for measuring the custom chip.

and accurate DC value for the custom chip. To shorten DC routing distance, parts of the bypass capacitors are soldered underneath of the chip, on the back of the test board. Considering the process variation occurred during the fabrication, multiple I-V curve sweeps are given separately for each bias transistor on the chip with a Keithley 2450 source meter to provide the required bias currents for the chip. Then it is easy to find the corresponding voltage of the desired bias current and set it by adjusting the value of the potentiometer. The I-V curve used to set the reference current (50 $\mu$A) for the current mirror of the on-chip op-amp is shown as Fig. 4.3.

The parameters for all DC setting-up are listed as shown in Table. 4.1. All the bias voltages are provided by the potentiometer. A function generator (Tektronix) is used as the base-band RF signal and Keithley source meters are used to source the designed voltage (like VDD, supply voltage for the LDO) for the test board. For testing convenience, there are optional function buttons designed on the chip which are listed in Table 4.2. The whole circuit runs with a current of 2.8 mA, leading to a power consumption of 5 mW.

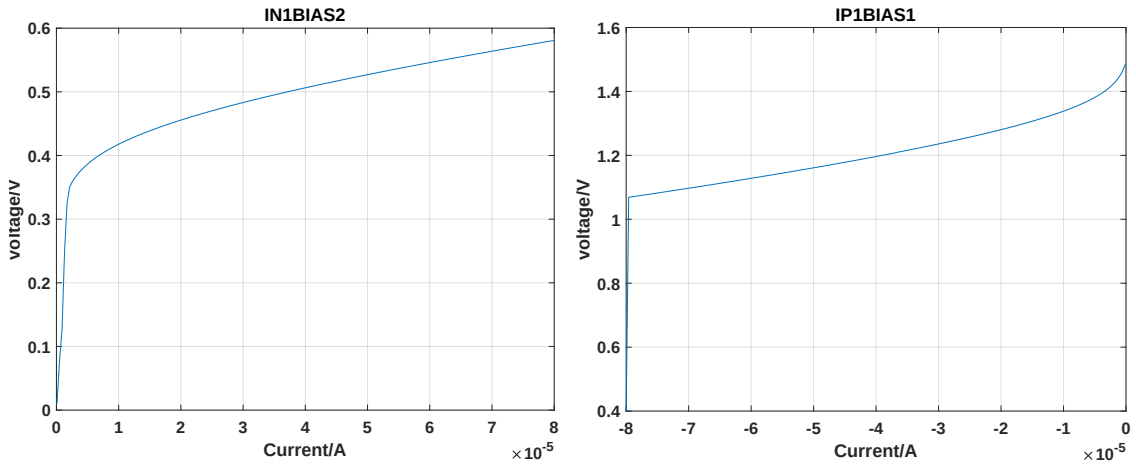


Figure 4.3. The measurement I-V curve used to set the reference current for the bias current (50 uA). This curve is obtained by using a Keithley source meter.

Table 4.1. DC Setting-up Parameters

| Power Suply | Reference Voltage | Bias Current | VBP2 | BP4 |
|---|---|---|---|---|
| 1.8 V | 900 mV | 50 $\mu$A | 400 mV | 510 mV |
| VBN1 | CASCP | CASCN | NB | NBC |
| 1.1 V | 300 mV | 1.2 V | 603 mV | 1.2 V |

Table 4.2. Test Parameters

| Chopping_EN | | Feedback_EN | | 1st Integrator Output | |
|---|---|---|---|---|---|
| 0 | chopping | 0 | with feedback | 0 | off |
| 1 | no_chopping | 1 | without feedback | 1 | on |

## 4.1 Performance Test

### 4.1.1 SPI Control Signal and the Clock System

As mentioned in the last chapter, the feedback capacitor's value for each integrator is controlled by a serial peripheral interface (SPI) bus. In this test, we use the Arduino Mega as the microcontroller to achieve this synchronous serial data communication with the chip. The selected ports are MOSI (Master Out Slave In), SCK (Serial Clock), and two

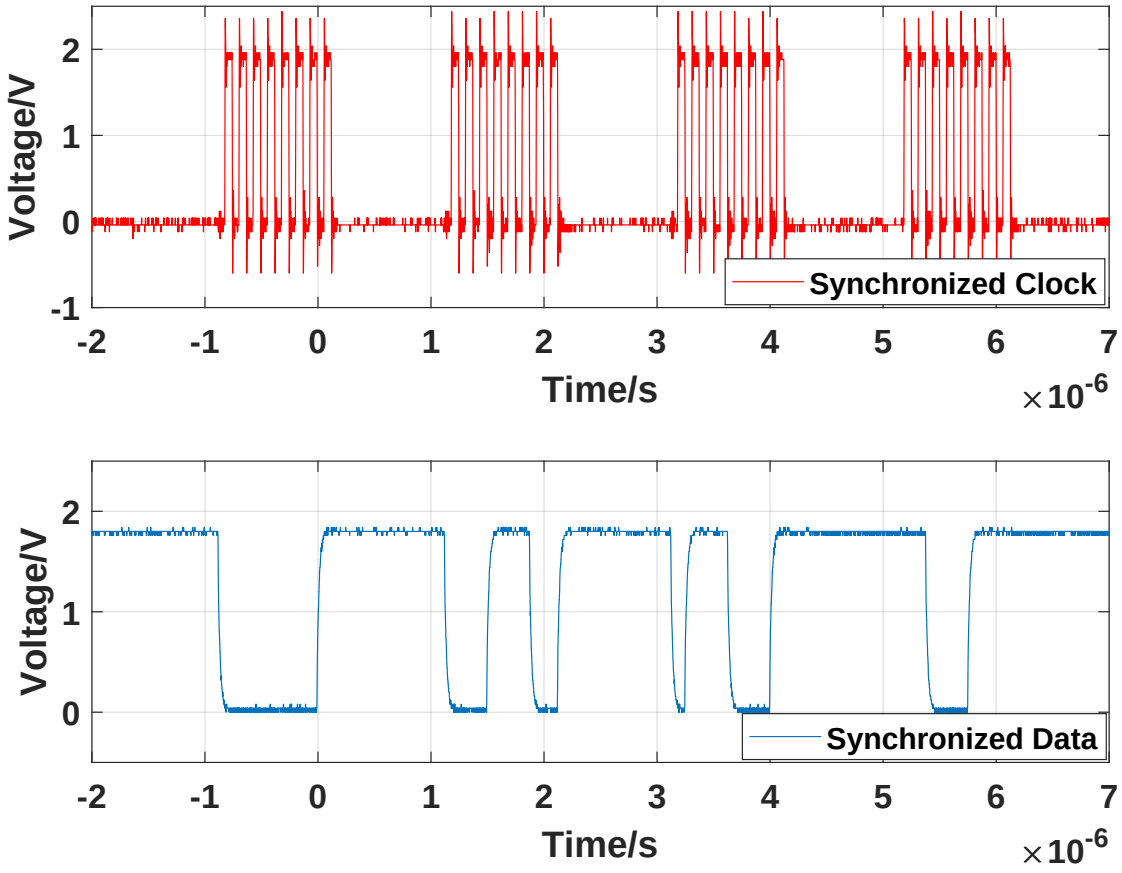


Figure 4.4. The recorded output sequence from the Arduino. Sample clock is set to 8 MHz, and the synchronized data is the required initial value for the capacitor DAC.

extra enable ports (53 and 49). The clock pulse which synchronizes data transmission is set to 8 MHz and the serial data is shifted from the least significant bit (LSB). The microcontroller's output as required is recorded by the oscilloscope, shown as Fig. 4.4.

The recorded sequence of the on-chip clock system is shown in Fig. 4.5, which runs at a clock frequency 20 MHz for the clock divider. The generated sample clock (red one) is 10 MHz and the chopping clock (blue one) which is set to half of the sampling clock is 5 MHz.

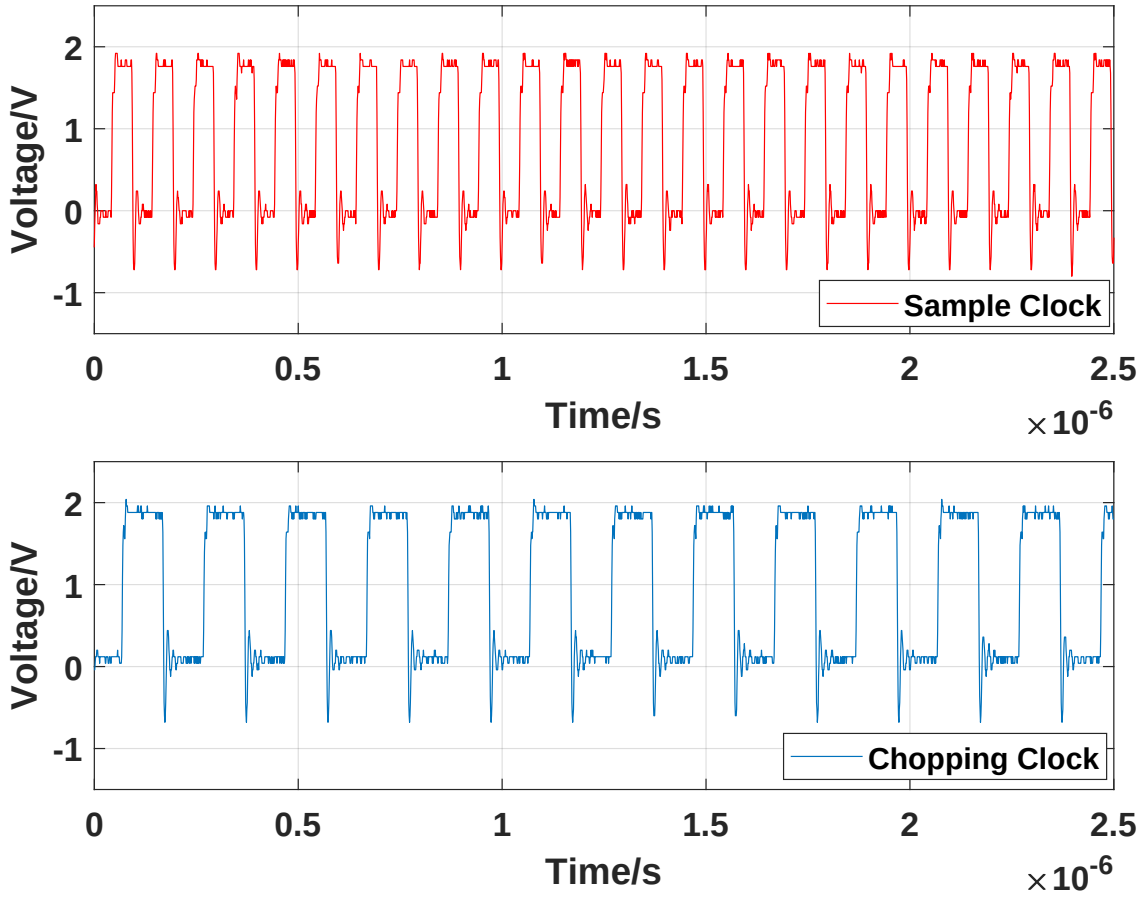


Figure 4.5. A recorded output sequence from the on-chip clock system. The sample clock is 10 MHz and the chopping clock is 5 MHz.

### 4.1.2 Delta-Sigma Modulator Performance

The first integrator, as the main source of noise, plays a significant role in the whole circuits. Two class AB buffers are inserted at the output of first integrator inside of the chip, so that the scaled output of the integrator can be observed through oscilloscope. Meantime, the common-mode voltage of the op-amp can be checked at this test point to verify the operation of the op-amp, which can strongly affect the performance of first integrator. In addition, The DC voltage at this output can be seen as a reference when the adjustment of the bias current is given to the op-amp. The first integrator's output

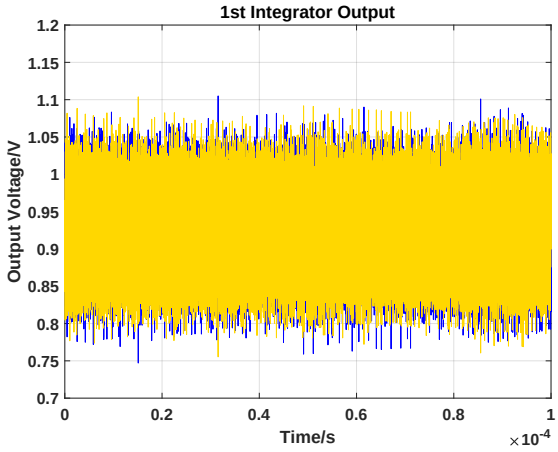


Figure 4.6. The recorded output for the first integrator.

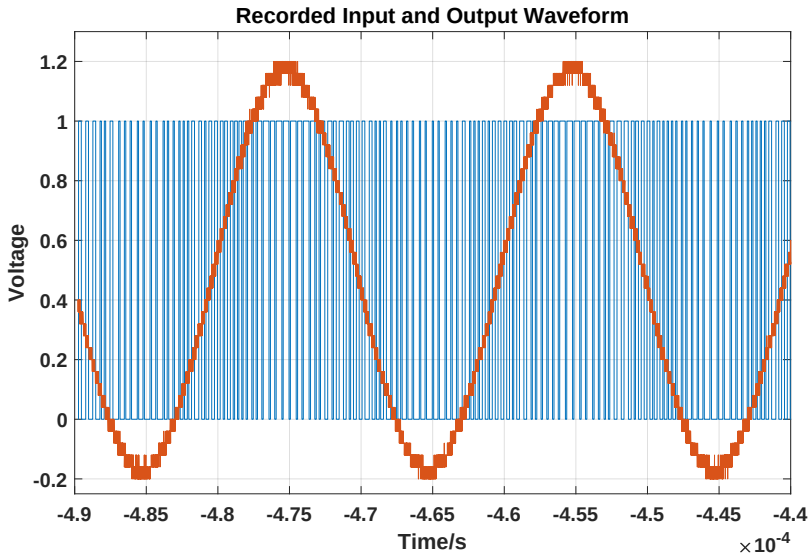


Figure 4.7. The recorded input signal and output sequence. Input frequency is 50 kHz, and sample frequency is 10 MHz.

is shown in Fig. 4.6. The measurement output voltage is limited in about 350 mV, which is about 300 mV in the simulation. The tested DC voltage of the output is 920 mV, which is close to the desired value for the op-amp's common-mode voltage, 900 mV. So the common-mode circuit for the op-amp works well in this chip and the first integrator output is successfully limited to the desired range as a good condition for next stage.

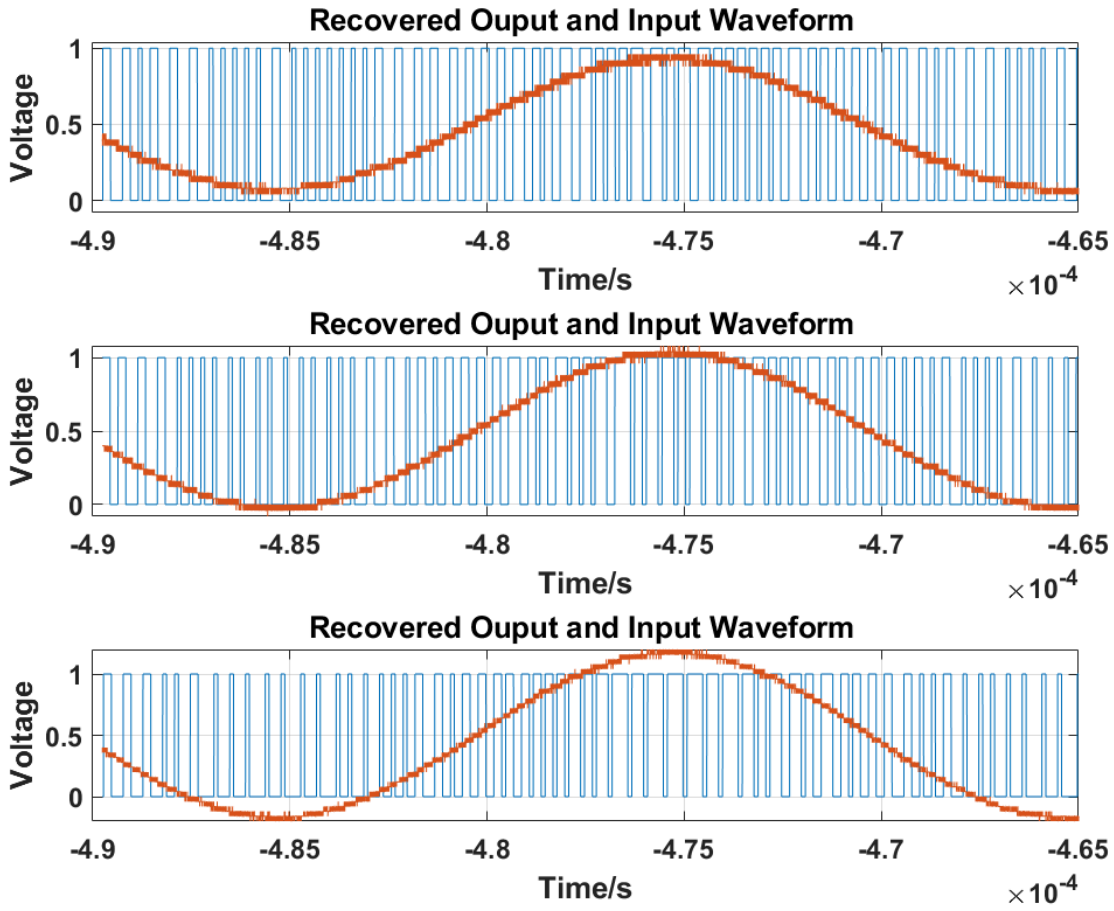


Figure 4.8. The recorded output sequence varies with the input signal's amplitude: 0.8 mV, 1 mV, 1.2 mV. Input frequency is 50 KHz, and sample frequency is 10 MHz.

The oscilloscope-recorded output of the comparator, namely the output of the whole system is shown in Fig. 4.7. As a reference, the input signal is observed too. It shows the achievement of delta sigma modulator's core function as an analog-to-digital converter. Fig. 4.8 shows different output waveform varies with the increased input voltage. We can see the output sequence saturates more and more in the center of the waveform with input voltage's increasing, which indicates increased signal power takes more percentage above the quantization noise.

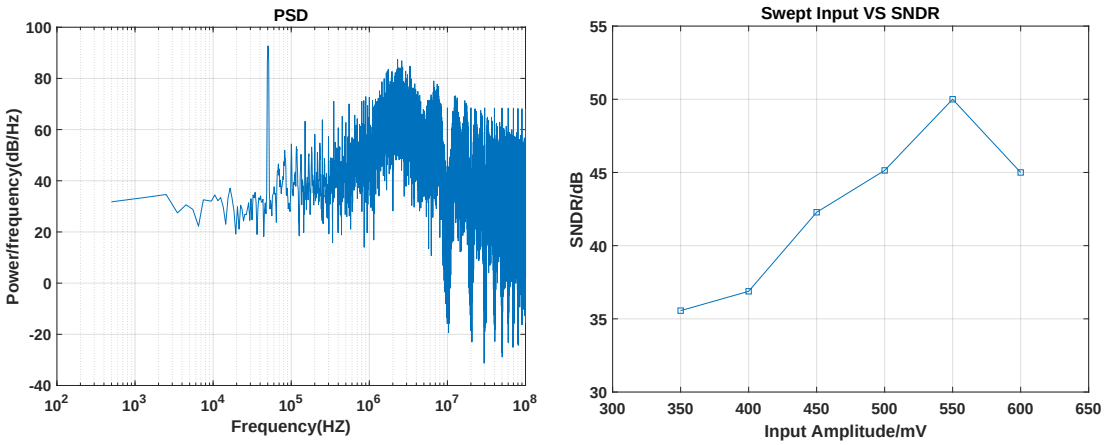


Figure 4.9. (a) The power spectrum density when input amplitude is 550 mV. (b) The swept SNDR with different input voltages from 350 mV to 600 mV.

When the chip runs with a sampling frequency of 10 MHz, and the input frequency is set to 50 kHz, namely with OSR of 100, the system has maximum signal to noise and distortion ratio (SNDR), which arrives at 50 dB with 550 mV input amplitude. The power spectrum density (PSD) of the output is shown in Fig.4.9(a). From the PSD, we can easily see the output signal's power spectrum density with the peak, and noise is compressed in low frequency and shaped out to the high frequency domain. The swept SNDR of the output variation with different input is shown in Fig. 4.9(b). The amplitude of the input varies from 350 mV to 600 mV. We can see the peak SNDR occurs at 550 mV and then starts to fall because of the increase distortion.

Shown in Fig. 4.9, the noise level is higher than the simulation result, which means more noise comes from the circuit. And the compressed noise is shaped out of the pass-band with a slope of 40 dB, which indicates that the worked order for the noise transfer function (NTF) is just two (instead of four), and that there is a deviation from the desired NTF. This is the dominant reason for the limited SNDR.

These results may be explained as follows. During this set of tests, the sampling frequency was set to 10 MHz, which is reduced by 10 times compared with the required sampling frequency (100 MHz) used in simulations. In this situation, the time constants of the on-board integrators should be increased by the same factor (10×) to maintain the desired NTF and SNDR. However, the SPI control for the capacitor DAC provides just 10% adjustment of the time constant (since it is designed only to compensate for process variations) and is therefore insufficient to compensate for the lower clock frequency. The detailed verification of this effect using both the Simulink model and circuit simulations will be given in the next section. The conclusion is that to obtain the desired SNDR, a CT-DSM should be run as close as to the desired sampling clock frequency; note that this constraint does not apply to a DT-DSM, whose loop filter transfer function simply scales with the clock frequency. In addition, the peak SNDR occurs when the input is 500 mV, while this is 750 mV in the simulation. The op-amp's real linear range is not ideal as the simulation, so the linearity of the op-amp also degrades the measured SNDR.

The chopping circuit helps improve the SNDR of the system as shown in Fig. 4.10, which compares the swept SNDR with and without chopping circuits following the variation of the input. It shows that the chopping circuit improves the SNDR around 10 dB. The comparison of the PSD with chopping and without the chopping circuit is shown in Fig. 4.10(b), when the input is 550 mV. The chopping one has a lower noise floor than the no-chopping counterpart, which indicates chopping technique improves the circuit performance by reducing low-frequency noise such as offset, $1/f$ noise, and temperature fluctuations. As a result, chopping is valuable in this application.

The swept SNDR for both CT-DSM channels on the chip has been tested, and they have similar performance as shown in Fig. 4.11.

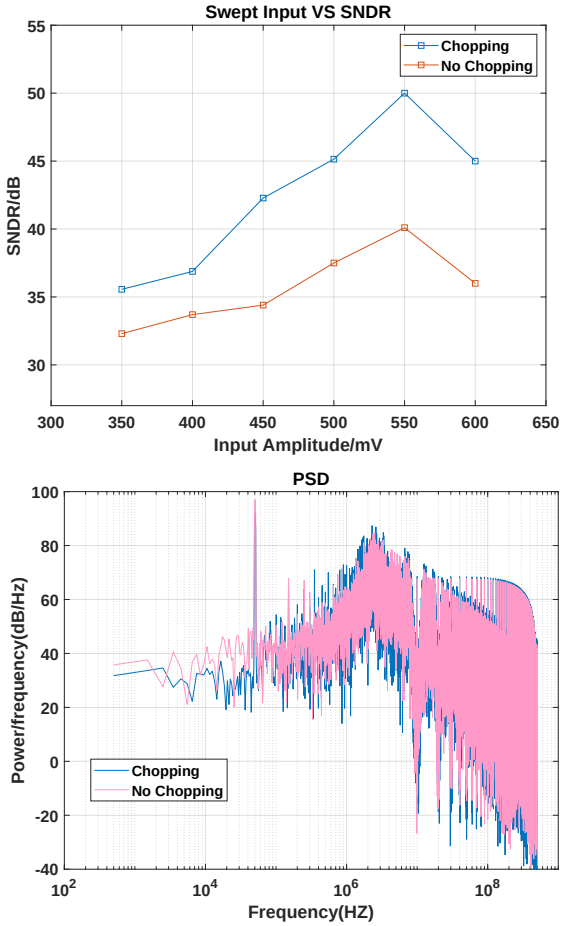


Figure 4.10. (a) Comparison of measured SNDR with chopping circuit and without chopping circuit; (b) comparison of PSD with chopping circuit and without chopping circuit at the maximum SNDR.

The recovered output signal is shown in Fig 4.12(a), which is applied with a roughly low-pass filter providing by the oscilloscope. To provide a better low-pass filter to recover the signal, the collected output is processed with a Butterworth low-pass filter in MATLAB, which can provide a frequency response as flat as possible in the passband. The comparison between the recovered signal from MATLAB and the input signal is shown in Fig. 4.12(b). This simple recovery of the signal is the advantage of using a

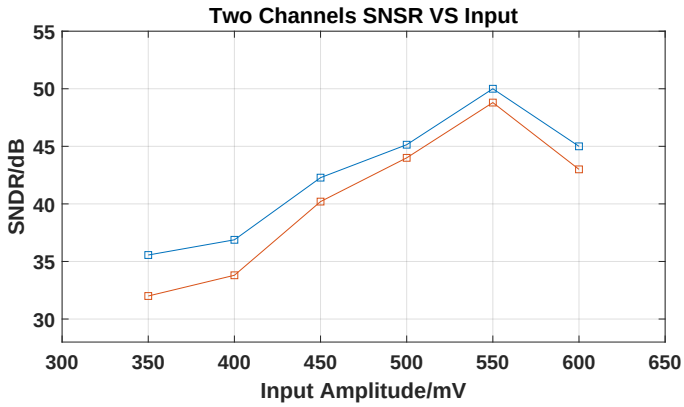


Figure 4.11. Measured SNDR of the two modulator channels versus input voltage.

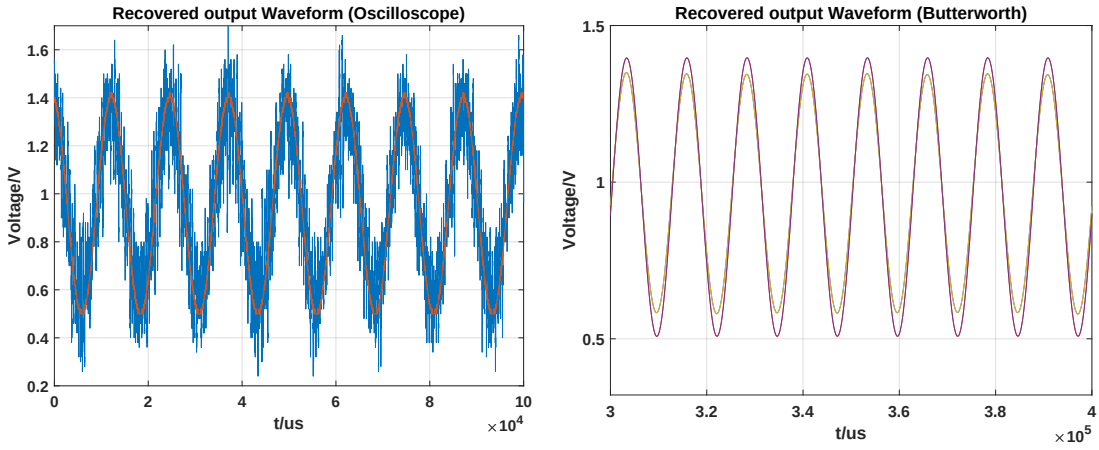


Figure 4.12. Comparison between the recovered output signal and input signal, which is (a) recorded by the oscilloscope; (b) after applying a Butterworth low-pass filter in MATLAB.

delta-sigma modulator: one does not require a DAC to convert the digital signal to analog signal at the receiver side, and the signal reconstruction can be easily performed by an analog low-pass filter component or directly processed by adding a low-pass filter on a digital platform. Thus, it simplifies the optical receiver design and enable a direct interface to legacy data acquisition equipment (e.g., commercial MRI scanners) that process analog inputs.

## 4.2 Simulation Verification and Performance Analysis

For this continuous-time (CT) delta sigma modulator design, RC integrators are cascaded to maintain the desired noise transfer function, in which the RC values are calculated from the time constant of the loop filter. With a fixed-value resistor which is calculated from the thermal noise requirements, the capacitor value is defined by the scaled time constant with the inverse of sample frequency. Therefore, the system should operate with the desired sample frequency to maintain the designed NTF. However, once the sample frequency changes, the NTF will be different. For example, if the sample frequency decreases by 2, the required time constant will increase by the same factor. This is completely different from the discrete-time (CT) delta sigma modulator, for which the loop-filter is in discrete-time (DT) form and thus has time constants naturally scaled as $1/f_{clk}$ since the value ($R$) of a switched-capacitor resistor is set by $R = 1/(f_{clk} \cdot C)$. Therefore, a DT delta-sigma modulator can be operated at any clock frequency (mainly limited by the settling time of op-amp) while maintaining the same NTF. However, this is not true for a CT delta sigma modulator unless the RC constants for each integrator can be scaled with $f_{clk}$. In this case, the tuning range of capacitors controlled by SPI is only 10% , which is largely insufficient to maintain the NTF with the reduction of $f_{clk}$.

Verification simulations with a low sampling clock frequency of 10 MHz were done using both the Simulink model and Cadence simulations as a proof-of-concept. The results correspond to the analysis above. The power spectrum density of the output when maximum SNDR occurs in Simulink model and cadence circuit is shown in Fig. 4.13. Maximum SQNR and SNDR are respectively 51.1 dB and 42 dB. Especially in Fig. 4.13(b), the simulation results closely match the test results: the noise level is between 20 dB to 40 dB and the slope rate of the noise shaping is 40 dB/decade. For low sampling clock

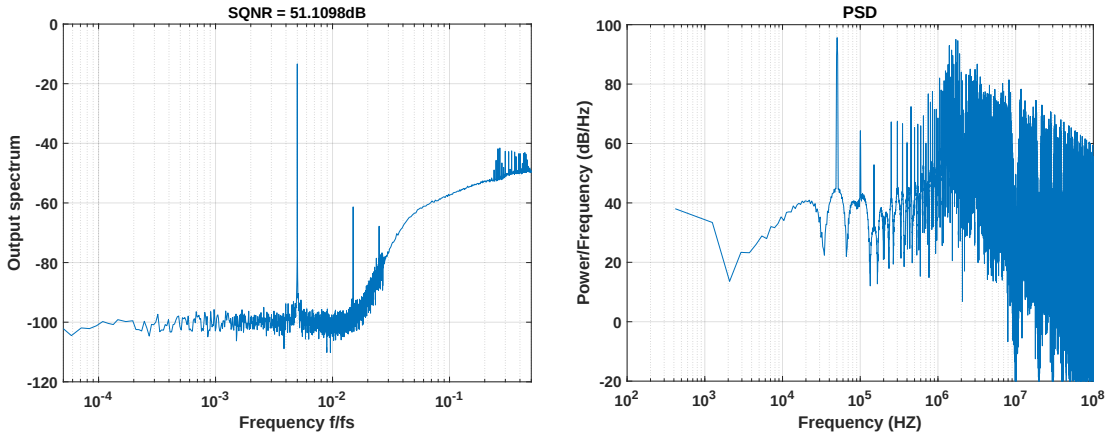


Figure 4.13. The power spectrum density of the output when maximum SNDR occurs in (a) Simulink model, and (b) Cadence circuit.

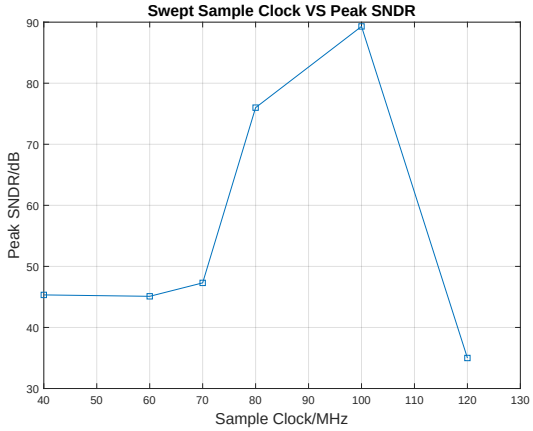


Figure 4.14. The corresponding maximum SNDR versus the frequency of the sample clock.

frequencies, the matching results between simulation and test indicate that the NTF is not the ideal one for this fourth-order CT delta sigma modulator and that is the main reason for the limited SNDR in testing. A frequency sweep is given to the sample clock in simulation, the corresponding maximum SNDR is shown in Fig. 4.14. We can see the maximum SNDR improves with the increasing sample frequency and obtains its optimal performance when sample frequency arrives at the designed value, namely 100 MHz.

The conclusion is that this system should be operated with the designed clock frequency to get the desired NTF. In this context, the challenge is to generate a stable high-frequency input clock for the chip at the board level, as described next. In particular, we need an input clock frequency of $2 \times 100 = 200$ MHz to obtain quadrature sampling clocks at 100 MHz for the two DSM channels.

## 4.3 High Frequency Test Board Design and Test

To operate the whole circuit at the targeted clock frequency, a new test board with two kinds of clock source was designed. A crystal oscillator (AX3DCF1-200, Abracon) generating 200 MHz clock is selected as the source of clock divider to provide a sample clock of 100 MHz and chopping clock of 50 MHz. The output of the AX3DCF1-200 uses low-voltage differential signaling (LVDS) as the standard protocol, so 100 Ω impedance matching is considered when routing the differential pairs. In addition, due to the limited voltage swing (±300 mV) of LVDS, a high-speed level translator chip (Si53306-B, Silicon Labs) that supports LVDS input and LVCMOS output is added to generate desired voltage levels for the on-chip clock buffers. On the other hand, an RF signal generator port is set as an alternative choice for the clock divider; this is fed through a transformer with ratio of 1:1 to generate the required differential output for the level translator. The schematic of the high-frequency clock generator is shown in Fig. 4.15.

The oscilloscope-probed 200 MHz clock is shown in Fig. 4.16. The oscillator's datasheet shows its rising/falling time range is 300-500 ps(20%-80%Vpp), while the measured rising/falling time of 200 MHz clock is 1 ns, which is 20% of the duty cycle (5 ns). Considering the parasitic capacitor on the probe, the real rising/falling time should be shorter than 1 ns. However, according to test results of chopping clock and sample clock, the

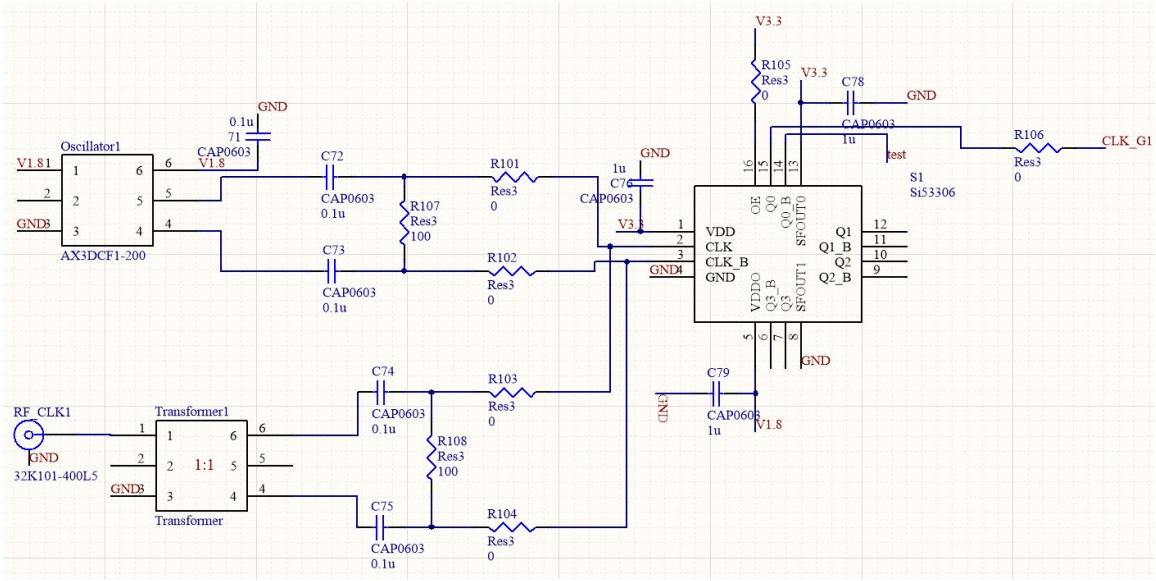


Figure 4.15. Schematic of the high-frequency clock system.

parasitic capacitor on the pads has significant influence with the increase of clock frequency. With such a unclear clock, the whole circuit has a maximum measured SNDR of 47 dB when the input voltage is 700 mV and VDD is set to 2.2 V. The measured power spectrum density of the output signal with maximum SNDR is shown in Fig. 4.17. Note that when testing, the power supply was increased from 1.8 V to 2.2 V, which is within the acceptable range of both the on-chip 1.8 V transistors and the ESD protection diodes on the pads. This change increased the drain-source voltages across devices within the op-amps, thus increasing i) the measured linear range from 500 mV to 700 mV, and ii) the measured peak SNDR by ~15 dB.

Verification simulations on the Cadence circuit were also done with a realistic clock rising/falling time of 0.8 ns (ideal one is 0.1 ns). These simulation result show that the desired NTF is destroyed, and the resulting SNDR matches the test results. Thus, redesign of the clock system is critical for improving the performance of the CT-DSM modulator.

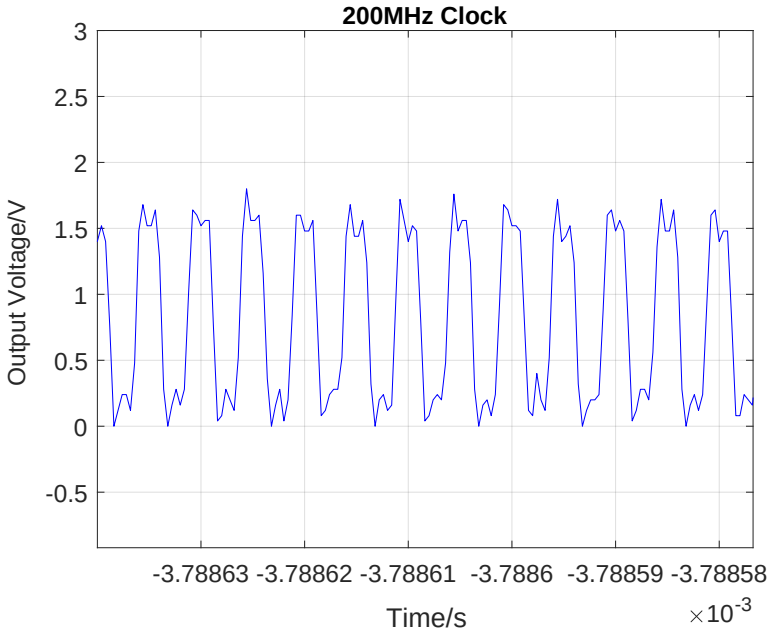


Figure 4.16. Oscilloscope-probed clock waveform at the target input frequency of 200 MHz.

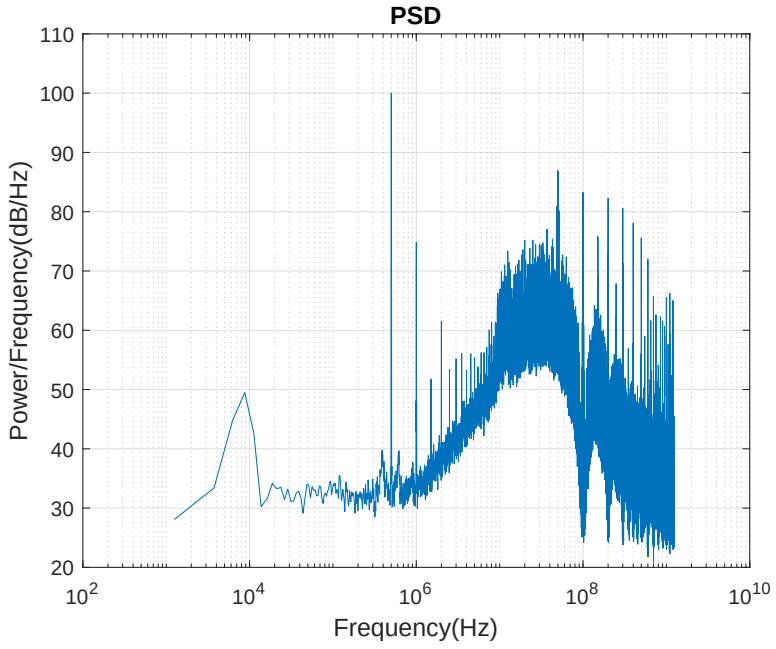


Figure 4.17. The measured PSD of the output signal with maximum SNDR that was obtained using the target clock frequency of 200 MHz.

## 4.4 Data Processing for the Delta sigma modulator

An effective signal processing method acts an important role when applied to evaluate the signal's SNDR and analyze the ADC's performance. In this research, specific attentions are mainly given to post-processing, and choosing a window function to deal with the finite length of the measured output sequences.

For post-processing method, level shifting is important since the measured output of the delta-sigma modulator is an analog waveform while the data of interest is a digital sequence. Thus, the collected data is first compared with a threshold value to convert the analog data recorded from the oscilloscope to a digital data stream (0 or 1), which removes the measurement noise coming from the oscilloscope, power supplies, etc.

The power spectrum density (PSD) is the main tool to evaluate the quality of the signal and noise. When subjecting a time-domain signal to a Fast Fourier Transform (FFT) to acquire its spectrum in the frequency domain, the choice of windowing has a significant effect on the conversion. Because we cannot obtain an infinite-length record of the output sequence coming from the delta-sigma modulator, the use of a smooth window function on the finite-length recorded signal is required to improve SNDR estimation accuracy. The absence of a window corresponds to using a rectangular window, which can generate significant SNDR estimation errors due to the relatively high spectral sidelobes introduced after convolution with its Fourier transform (which is a sinc function). Using a smooth window function greatly reduces this effect by decreasing the sidelobe levels after convolution. Three common windows and their Fourier transform magnitudes are shown in Fig. 4.18. The peaks of high-frequency lobes in the spectrum of the Hann and Hann$^2$ windows go to zero, while the rectangular one approaches a constant value. In addition, we should ensure that signal leakage into adjacent bins is a small

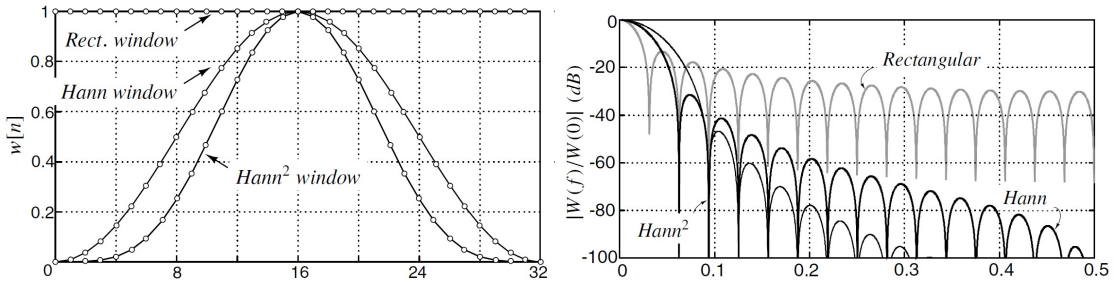


Figure 4.18. (a) The rectangular, Hann, and Hann$^2$ windows; (b) Fourier transform magnitudes of the rectangular, Hann, and Hann$^2$ windows.

value compared to the actual in-band noise density. In this situation, the Hann window usually provides sufficient protection [1]. In fact, it ensures that the signal energy is almost completely localized within ±2 bins of the spectral peak, thus largely eliminating the effect of signal leakage. The power spectrum density (PSD) plots in this thesis were thus evaluated based on the Hann window.

# 5 Conclusion and Future Work

This thesis proposes a novel digital RF-over-fiber transmission link for the MRI signal based on delta sigma modulation. A discrete-time delta sigma modulator (commercial chip) was applied into the transmission link as the proof-of-concept. Then based on the MRI signal's requirement of high signal-to-noise and distortion ratio (SNDR), a fourth-order continuous-time delta sigma modulator circuit was designed, simulated, and fabricated in the TSMC 180 nm CMOS process. Testing results are also described. The simulation performance and test results verify the delta sigma modulator's functionality as an analog-to-digital converter (ADC). A conference paper and an abstract were published based on the simulation and testing results[22]. In this chapter, the performance of the chip is summarized and the future work is also discussed.

## 5.1 Conclusion

Transmission of digitized RF-over-fiber based on the discrete-time delta sigma modulator (commercial chip) was verified by the experiment. The consistency of the signal linear range between the transmitter side and receiver side proves the transmission reliability of the optial fiber. For this second-order delta sigma modulator, the maximum signal-to noise and distortion ratio (SNDR) is 56 dB when the over sampling rate (OSR) is

50. The signal's linear range has been studied and optimized through comparative testing with different OSR values. To further improve the transmission link's performance, a higher OSR and higher order delta sigma modulator should be designed. With a target SNDR of 90 dB, which comes from the requirement of the MRI signal's properties, a Simulink model is built using the optimization capabilities of the MATLAB Delta Sigma Toolbox.

Consequently, a fourth-order continuous-time delta sigma modulator with higher OSR was proposed as an improvement over the discrete-time version. The cascaded integrators with feedforward (CIFF) loop-filter structure was chosen to increase the order of the loop filter and provide a fast path for each stage. A feedforward compensation op-amp is chosen for the RC integrator because its high speed and low power consumption. A chopping circuit is utilized in the first op-amp integrator stage to reduce input-referred $1/f$ noise and offset. The first integrator stage also uses an assistant circuitry to steer currents from the feedback DAC and input signal, thus improving the large-signal performance of the op-amp. A clocked dynamic comparator is selected as 1-bit quantizer, which is inherently linear and simplifies the DAC design. To recover the signal from the output stream, only an analog lowpass filter is needed. The proposed CT-DSM is designed in the TSMC 180 nm process. Transistor-level simulations show a peak SNDR of 89.3 dB for a sample frequency of 100 MHz and an OSR of 100, which is sufficient for this application.

The chip was firstly tested with a low sampling clock frequency to provide a clear clock for the whole system. With OSR of 100 and a sampling clock of 10 MHz, the maximum SNDR measured was 50 dB, and both channels were found to operate in a similar manner. The chopping circuit helps to improve the circuit SNDR performance by

10 dB. The recovered signal can be obtained just by employing a Butterworth lowpass filter with the MATLAB, which is one of the benefits of using a delta-sigma modulator's - namely, simplifying the receiver design compared with other types of ADC. The delta-sigma modulator's digitizing function as an ADC is verified through the time-domain performance. The whole circuit runs with a current of 2.8 mA, leading to a power consumption of 5 mW and the corresponding Walden figure of merit (FOM) of 195 fJ/bit.

Through analysis of the limited SNDR performance, the noise transfer function (NTF) was found to deviate from the desired one because of the low sampling clock frequency. For a continuous-time delta sigma modulator, the integrator time constants within the loop filter need to increase by the same factor when the sample frequency is decreased; otherwise, the NTF will degrade. This behavior is completely different from the discrete-time (DT) delta sigma modulator, for which the loop-filter is in discrete time and thus has time constants that naturally scale as $1/f_{clk}$ since the value ($R$) of a switched-capacitor resistor is set by $R = 1/(f_{clk} \cdot C)$. Corresponding simulations have verified these analysis results.

In order to overcome this issue, a new test board that supports high sampling clock frequencies was designed. The new board-level clock generator circuit considers both the routing capacitance and impedance matching to generate a 200 MHz input clock for the custom modulator chip. Because of the limited rising/falling time of the oscillator and the parasitic capacitors on the pad, the whole system still runs with an unclear clock system, which leads degradation of the measured SNDR. Increasing the power supply for the chip improves the SNDR performance, with the trade-off being higher power consumption. These results are consistent with transistor-level simulations, thus suggesting that an optimized clock system should provide significantly better performance.

## 5.2 Future Work

This thesis shows the feasibility of a fourth-order continuous-time delta sigma modulator with CIFF structure. However, additional work is still needed to optimize the performance of the circuit. A clean high-frequency clock should be provided to run the system in the desired environment. For high-frequency testing, impedance matching should be considered during the test board design and for connecting to benchtop test equipment. For the second version of the chip design, an on-chip phase-locked loop (PLL) can be considered to provide a precise clock system and a quad flat no-lead (QFN) package should be used to provide less parasitic capacitance.

After getting better test performance, this chip can be installed in the RF-over-fiber transmission links to verify the whole idea and generate final test results in the environment of a MRI scanner.

# Appendix A
# PCB Design for Chip Test

This appendix presents the schematic and layout of the test board used as the chip test bench.

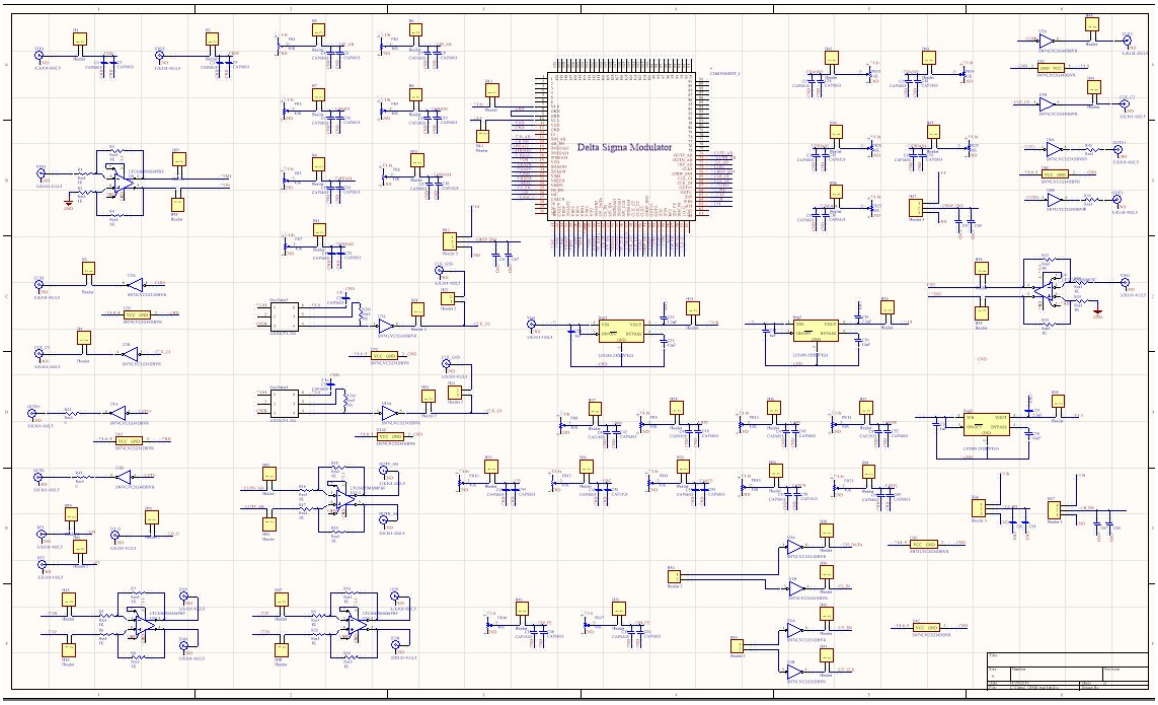


Figure A.1. Schematic of the test board.

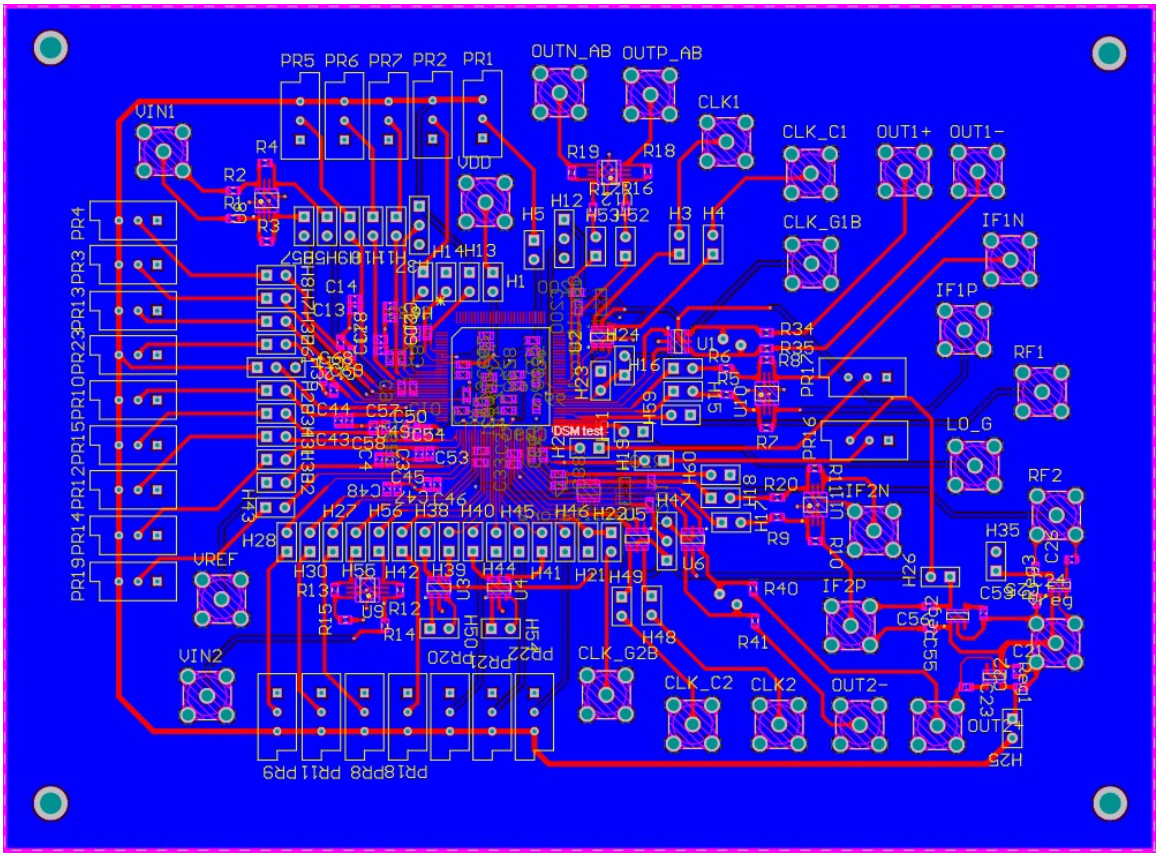


Figure A.2. Layout of the test board.

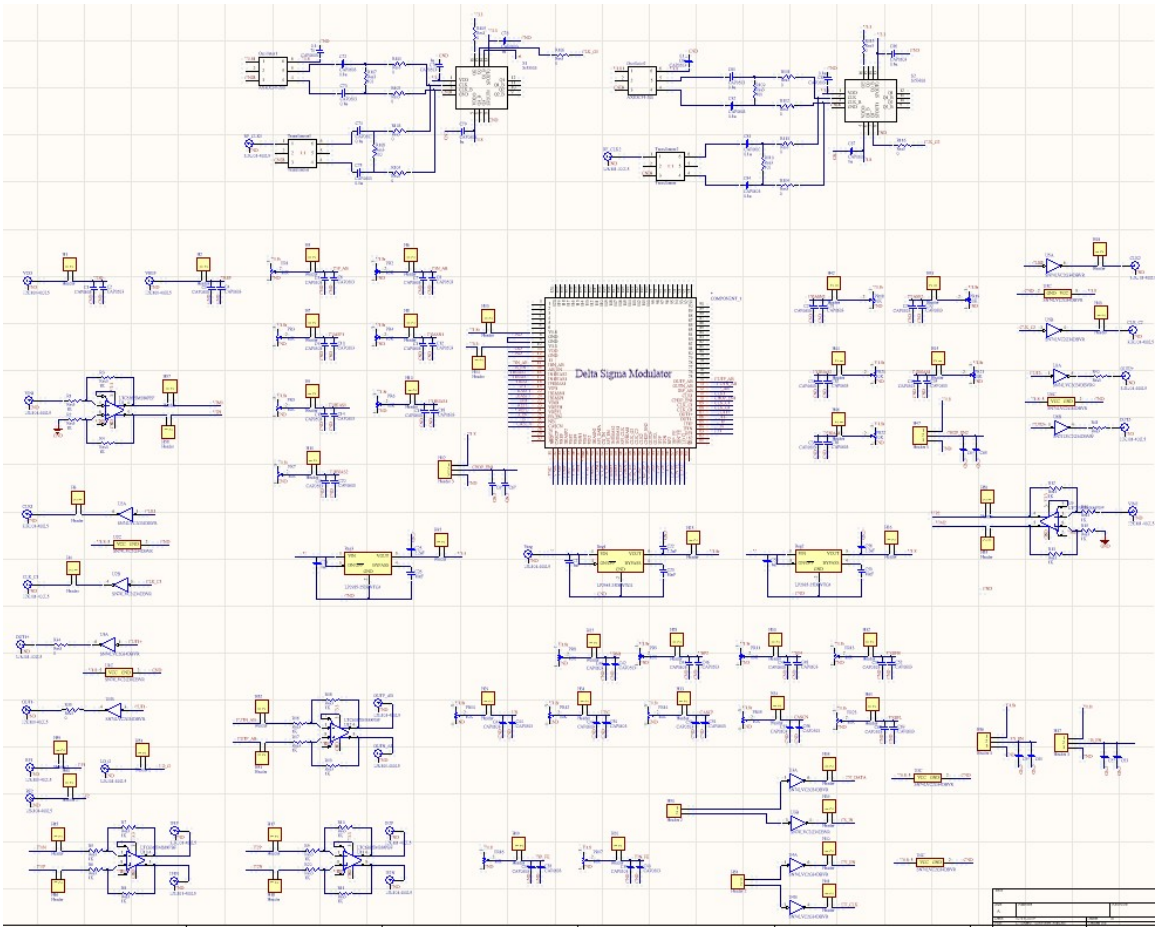


Figure A.3. Schematic of the test board for high-frequency operation.

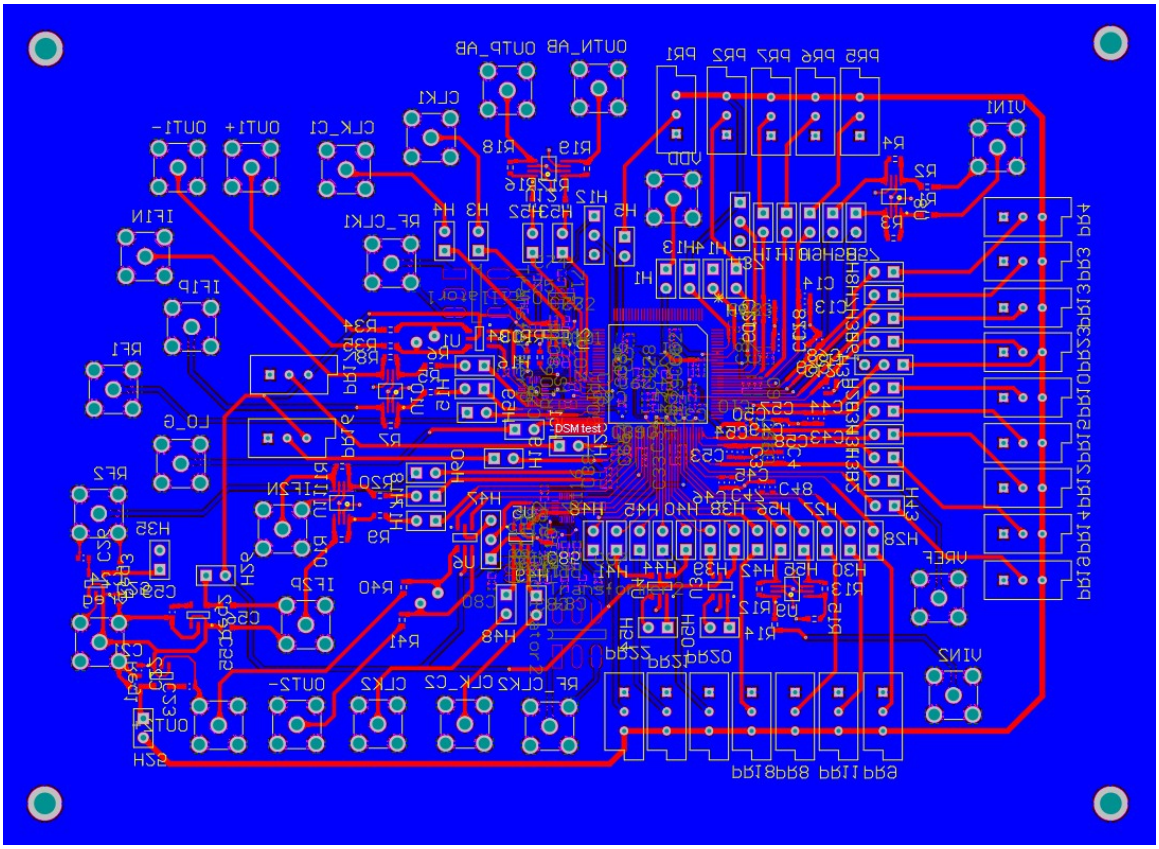

Figure A.4. Layout of the test board for high-frequency operation.

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