

# Toward A Formalized Approach for Spike Sorting Algorithms and Hardware Evaluation

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**Abstract**—Spike sorting algorithms are used to separate extracellular recordings of neuronal populations into single-unit spike activities. The development of customized hardware implementing spike sorting algorithms is burgeoning. However, there is a lack of a systematic approach and a set of standardized evaluation criteria to facilitate direct comparison of both software and hardware implementations. In this paper, we formalize a set of standardized criteria and a publicly available synthetic dataset entitled *Synthetic Simulations Of Extracellular Recordings (SSOER)*, which was constructed by aggregating existing synthetic datasets with varying Signal-To-Noise Ratios (SNRs). Furthermore, we present a benchmark for future comparison, and use our criteria to evaluate a simulated Resistive Random-Access Memory (RRAM) In-Memory Computing (IMC) system using the Discrete Wavelet Transform (DWT) for feature extraction. Our system consumes approximately (per channel) 10.72mW and occupies an area of 0.66mm<sup>2</sup> in a 22nm FDSOI Complementary Metal-Oxide-Semiconductor (CMOS) process.

**Index Terms**—Spike Sorting, RRAM, IMC, CMOS, DL

## I. INTRODUCTION

ELECTROPHYSIOLOGY, extracellular recordings of neuronal populations, has become a cornerstone for neuroscience research due to its ability to measure action potential and neuronal activities in the vicinity of electrodes. However, extracellular recordings are the summation of action potentials fired by a variety of neurons within the recording vicinity, and consequently require decoding. Advances in CMOS and emerging IMC technologies [1], such as RRAM, allow for an exponential increase in number of neurons that can be simultaneously recorded, which calls for development of fast, efficient, and automated spike sorting algorithms to decode the recorded information.

Extracellular recordings paired with spike sorting are prerequisites for both commercial applications, such as Brain-

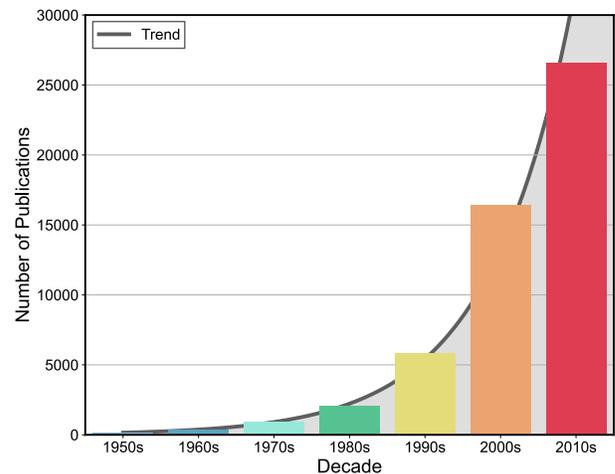


Fig. 1: Number of publications related to spike sorting over the decades since its pioneering in the 1950s.

Machine Interfaces (BMIs), which can restore motor functions or damaged sensory functions [2], and for research applications, where interactions between different neurons and their network effects that give rise to complex higher order functions such as movement, perception, and memory are studied. Since the pioneering work of the spike sorting field in the 1964 [3], the field has attracted an exponentially growing attention from the neuroscience and engineering community, as demonstrated in Fig. 1. However, there lacks a standardized set of criteria for evaluating spike sorting algorithms, which poses a challenge for researchers when comparing algorithms and hardware combinations to suit specific applications. In this paper, our specific contributions are as follows:

- 1) We formulate a set of criteria and standardized dataset for evaluating spike sorting algorithms and hardware;
- 2) We present a case study using our criteria to benchmark a RRAM IMC and compare performance to a traditional CMOS hardware implementation.

TABLE I: Overview of criteria and algorithms used by spike sorting publications in the literature.

Paper	Year	Criterion(s)	Main Algorithm(s)
[5]	2000	Accuracy, noise tolerance.	Neural network spike classification.
[6]	2004	Accuracy.	Wavelet feature extraction and superparamagnetic clustering.
[7]	2006	Accuracy, computational complexity, power consumption on custom hardware.	Integral Transform.
[8]	2010	Accuracy, custom FPGA execution speed and precision, resources associated with each computing component.	Hardware implementation of neural network spike sorting on custom FPGA.
[9]	2011	Accuracy, alignment invariance.	Fuzzy logic spike sorter.
[10]	2012	Accuracy.	Adaptable feature extraction.
[11]	2012	Accuracy, computational complexity, power consumption on custom hardware.	ZCFs and hardware architecture.
[12]	2013	Power consumption on custom system architecture, memory requirement, accuracy.	16-channel online spike sorting algorithm and implantable hardware design.
[13]	2018	Accuracy, execution time.	Spike sorting based on shape, phase, and distribution features, and K-Tops clustering.
[14]	2019	Accuracy, firing rate and noise tolerance, requirement for manual intervention.	Normalized template matching for spike sorting.
[15]	2020	Accuracy, memory requirement.	Salient feature extraction and on-implant module design.
[16]	2020	Accuracy.	Spike sorting with DL.
[17]	2020	Noise tolerance, accuracy, computational complexity.	Feature extraction with feature denoising filter preserve maximum information.

## II. RELATED WORK

Table I shows an overview of several noteworthy publications from the past decade, and the criteria each used for evaluation. While all studies evaluate the classification accuracy of their algorithm, only some also investigate the algorithm’s performance over a variety of other criteria. Due to the relatively recent re-emergence of the spike sorting field, there is currently no consensus on a standardized method to use. Additionally, unlike other well established signal processing techniques, such as power spectral analysis, accuracy is not the only criteria of consideration due to the highly demanding nature of spike sorting applications and experimental settings.

We note that this paper is not intended to serve as a survey or review paper like [4], and that while many of the formalized criteria have been previously reported in related works, as a collective, they have not been done so systematically.

## III. PRELIMINARIES

Spike sorting refers to algorithms that detect individual spikes (action potentials) from extracellular neural recordings and classifies them according to their shapes, which attributes detected spikes to the originating neurons. This technique operates on the principal that different neurons tend to produce spikes of varying shapes, due to their varying proximity to the electrode, as well as their varying morphology of dendritic trees [18]. Current spike sorting techniques generally involve 3 steps: 1) Spike detection; 2) Feature extraction; 3) Classification. A general processing pipeline is shown in Fig. 2. Bandpass filtering is generally used to eliminate high frequency artefacts and low frequency noise. For online applications, a causal filter is required, while non-causal filters are preferred for offline analysis. Spike detection isolates single spike waveforms, typically of duration 1-3ms, and aligns them accordingly. Next, 2 or 3 features that best distinguish between different spike classes are extracted, which alleviates the problem of "curse of dimensionality". The extracted features are

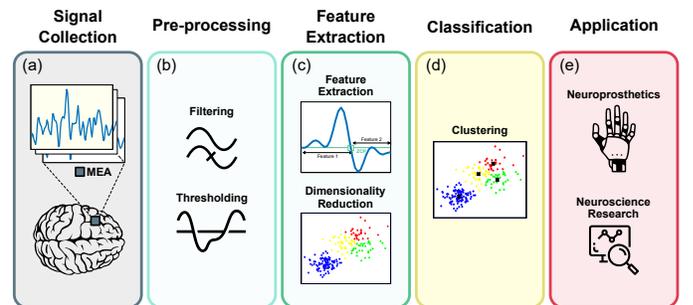


Fig. 2: A general processing pipeline for spike sorting.

TABLE II: Proposed spike-sorting criteria.

Criterion	Description
① Detection Accuracy (%)	Spike detection accuracy.
② Detection AUROC	Spike detection Area Under the ROC (AUROC).
③ Feature Extraction and Classification Accuracy (%)	The overall sorting accuracy out of the correctly detected spikes.
④ ICV	Measurement of the compactness of each cluster.
⑤ Power (W/Ch)	Power (per channel).
⑥ Energy (J/Ch)	Energy (per channel).
⑦ Area (m <sup>2</sup> /Ch)	Area (per channel).
⑧ Latency (s/Ch)	Latency (per channel).

then used as inputs to supervised or unsupervised classification algorithms which output the corresponding class for each spike.

## IV. PROPOSED SET OF FORMULATED CRITERIA

In Table II, our proposed spike-sorting criteria is summarized. In this section, we discuss each criterion in more detail.

### A. Accuracy Performance

Accuracy is the most commonly used criterion across almost all spike sorting publications, as it is the most direct indication

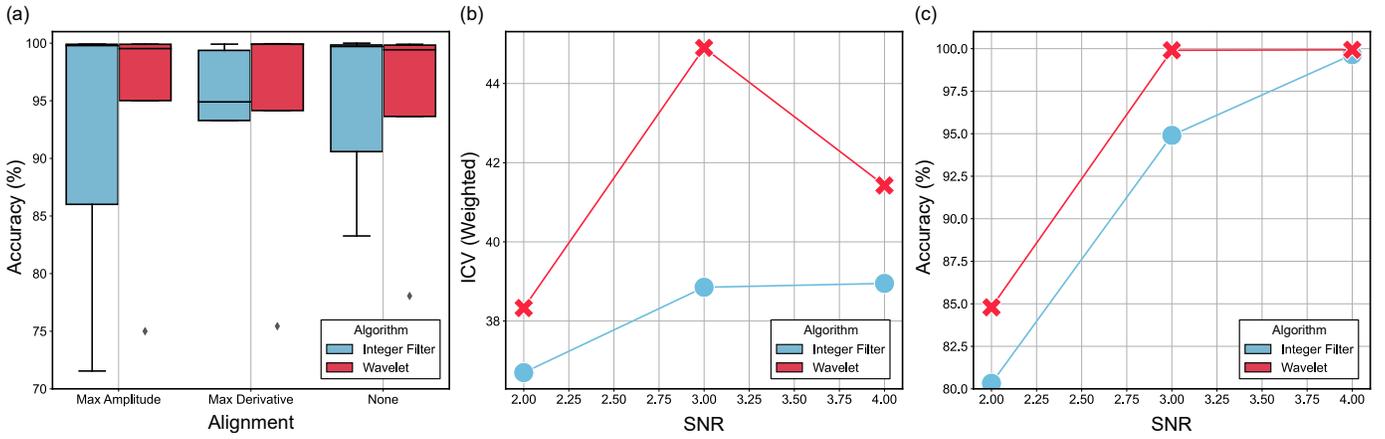


Fig. 3: (a) The impact of spike alignment techniques on classification accuracy for both algorithms. It can be seen that alignment slightly improves the wavelet but hinders the integer filter technique. (b-c) A comparison of the ICV and accuracy metrics when both algorithms are used for different SNRs. Between ICV and accuracy metrics, a Pearson Correlation Coefficient (PCC) of 0.7232 is reported, which indicates weak correlation.

of an algorithm’s performance. As previously mentioned, most spike sorting algorithms are comprised of 3 stages: spike detection, feature extraction, and clustering. Amongst these, spike detection is often isolated and its accuracy (the ① spike detection accuracy) is evaluated independent of later steps. Likewise, feature extraction and clustering are often combined and tested for classification accuracy, independent of detection accuracy. This accuracy evaluation scheme is to ensure that the user can accurately determine how each stage contributes to the accuracy and make necessary changes if required. Additionally, noise tolerance metrics should be included to assess performance degradations.

1) *AUROC*: In addition to reporting the spike detection accuracy, many works also construct ROC curves and report the ② detection AUROC for discrimination evaluation [4].

2) *Feature Extraction and Classification Accuracy*: To eliminate any confounding effects from the spike detection step, when evaluating the ③ feature extraction and classification accuracy, ground truth spikes should be used if they are available. When ground truth labels are not available, in lieu of the classification accuracy, the ④ ICV [19] metric, as defined in (1), can be used.

$$ICV = \frac{1}{N_i} \sum_{j=1}^{N_i} (v_j - \mu_i)^2 \quad (1)$$

The ICV metric was originally used to measure the compactness of each cluster, where  $v_j$  is the  $j$ th spike in the  $i$ th cluster,  $\mu_i$  is the mean waveform, and  $N_i$  is the number of spikes in cluster  $i$ . For more comprehensive accuracy testing, performance on real data sets can be evaluated.

3) *Noise Tolerance*: Noise tolerance is crucial to consider when choosing spike sorting algorithms, as noise can significantly hinder some algorithms while others remain relatively more robust [17]. Different datasets used by various studies have vastly different noise levels presenting challenges to

TABLE III: Hardware performance of our simulated system adopting the DWT for feature extraction.  $\diamond$ Not reported.

Criterion	Our Reported Values	65-nm CMOS [20]
Power (mW/Ch)	10.72	0.000175
Energy (mJ/Ch)	1.45	N/R $\diamond$
Area (m <sup>2</sup> /Ch)	0.66	4.14e-7
Latency (ms/Ch)	135.53	N/R $\diamond$

direct comparison, hence a standardized dataset with varying noise level should be used such as the one used in this work.

4) *Alignment Requirements*: Alignment is an additional spike sorting step that refers to aligning spikes before the feature extraction and classification. Some algorithms benefit significantly from this additional step, while some do not [9]. Alignment benefits should be compared when evaluating ①, ②, ③, and ④.

#### B. Power, Energy, Area, and Latency

The ⑤ power, ⑥ energy, ⑦ area, and ⑧ latency (per channel) should be reported for all stages (a)-(e) in Fig. 2 for a specific hardware implementation technology. In addition to facilitating direct comparison, these metrics can be used to evaluate the online applicability of a given system under different resource constraints.

### V. THE SSOER DATASET

One of the greatest challenges facing spike sorting algorithm development is the lack of labelled experimental data, which gives researchers the ability to validate their algorithms and measure evaluate performance. Hence, synthetic extracellular recordings have been developed to simulate neural recordings, constructed from known spike shapes as ground truths. In this paper, we formulate a dataset for unsupervised and supervised spike sorting algorithms entitled SSOER [21], which is the amalgamation of five smaller synthetic datasets with varying

SNRs, which were originally presented in [22]. These datasets are comprised of spikes from a database with 594 different average spike shapes, taken from real recordings from monkey neocortex and basal ganglia. Recordings are sampled with a sampling frequency of 96 kHz, filtered, and then down-sampled to 24 kHz. SSOER is made openly accessible<sup>1</sup>.

## VI. CASE STUDY: A RRAM IMC SYSTEM

To demonstrate the robustness of our formalized approach, we present a case study evaluating a simulated RRAM IMC system implemented using a 22nm FDSOI CMOS process with device integration at the Back-End-Of-The-Line (BEOL). RRAM devices can be arranged in crossbar configurations to efficiently perform analogue Vector-Matrix Multiplications (VMMs) in-memory [1], [23], [24], which is the most dominant operation in many popular algorithms. For spike-sorting applications, RRAM is preferable over charge-based memory such as SRAM and DRAM due to its scalability down to nanometer scale [25]. We use a crossbar model proposed by Primeau et al. 2021 [26], which is based on existing semi-passive crossbar models [24], [27], to simulate the feature extraction stage of the spike sorting pipeline. To compute the DWT, five unique decomposition levels (iterations) were used, each comprising of many VMM operations. These were mapped onto a singular crossbar made-up of 64 modular tiles of  $(8 \times 8)$  RRAM devices. More comprehensive system- and circuit-level information, all simulated models, and detailed hardware evaluation methodologies are made accessible<sup>1</sup>. In Fig. 3, the performance of our IMC implemented DWT, i.e., metrics ① – ④, is compared against a digital integer filter algorithm from [20]. Metrics ⑤ – ⑧ are reported in Table III.

From Fig. 3 (a), for both algorithms, it can be observed that alignment improved classification accuracy across all datasets in most cases, while integer filter generally benefited more from the alignment. In Figs. 3 (b-c), a PCC of 0.7232 was reported between both metrics, indicating weak correlation. This, however, is still deemed significant, considering that the ICV metric can be determined without the need to label data. The classification accuracy decreased for both algorithms with increasing noise level, less so with the wavelet technique.

In Table III, the total reported power and area values of the simulated IMC RRAM system are significantly larger than that reported by [20]. As this case study was designed to demonstrate the effectiveness of our formalized approach, and not to investigate the feasibility of IMC RRAM systems for spike sorting applications, no architectural hardware optimizations were performed, such as gating and latency balancing.

## VII. CONCLUSION

In this work, a formalized approach for spike sorting algorithms and hardware evaluations was proposed and a case study has been performed to demonstrate the efficacy of such methodology. With the consolidated SSOER dataset, the critical challenge of direct comparison between systems

have been addressed which should aid future researchers with selecting the appropriate spike sorting systems as well as identifying areas for improvements.

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<sup>1</sup><https://github.com/TimothyZh/MWSCAS2022SpikeSortingCriteria>

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