Stochastic neuron design using conductive bridge RAM

Giorgio Palma, Manan Suri, Damien Querlioz, Elisa Vianello, Barbara de Salvo

Stochastic neuron design using Conductive Bridge RAM

Giorgio Palma*, Manan Suri*, Damien Querlioz†, Elisa Vianello*, Barbara De Salvo*
*CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France.
†Institut d'Electronique Fondamentale, Univ. Paris-Sud, CNRS, 91405, Orsay, France.

***Abstract*— We present an original methodology to design hybrid neuron circuits (CMOS + non volatile resistive memory) with stochastic firing behaviour. In order to implement stochastic firing, we exploit unavoidable intrinsic variability occurring in emerging non-volatile resistive memory technologies. In particular, we use the variability on the 'time-to-set' (t_{set}) and 'off-state resistance' (R_{Off}) of Ag/GeS_2 based Conductive Bridge (CBRAM) memory devices. We propose a circuit and a novel self-programming technique for using CBRAM devices inside standard Integrate and Fire neurons. Our proposed solution is extremely compact with an additional area overhead of 1R-3T. The additional energy consumption to implement stochasticity in Integrate and Fire neurons is dominated by the CBRAM set-process. These results highlight the benefits of novel non memory technologies, whose impact may go far beyond traditional memory markets.**

I. Introduction

Neuroinspired (or 'neuromorphic') hardware research has gained a lot of importance in recent years due to its promising low-power, fault-tolerant, and ultra-adaptative computing paradigms [1], [2], [3], [4], [5]. Neuromorphic computing is usually accomplished with deterministic devices and circuits. However, literature in the fields of neural networks [6], [7] and of biology [8] suggests that in many situations, actually providing a certain degree of stochastic, noisy or probabilistic behavior in their building blocks may enhance the capability and stability of neuroinspired systems. Some kind of neural networks even fundamentally rely on stochastic neurons, like Boltzmann machines [9], [10]. Finally, stochastic neurons may perform signal processing in extremely noisy environments using a phenomenon known as 'stochastic resonance' [11], [12].

In neuromorphic hardware, providing stochastic behavior to neurons using pseudo-random number generators will lead to significant overheads. This explains interest in developing silicon neurons with an intrinsic stochastic behavior, but which may be controlled. In previous works, different techniques to implement controlled stochasticity in hardware neural networks have proposed. It is possible to exploit the thermal noise in the CMOS but this may lead to silicon overheads and unwanted correlations [6]. Other techniques exploit CMOS circuits with using noise but have significant area overhead [13], or the noise of photons with photodetectors [14] or even special kinds of 'noisy transistors' [15]. Finally it was proposed to use fundamentally probabilistic nanodevices like single electron transistors [16], but which might suffer from poor CMOS compatibility and room temperature operation. In this paper, we describe an original circuit and methodology to design a neuron with stochastic firing behavior exploiting certain physical effects of emerging non-volatile resistive memory technology devices such as Conductive Bridge memory (CBRAM). There are significant advantages of our approach because of the easiness of fabrication in the Back-End-Of-Line (BEOL), CMOS compatibility [17], predicted scalability to sub-$20\,\mathrm{nm}$ [18] and low programming voltages of CBRAM memory devices [19].

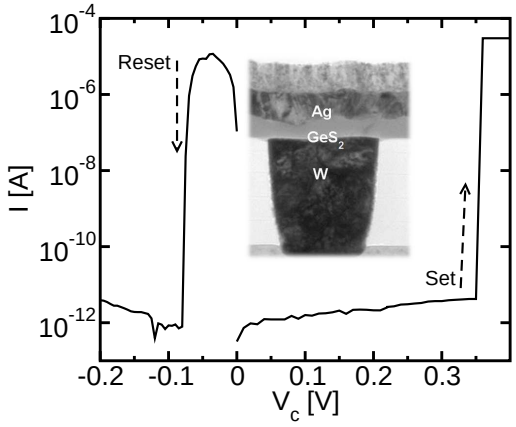

Fig. 1. Quasi-static I-V curve for the CBRAM device showing the switching from high (reset) to low resistive states (set). TEM image of the CBRAM resistor element [23]. The GeS_2 layer has a thickness of $30\,\mathrm{nm}$.

The remainder of this paper is organized as follows: in Section II, we describe the structure and the working principle of our CBRAM devices, and the stochastic effects which we exploit for designing the non-deterministic firing neuron. Section III, describes the basic concept and an example of simple circuit for obtaining a stochastic neuron. Section IV discusses transient simulations that we performed on a basic circuit, which validates our concept.

II. CBRAM technology

A. Structure and working principle

Fig. 1 shows a TEM image of the CBRAM device structure used in this work. A Tungsten (W) plug, typically used as interconnect between two metal levels, is used as bottom electrode for the CBRAM. The solid electrolyte consists of a $30\,\mathrm{nm}$ thick GeS_2 layer deposited by radio frequency physical vapour deposition (RF-PVD). A $3\,\mathrm{nm}$ Ag layer is dissolved into the GeS_2 using the photo-diffusion process [20]. Then a 2^{nd} layer of Ag is deposited to act as top electrode.

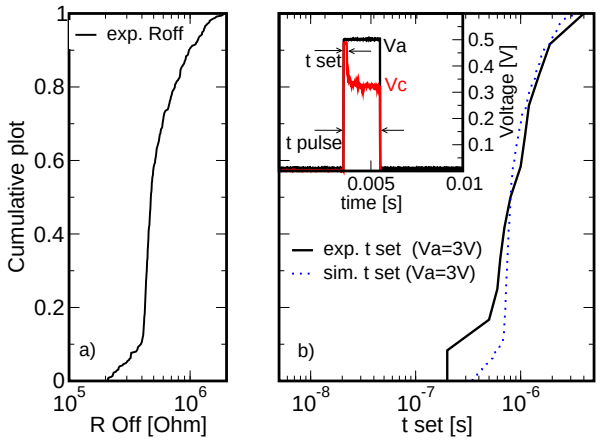

Fig. 2. (a) R_{Off} distribution obtained in GeS_2 based 1R CBRAM devices.(b) Experimental (line) and simulated (dotted) t_{set} distribution obtained cycling the CBRAM cell with a pulse amplitude V_a=3 V. (b in the inset) Example of a typical oscilloscope trace tracking the voltage on the CBRAM (V_c) and the applied pulse (V_a). Between every set operation a reset operation was performed (not shown).

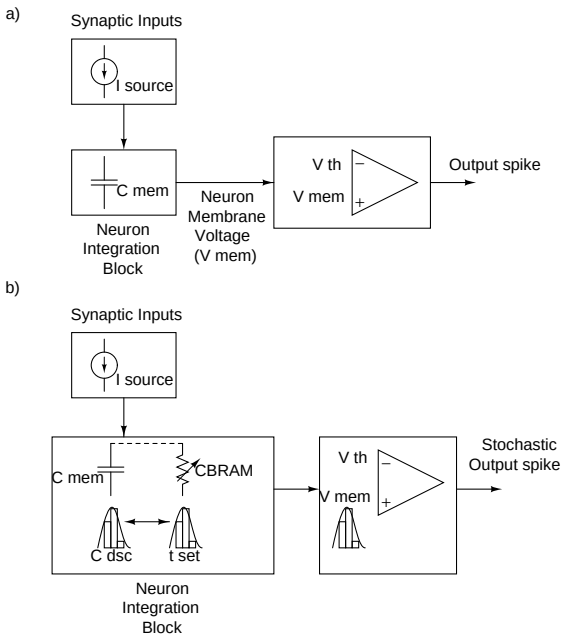

Fig. 3. (a) Schematic image shown the basic concept of a Integrate and Fire neuron [26]. (b) Schematic showing the basic concept of our proposed Stochastic Integrate-Fire neuron (S-IF).

CBRAM working principle relies on the reversible formation of a conductive filament (CF) through a solid electrolyte that results in transition to low and high resistance, respectively, which are referred to as set and reset processes (Fig. 1) [21]. During the set process a positive voltage is applied to the anode which oxidizes, generating Ag^+ ions. The latters, under the influence of the electric field, migrate by hopping to the W cathode where they are reduced and nucleate, building-up an Ag-rich CF. Upon reversal of voltage polarity, besides an electronic current flowing in the CF, an electrochemical current gives rise to Ag^+ ions, inducing a collapse of the filament radius resetting the system to the high resistance state [22].

B. Stochastic effects

By cycling many times our devices a statistical distribution of the high resistive state (R_{Off}) was obtained. Dispersion in R_{Off} may be interpreted in terms of stochastic breaking of the filament during the reset process, due to the unavoidable defects close to the filament which act as preferential sites for dissolution. In previous work [23] we showed, with the help of modeling, that a distribution in R_{Off} leads to a spread in others physical quantities like the left-over filament height (h) and the t_{set}. In this work we push further the analysis by matching the modeled t_{set} distribution with experimental data. In particular, we characterized the kinetic of the set operation by pulse measurements. Fig. 2 inset shows an example of the oscilloscope trace for the evolution of voltage drop across the cell (V_c) during a set pulse. Initially, the cell is in the high resistive state ($R_{Off} \simeq 10^6\,\Omega$) and most of the applied voltage drops on the cell. Then at time t_{set} an abrupt decrease of V_c is observed, revealing a sudden drop of the cell resistance corresponding to the switching from high to low resistive state. Starting from some of the measured values of R_{Off} (Fig. 2(a)) we collected the spread in t_{set} when the applied pulses were V_a=3 V and t_{pulse}=5 µs (Fig. 2(b)). The dotted line in Fig. 2(b), shows the simulated values of t_{set}. To obtain the simulated curve of t_{set}, first the distribution of h was calculated using [24], [25]:

$$R_{\text{Off}} = \frac{\rho_{\text{on}} h + \rho_{\text{off}}(L-h)}{\pi r^2} \tag{1}$$

where ρ_{on} is the resistivity of the Ag-rich nanofilament, ρ_{off} is the resistivity of the GeS_2, L is the chalcogenide thickness and r is the conductive filament radius, then t_{set} using:

$$t_{\text{set}} = \frac{L-h}{v_h \exp\left(\frac{-E_A}{k_B T}\right) \sinh\left(\alpha q \frac{V_c - \Delta}{k_B T}\right)} \tag{2}$$

where q is the elementary charge, v_h is a fitting parameter for the vertical evolution velocity, E_A is the activation energy, k_B is the Boltzmann constant, T is the temperature (300 K), α and Δ are fitting parameters to take into account vertical electric field dependency and the overpotential that controls the kinetic of the cathodic reaction respectively (Table I). In the following section we show how the spread in t_{set} can be used to make the firing of an Integrate and Fire neuron non-deterministic.

III. Stochastic Neuron Design

A. Integrate and Fire Neuron

The complexity of a neuron circuit depends on the overall functionality of the neural network and of the chosen biological

TABLE I
PARAMETERS USED IN THE SIMULATIONS.

Parameter	Value	Parameter	Value
v_h	2 m/s	E_A	0.35 eV
ρ_{on}	$2.3 \times 10^{-6}\,\Omega$ m	ρ_{off}	$10^{-3}\,\Omega$ m
α	0.08	Δ	0.15 V
r	2.2 nm	L	30 nm

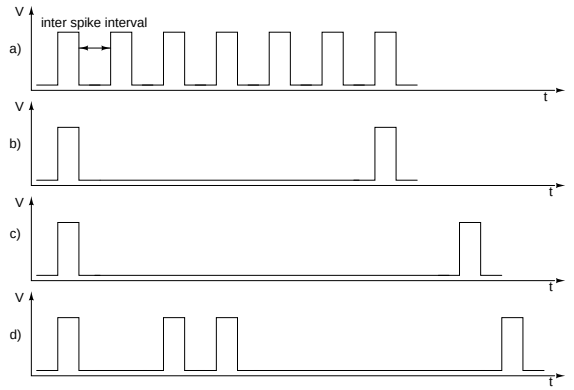

Fig. 4. (a)-(d) Schematic of output neuron firing patterns for different example test cases.

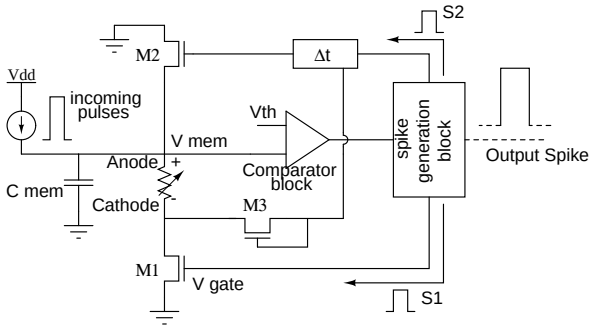

Fig. 5. Proposed circuit-equivalent of the S-IF neuron.

models. For our purpose of concept validation, we chose one of the simplest, the Integrate and Fire neuron model. Fig. 3(a) shows the concept of a simple Integrate and Fire neuron model. It constantly sums (integrates) the incoming synaptic-inputs or currents (excitatory and inhibitory) inside the neuron integration block using a capacitor. More advanced designs also work with this principle [26]. This integration leads to an increase in the membrane potential of the neuron V_{mem}. When the membrane potential reaches a certain threshold value V_{th}, the neuron generates an output spike (electrical signal). After the neuron has fired the membrane potential goes back to a resting value (initial state), through discharging of the capacitor C_{mem}. Usually, the output firing activity of a Integrate and Fire neuron is deterministic because the neuron fires every time the membrane potential reaches a defined threshold value.

B. Stochastic-Integrate and Fire principle and circuit

To introduce non-deterministic or stochastic behavior in Integrate and Fire neuron, we propose to connect a CBRAM device to the capacitor C_{mem}, such that C_{mem} could only discharge through the CBRAM device by switching it to the low-resistive state (Fig. 3(b)). The anode of the CBRAM and the V_{mem} net of the capacitor should be connected. The duration for which current can flow through the low-resistive CBRAM device can be controlled using a transistor. In such a configuration, the spread on the t_{set} of the CBRAM would translate to a spread on the discharge-time (t_{dsc}) of the capacitor. For consecutive neuron spikes, this would lead different initial state of C_{mem}, thus making the firing of the neuron stochastic. Fig. 4 illustrates conceptually the impact of four different values of t_{set} (keeping constant pre-synaptic weights), on the inter-spike interval. In case (a), t_{set} is very long thus the capacitor has a very weak discharge. As a consequence just few additional incoming pre-neuron spikes are required to charge back the V_{mem} to the level of V_{th}, thus leading to an output pattern with the shortest inter-spike interval. In case (b), t_{set} was the shortest, and hence the capacitor discharged the most.

Thus for this case, more incoming pre-neuron spikes are needed to recharge V_{mem}. Case (c) represents a deterministic Integrate and Fire situation with full V_{mem} discharge. Finally, case (d) depicts a situation with different t_{set} durations for consecutive output spikes. It is a possible representation of neuron inter-spike intervals for a random sequence of t_{set} values that can be obtained by cycling the CBRAM device multiple times.

The circuit equivalent of the Stochastic-Integrate and Fire neuron concept shown in Fig. 3(b) is presented in Fig. 5. It consists of a current-source to simulate input currents coming from synapses and pre-neurons, a capacitor C_{mem} to integrate the current and build up the neuron membrane-voltage V_{mem}, a nMOS transistor M1 to perform set operation, two nMOS transistors M2 and M3 to perform the reset operation, a comparator block, a spike-generation block, a delay-element Δt and a CBRAM device. The delay element is used to perform the reset operation of the CBRAM device at the end of each neuron spike.

In Fig. 5, initially the CBRAM is in high-resistive state. As incoming pre-synaptic current is accumulated in C_{mem}, V_{mem} would constantly build up at the anode of the CBRAM. During this time M1, M2 and M3 are off. When the neuron spikes, the spike-generation block will generate an output-spike and two additional pulsed-signals (S1, S2) going to M1 and Δt respectively. S1 acts as a gating signal to turn on M1. V_{mem} build-up and switching on of M1 will enable set-operation of the CBRAM since a positive voltage drop is established between the anode and the cathode. However during the set-operation, M2 and M3 are not turned on, as Δt delays the signal S2.

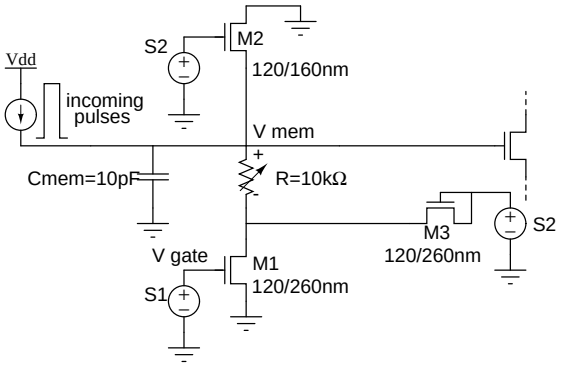

Fig. 6. Circuit used to demonstrate the concept of a S-IF effect when the CBRAM is in the set state.

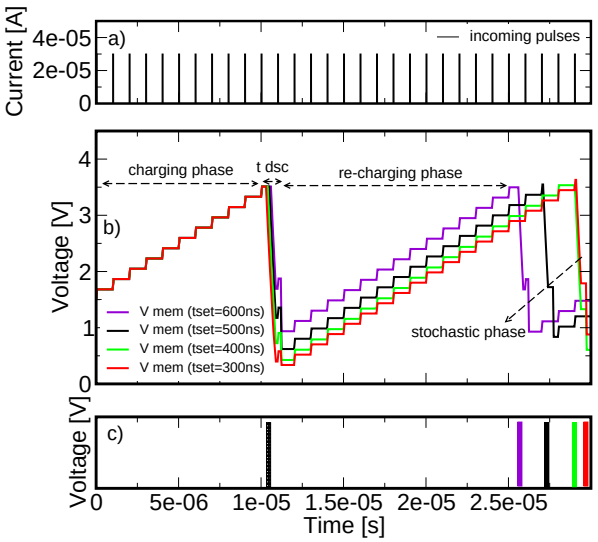

Fig. 7. Full evolution of V_{mem} simulating the circuit shown in Fig. 6. (a) Pre-neuron incoming pulses are used to build up V_{mem}. (b) Initially V_{mem} builds up as consequence of incoming currents (charging phase). Set operation lead to different discharge of C_{mem} (t_{dsc}). During the recharging phase a different number of incoming pulses will raise V_{mem} till V_{th}. (c) Expected different inter-spike intervals depending on the t_{set}.

At the end of the set-operation, the signal S2 will turn on M2 and M3 thus building up the voltage at the cathode to switch the CBRAM to the off-state (reset). Thus, before the next consecutive neuron spikes the CBRAM device is automatically reset and reprogrammed to a different initial R_{Off} state. Note that the flow of current through the CBRAM, during the set-operation, leads to a discharge of the capacitor C_{mem} thus decreasing the membrane voltage V_{mem}. The amount of decrease in V_{mem} can be estimated by calculating the total duration (t_{dsc}) for which current flows through the switched CBRAM. t_{dsc} is the difference of the pulse-width of the signal S1 and the t_{set} (inset of Fig. 2). Depending on the value of t_{set} every time the neuron spikes, different amount of C_{mem} discharge will occur. Thus, in between any two firing cycles, the neuron may require different amount of incoming current to charge V_{mem} to the level of V_{th}.

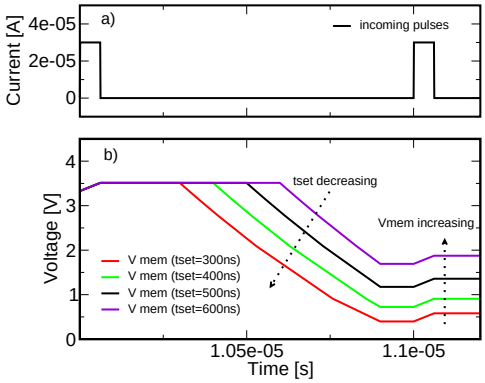

Fig. 8. (a) Pre-neuron incoming pulses are used to build up V_{mem}. (b) Zoom on V_{mem} during the discharging phase for different t_{set} in the range 300 ns-600 ns. Lower t_{set} leads to lower residual membrane voltage V_{mem}.

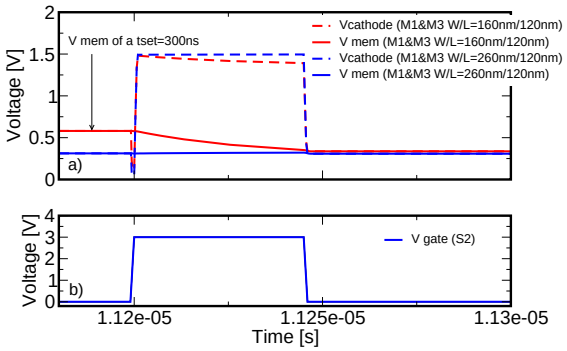

Fig. 9. (a) Time-evolution of V_{mem} and $V_{cathode}$ that establish a voltage drop on the CBRAM to enable reset operation. Larger M3 increase the voltage drop, since $V_{cathode}$ builds up more. V_{mem} corresponding to a t_{set} of 300 ns is considered. (b) Pulse applied to M3.

IV. Results and Discussion

A. Set- and reset- operation

We performed SPICE transient simulation, with Eldo simulator, to validate the proposed concept using a simplified circuit shown in Fig. 6. Transistors and capacitors sizing were not optimized with respect to a real implementation, but to give a simple proof-of-concept. Fig. 7(a) shows a simulated train of incoming pulses (excitatory currents) and the corresponding evolution of the V_{mem} (Fig. 7(b)) between two consecutive neuron spike-cycles. When V_{mem} reaches a threshold voltage V_{th} ($V_{th} \simeq 3.5\,V$ in our simulation), the CBRAM device undergoes set-operation, and C_{mem} begins to discharge. Fig. 7(b) shows the discharging and re-charging of C_{mem} for four different simulated values of t_{set} (in the range 300 ns - 600 ns). Fig. 7(c), shows the expected output of the neuron. Note that different number of incoming pulses are required to reach the neuron firing threshold again, since the initial V_{mem} value is dominated by the stochasticity in t_{set} . Five additional incoming pulses are needed to reach the threshold for the shortest value of t_{set} (300 ns). Fig. 8 shows the zoomed version of C_{mem} discharging for the the different simulations shown in Fig. 7. Note that the longest t_{set} (600 ns) corresponds to the least amount of C_{mem} discharge, and vice-versa. To simulate the reset operation, a pulse of 45 ns with an amplitude of 3 V was applied at M2 and M3, while keeping M1 off. Such high voltage on M3 is required to build up a voltage on $V_{cathode}$. Fig. 9 shows the time evolution of $V_{cathode}$ and V_{mem} when the initial value of V_{mem} was generated by a t_{set} of 300 ns for two different width of M3. The actual voltage drop on the CBRAM can be increased increasing the size of the nMOS as shown in Fig. 9. Moreover, during the reset, an additional discharge of V_{mem} is possible depending on the size of M3, since M2, that is directly connected to V_{mem}, is turned on by S2 (Fig. 10(a)).

B. Parameter constraints

Due to the intrinsic physics of CBRAM device, some constraints in implementing the proposed circuit should be considered. In particular, V_{th} has to be greater than the minimum value of the voltage-drop required to set the CBRAM device for a given pulse-width. The amplitude of S1 should be sufficient

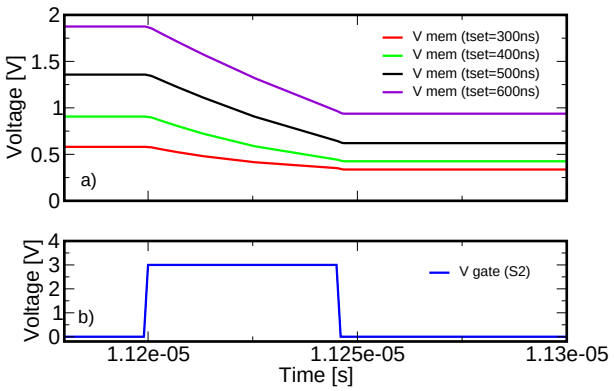

Fig. 10. (a) Time-evolution of V_{mem} during the reset operation for t_{set} in the range 300 ns - 600 ns. Different residual voltages are obtained. (b) Pulse applied to M3.

to turn on the gate of M1, while the pulse-width of S1 depends on the V_{th} and the spread on t_{set}. If S1 pulse-width is very long it would always lead to a complete discharge of C_{mem} and the t_{set} stochasticity cannot be exploited. However S1 cannot be arbitrarily small, it has to be greater than the minimum t_{set} value at a given voltage applied on the anode of the CBRAM device. In a previous work, we have shown the dependence of applied pulse-width and the amplitude of V_a for the CBRAM set-operation [19]. Thus, by tuning the characteristics of S1, the stochastic response of the neuron can be controlled. The amplitude of S1 would determine the amount of current flowing through M1 (compliance current) and thus the final value of the CBRAM resistance in the set state. The set state resistance would determine the programming conditions for the consecutive reset-operation [27]. Thus, the characteristics of S2 can be tuned based on the final CBRAM resistance obtained after the set-operation.

C. Energy consumption

For the proposed S-IF, additional energy consumption per spiking cycling of the neuron will be devoted to perform set and reset operation. The extra-energy consumption is dependent on the ratio R_{Off}/R_{On}; in particular on R_{On} since hundreds of µA can flow before M1 would be turned off, if the low resistance state is $\simeq 10^4\,\Omega$, thus raising the power consumption. We estimated the energy consumption during the set operation using: E_{set}=V_{set} I_{set} t_{set}. In our simulations we used V_{set}=3.5 V (i.e. V_{th}), I_{set}=350 µA, t_{set} in a range between 300 ns and 600 ns that gives a E_{set} energy mean value of 55 nJ. The energy devoted to reset the CBRAM is negligible. For a real system, E_{set} can be strongly reduced increasing the resistance of the low resistive value thus reducing I_{set}, since for the proposed application the ratio R_{Off}/R_{On} is not a major constraint.

V. Conclusions

In this paper, we showed how CBRAM used in an unexpected fashion may allow designing stochastic neurons with low area overheads. We described how CBRAM physics naturally leads to a stochastic behavior in the programming time (t_{set}), which may be exploited in a circuit. SPICE simulations validate the concept on a simple Integrate and Fire neuron. The concept could be extended to more complex neuron designs like [26] and [28], paving the way for the fabrication of complex neuromorphic networks. Other emerging memory technologies might be used for the same purpose provided a certain range of stochasticity in t_{set} as reported in [29] and [30]. These results highlight the benefits of novel non memory technologies, whose impact may go beyond traditional memory markets.

Acknowledgment

The PhD of M. Suri is co-financed by DGA-France. The authors would like to thank ALTIS semiconductors for providing the CBRAM devices for this study.

References

[1] D. S. Modha, R. Ananthanarayanan, S. K. Esser, A. Ndirango, A. J. Sherbondy, and R. Singh, “Cognitive computing”, Commun Acm, vol. 54, p. 62, Aug. 2011.

[2] G. Snider, R. Amerson, D. Carter, H. Abdalla, M. S. Qureshi, J. Lveill, M. Versace, H. Ames, S. Patrick, B. Chandler, A. Gorchetchnikov, and E. Mingolla, “From Synapses to Circuitry: Using Memristive Memory to Explore the Electronic Brain”, Computer, vol. 44, no. 2, pp. 2128, 2011.

[3] P. Merolla, J. Arthur, F. Akopyan, N. Imam, R. Manohar, and D. S. Modha, “A digital neurosynaptic core using embedded crossbar memory with 45pJ per spike in 45nm”, in IEEE Custom Integrated Circuits Conference (CICC), 2011, pp. 1-4.

[4] M. Suri, O. Bichler, D. Querlioz, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, and B. DeSalvo, “Phase change memory as synapse for ultra-dense neuromorphic systems: Application to complex visual pattern extraction”, in IEDM Tech. Dig., 2011, pp. 4.4.1- 4.4.4.

[5] M. Sharad, C. Augustine, G. Panagopoulos, K. Roy, “Spin-Based Neuron Model with Domain-Wall Magnets as Synapse”, IEEE Trans. on. Nanotech. vol. 11 (4) pp. 843-853 (2012).

[6] J. Alspector, B. Gupta, and R. B. Allen, “Performance of a stochastic learning microchip” ,in Advances in Neural Information Processing Systems, vol. 1. Morgan Kaufmann Publishers Inc., 1989, pp. 748-760.

[7] M. van Daalen, P. Jeavons, and J. Shawe-Taylor, “A stochastic neural architecture that exploits dynamically reconfigurable FPGAs”, in IEEE Workshop on FPGAs for Custom Computing Machines, 1993. Proceedings, 1993, pp. 202-211.

[8] S. Fusi, P. J. Drew, and L. Abbott, “Cascade models of synaptically stored memories”, Neuron, vol. 45, no. 4, pp. 599-611, 2005.

[9] G. E. Hinton and R. R. Salakhutdinov, “Reducing the Dimensionality of Data with Neural Networks”, Science, vol. 313, no. 5786, pp. 504-507, Jul. 2006.

[10] R. Salakhutdinov and G. Hinton, “An Efficient Learning Procedure for Deep Boltzmann Machines”, Neural Comput., vol. 24, no. 8, pp. 1967-2006, Apr. 2012.

[11] K. Wiesenfeld and F. Moss, “A Stochastic resonance and the benefits of noise: from ice ages to crayfish and SQUIDs”, Nature, vol. 373, no. 6509, pp. 33-36, Jan. 1995

[12] D. Querlioz, V. Trauchessec, “Stochastic Resonance in an Analog Current-Mode Neuromorphic Circuit”, to be published in Procs. of IEEE ISCAS, 2013.

[13] J. Alspector, J. Gannett, S. Haber, M. Parker, and R. Chu, “A VLSI-efficient technique for generating multiple uncorrelated noise sources and its application to stochastic neural networks”, IEEE Trans. Circuits. Syst., vol. 38, no. 1, pp. 109-123, Jan 1991.

[14] K. Cameron, T. Clayton, B. Rae, A. Murray, R. Henderson, and E. Charbon, “Poisson distributed noise generation for spiking neural applications”, in Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS), 2010, pp. 365-368.

[15] T.-J. Chiu, J. Gong, Y.-C. King, C.-C. Lu, and H. Chen, “An Octagonal Dual-Gate Transistor With Enhanced and Adaptable Low-Frequency Noise”, IEEE Electron Device Lett., vol. 32, no. 1, pp. 9-11, 2011.

[16] T. Oya, T. Asai, and Y. Amemiya, “Stochastic resonance in an ensemble of single-electron neuromorphic devices and its application to competitive neural networks”, Chaos, Solitons and Fractals, vol. 32, no. 2, pp. 855-861, Apr. 2007.

[17] S. Dietrich, M. Angerbauer, M. Ivanov, D. Gogl, H. Hoenigschmid, M. Kund, C. Liaw, M. Markert, R. Symanczyk, L. Altimime, S. Bournat, G. Mueller, “A Nonvolatile 2-Mbit CBRAM Memory Core Featuring Advanced Read and Program Control”, Solid-State Circuits, IEEE Journal of, vol. 42 (4) pp. 839-845 (2007).

[18] M. Kund, G. Beitel, C.-U. Pinnow, T. Rohr, J. Schumann, R. Symanczyk, K.-D. Ufert, G. Muller, “Conductive bridging RAM (CBRAM): an emerging non-volatile memory technology scalable to sub 20nm”, in IEDM Tech. Dig., 2005, pp. 754-757.

[19] E. Vianello, G. Molas, F. Longnos, P. Blaise, E. Souchier, C. Cagli, G. Palma, J. Guy, M. Bernard, M. Reyboz, G. Rodriguez, A. Roule, C. Carabasse, V. Delaye, V. Jousseaume, S. Maitrejean, G. Reimbold, B. De Salvo, F. Dahmani, P. Verrier, D. Bretegnier, J. Liebault, “Sb-doped GeS_2 as performance and reliability booster in Conductive Bridge RAM”, in IEDM Tech. Dig., 2012, pp. 31.5.1-31.5.4.

[20] M. Mitkova and M.N. Kozicki, “Silver incorporation in GeSe glasses used in programmable metallization cell devices”, J. Noncryst. Sol., vol. 1023 pp. 299-302 (2002).

[21] D. Ielmini, “Modeling the universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth”, IEEE Trans. Electron Devices, vol. 58 (12) pp. 4309-4317 (2011).

[22] R. Waser, R. Dittmann, G. Staikov, and K. Szot, “Redox-based resistive switching memories-nanoionic mechanisms, prospects, and challenges”, Adv. Mater., vol. 21, no. 25-26, pp. 2632–2663, Jul. 2009.

[23] M.Suri, O. Bichler, D. Querlioz, G. Palma, E. Vianello, D. Vuillaume, C. Gamrat, B. De Salvo, “CBRAM devices as binary synapses for low-power stochastic neuromorphic systems: Auditory (Cochlea) and visual (Retina) cognitive processing applications”, in IEDM Tech. Dig., 2012, pp. 10.3.1-10.3.4.

[24] D.B. Strukov, G.S. Snider, D.R.Stewart and R.S. Williams, “The missing memristor found”, Nature vol 453, no. 7191, pp.80-83 (2008)

[25] S. Yu and H.-S.P. Wong, “Compact modeling of a Conducting Bridge Random Access memories (CBRAM)”, IEEE Trans. Electron Devices, vol. 58 (5) pp. 1352-1360 (2011).

[26] G. Indiveri, B. Linares-Barranco, T. J. Hamilton, R. Etienne-Cummings, T. Delbruck, S.-C. Liu, P. Häfliger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, S. Saighi, J. Wijekoon, and K. Boahen, “Neuromorphic silicon neuron circuits”, Front. Neuromorphic Eng., vol. 5, p. 73, 2011.

[27] F. Longnos, E. Vianello, G. Molas, G. Palma, E. Souchier, C. Carabasse, M. Bernard, B. De Salvo, D. Bretegnier, J. Liebault, “On disturb immunity and P/E kinetics of Sb-doped GeS_2/Ag Conductive Bridge Memories”, accepted in IMW 2013.

[28] J. V. Arthur and K. A. Boahen, “Silicon-Neuron Design: A Dynamical Systems Approach”, IEEE Trans. Circuits Syst. Regul. Pap., vol. 58, no. 5, pp. 1034-1043, 2011.

[29] T. Sakamoto, N. Banno, Noriyuki Iguchi, H. Kawaura, H. Sunamura, S. Fujieda, Kazuya Terabe, Tsuyoshi Hasegawa, Masakazu Aono, “A Ta2O5 solid-electrolyte switch with improved reliability”, VLSI Technology, 2007 IEEE Symposium on, pp.38-39 (2007).

[30] S. Kaeriyama, T. Sakamoto, H. Sunamura, M. Mizuno, H. Kawaura, Tsuyoshi Hasegawa, Kazuya Terabe, Tomomobu Nakayam, Masakazu Aono, “A nonvolatile programmable solid-electrolyte nanometer switch”, Solid-State Circuits, IEEE Journal of, vol. 40 (1) pp.168-176 (2005).