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Dimensional Control in Corner Lithography for Wafer-Scale Fabrication of Nano-Apertures

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***Abstract*— In this paper we investigate a new method to fabricate 3D-oriented nanostructures in wafer scale, and apply it to fabricate a nano-apertures at the apex of a pyramid. A number of new technologies require the use of apertures to serve as electrical, nano fluidic or optical probes. Controlling the size of the aperture is one of the key problems in fabrication process. Our approach is based on corner lithography and offers wafer scale control of the size of the aperture in diameters less than 1µm. We show how to control the size of the nano-aperture by timed isotropic etching of silicon nitride, which serves as a mask for the aperture formation.**

Keywords: Nanofabrication, 3D, Corner Lithography, Nano-aperture, Silicon nitride, LOCOS.

I. INTRODUCTION

A number of new technologies require the use of nano fluidic apertures to serve as fountain pens [1, 2] or for biological applications such as DNA translocation and single cell experiments [3, 4,5]. Controlling the size of the aperture as well as wafer scale fabrication are the key challenges in nano aperture manufacturing. Our approach is based on corner lithography [6, 7] which utilizes the material left in concave corners after conformal deposition and isotropic back etching as nano size structures or masks. Fig. 1 shows the corner lithography from top and cross view respectively before and after etching. The height of the remaining layer depends on initial thickness Z_0, angle of the concave corner α, etchant etch rate V_e and the time of etching t,

$$h = \frac{Z_0}{\sin\left(\frac{\alpha}{2}\right)} - R \qquad (R = V_e \times t)$$

The deposited layer needs to be conformal and uniform to obtain well-defined structured in nano scale which achievable by LPCVD (Low Pressure Chemical Vapour Deposited) techniques. The issues about this technique that will be discussed in this paper are the uniformity of deposited layer before and during etching, etch rate in the corner and flat surface, size controlling and shape of the remaining material in concave corner. After that, nano-apertures as an example of applications of nano structure demonstrated by corner lithography will be presented.

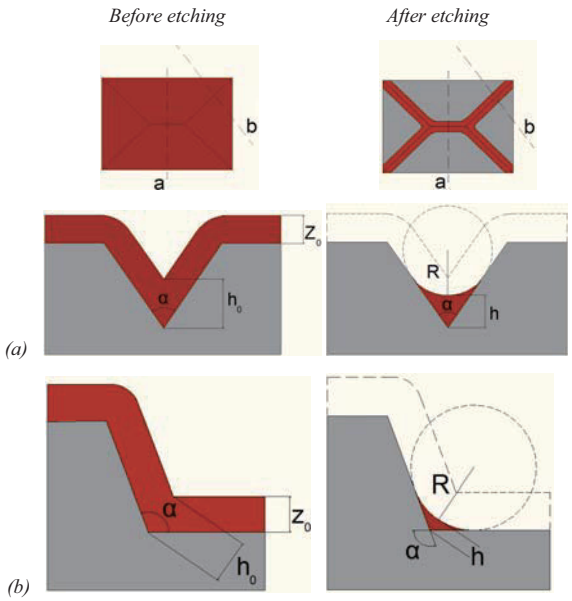

Figure 1. Corner lithography method from top and cross view: Dipositing conformal layer and ething isotropically the layer by time controlling.

The fabrication process for nano apertures is shown in Fig. 2. It starts by creating a template with concave corners and depositing a conformal layer with initial thickness of Z_0 on flat surfaces. Based on the angle of the corners, this results in a thickness of 1.78 Z_0 in the apex ($\alpha=71^0$) of the pyramid and

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1.23 Z_0 in the ribs ($\alpha=110^0$). In the subsequent isotropic back etching, the etching factor (F_e) determines the removal of respectively the material at the flat surfaces, in the ribs or in the apex. To create a nano wire pyramid [7] F_e should be between 1.00 and 1.23. For the fabrication of the nano aperture F_e should be between 1.23 and 1.78 [6]. Fig. 3 presents the corner lithography technique in steps to fabricate nano wire and dot by etching and over etching conformal layer in three dimensions. Practically in this work we chose F_e = 1.35 to have a safe margin with respect to possible non-uniformity. Silicon nitride is used as an inversion mask in LOCOS step and has high selectivity with respect to SiO_2 in etching by H_3PO_4 as an etchant in one hand. One the other hand, H_3PO_4 attacks to the Si in step (c), therefore 50% HF which doesn't etch Si as the other etchant has been selected. The main question that we address in this paper is the uniformity of the features made by corner lithography for both etchant types. We therefore study in details the isotropic back etching of the silicon nitride layer by two etchants: 50% HF and H_3PO_4 at 180 ^{0}C separately. We check uniformity of deposition, uniformity of the remaining layer and etch rate in flat layer and V-grooves and also the shape of the dot at the end of the concave corner during etching and over etching. Standard deviation of the SiN_x layer thickness is a function of initial thickness and the increase of the non-uniformity during to the etching process. The basic assumption of the corner lithography theory is that the etching is isotropic and has the same etch rate in the flat wafer surface, side wall of V-groove and concave corner. We address this experimentally by checking the etch rate in dummy wafer, thickness in side wall and height of remaining layer in concave corner in HRSEM images which are taken from device. To make the templates in silicon, we choose series of rectangular mask openings to study the V-grooves, and square mask for nano-aperture device and shift them with respect to each other.

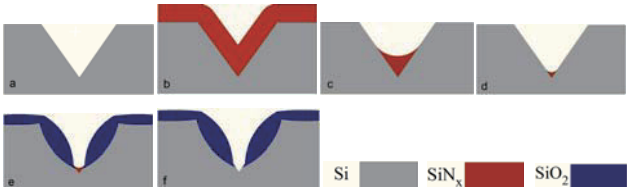


Figure 2. Fabrication process for a 3D silicon oxide pyramid with nano aperture in silicon <100>. After creating a template by KOH etching (a), depositing SiN_x as initial layer with the thickness of Z_0 (b), 1.35 Z_0 over etching in the corner(c), leaving small piece of layer at the end and using it as an inversion mask, the silicon oxide structural material for the pyramid is formed by local oxidation of the silicon (LOCOS) (d). Finally, remaining dots at the end of pyramids are removed.

Figure 3. Nano wire and dot after etching and over etching conformal layer in a 3D pyramid.

II. EXPERIMENTAL

We conducted experiments using dummy wafer and device. Dummy wafers were employed to check etch rate and uniformity of the deposited layer during etching, and device wafers to check the shape of the remaining material in the apex, etch rate in three main areas: flat surface, side wall and corner, and finally fabricate nano-apertures.

A. Uniformity in flat surface

<100> silicon wafer was selected to start with. After removing a thin layer of native oxide on the top of the wafer by 50% HF which is performed at room temperature, 250 nm low stress (silicon rich) silicon nitride was conformally deposited by LPCVD (Low Pressure Chemical Vapour Deposited). Then SiN_x layer was isotropically etched by H_3PO_4 (85 vol% solution) at 180 ^{0}C. The thickness of the remaining layer was measured every 10 min by ellipsometer in 25 points in different positions. This experiment was repeated by using 50% HF at room temperature instead of H_3PO_4 as a different etchant.

B. Shape of the remaining material

To start, series of 5µm×10µm and 10µm×20µm rectangular were drawn on the mask. After wet oxidation of a <100> silicon wafer (200 nm SiO_2), the rectangular patterns were consecutively transferred to a spin-coated resist. The uncovered oxide was etched with a buffered hydrofluoric (BHF) acid solution. The oxide layer served as a mask for potassium hydroxide etching (25% w/w KOH at 75 ^{0}C) and was finally removed by 50% HF to obtain v-grooves bounded by the <111> planes. Then 250 nm low stress silicon nitride SiN_x as an initial thickness Z_0 was conformally deposited by LPCVD. We employed dummy wafer with the same thickness to check etch rate of silicon nitride in parallel. Next SiN_x, was isotropically etched by 50% HF at room temperature. We observed SiN_x shape at the apex by HRSEM before etching and after removing 100, 150, 250, 308 and 338nm layer with F_e= 0.0, 0.4, 0.6, 1.0, 1.23 and 1.35 respectively. We repeated the process with H_3PO_4 at 180 ^{0}C as different etchant.

C. Nano-aperture

Series of squares with the size of 5µm×5µm and 10µm×10µm were defined as pattern on the mask. The basic processing steps are shown in fig.2. After creating a template by KOH etching with series of square with the size of 5µm×5µm and 10µm×10µm as a patterning mask (a), depositing 250 nm SiN_x as initial thickness Z_0 (b), 308 nm as F_e=1.23 removed by 50% HF at room temperature (e). Over etching of the SiN_x in the corner is continued to reach the dot at the end with F_e=1.35 by removing 30 nm layer and small piece of layer at the end is left to use it as an inversion mask (d). Next, the silicon oxide structural material for the pyramid is formed by local oxidation of the silicon (LOCOS) at 900 ^{0}C for 180 min which gives 500 nm layer as a result (e). Finally, remaining dots at the end of pyramids are removed by H_3PO_4 at 180 ^{0}C (f). By choosing F_e below 1.23Z_0 for nano wires in the four oblique ribs of the pyramid and below 1.78Z_0 for dots, accurate control of the size is achievable. The rate of the removing SiN_x layer was controlled by dummies.

III. Results and Discussions

Fig. 4 shows SiN_x etching as a function of time for etching of the dummy wafers. The error bars in each point indicates variation of the measured thickness in all positions in wafer which has defined as standard deviation. Before starting etching, the deposited SiN_x was quite uniform in 50% HF and H_3PO_4 at 180 ^{0}C both. During etching the standard deviation of the thickness of the remaining layer only increases slightly. Also etch rate for both etchants during etching is constant. Fig. 5 shows the increase of the standard deviation of the layer thickness (on flat surfaces) as a function of etching time. This standard deviation results in an effective error in F_e of 0.04 ($3\sigma/Z_0$) therefore F_e = 1.35 ±0.04 (based on the assumption that linear trend in sigma continues). This shows that it is possible to be well in the required range $1.23 \leq F_e \leq 1.78$ needed to create a nano-aperture. To check the uniformity and size of the remaining SiN_x in the concave corner, one needs to check etch rate at that point. Therefore, many samples were observed by HREM during etching and over etching. Size of the remaining SiN_x in side wall and apex were measured by HRSEM images. Fig. 6 shows the thickness in the apex and side wall during the etching time, as compared to the etch rate in the flat surface (measured by dummy wafer). The same etch rate was found in those areas indicate by the same slope of the graph. This uniformity in etch rate was found for both etchant types. It indicates that the size of SiN_x at the apex all over the wafer can be well predicted in both etchants. The shape of the remaining material (in grooves) after F_e = 1.00 and F_e = 1.35 is shown in fig. 7. We investigate differences in size and shape of dots by using 50% HF or H_3PO_4 at 180 ^{0}C in HRSEM images. The shape of the material left is as expected for etching in H_3PO_4, but shows a considerable deviation for etching in 50% HF. A possible explanation is attacking 50% HF to the Si and SiN_x interfaces. Fig. 8 shows the resulting nano-aperture after complete of the procedure of fig.2.

I. Conclusion

We have investigated a reproducible method in wafer scale to obtain three dimensional nano structures which are quite uniform and compatible with geometrical expectation and presented nano-apertures fabrication as an example of application of this method. An important result from the presented work is that it is possible to well control both uniformity of deposition and removal layer in flat surface and ribs for both etchant types investigated. This approach could be used in a wide range of micro-electromechanical systems applications that require the fabrication of tips or pyramidal pits.

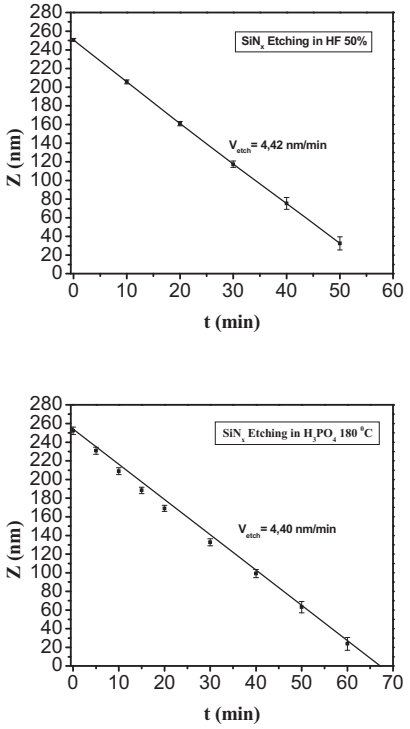


Figure 4. SiN_X etching by 50% HF and H_3PO_4 180 ^{0}C in flat surface.

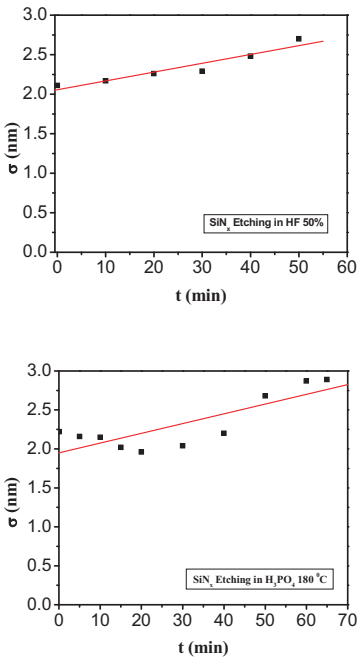
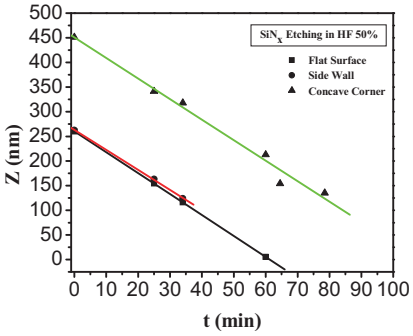


Figure 5. Standard deviation of remaining SiN_X layer after deposition and during etching by 50% HF and H_3PO_4 180 ^{0}C in flat surface.



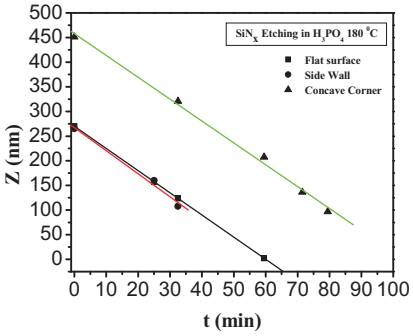


Figure 6. SiN_X layer after deposition and during etching by 50% HF and H_3PO_4 180 ^{0}C in flat surface, side wall and concave corner.

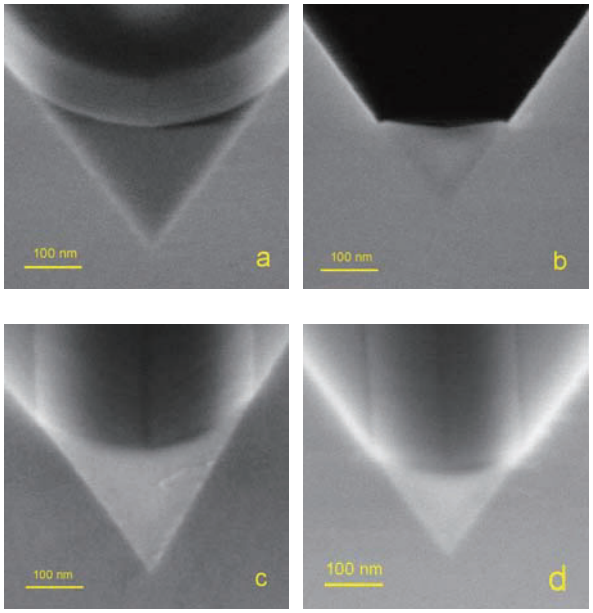


Figure 7. HRSEM micrographs of nano dots after etching and over etching ($1Z_0$, 1.35 Z_0) with HF 50% (a, b) and H_3PO_4 at 180 ^{0}C (c, d). all the scale bars are 100 nm.

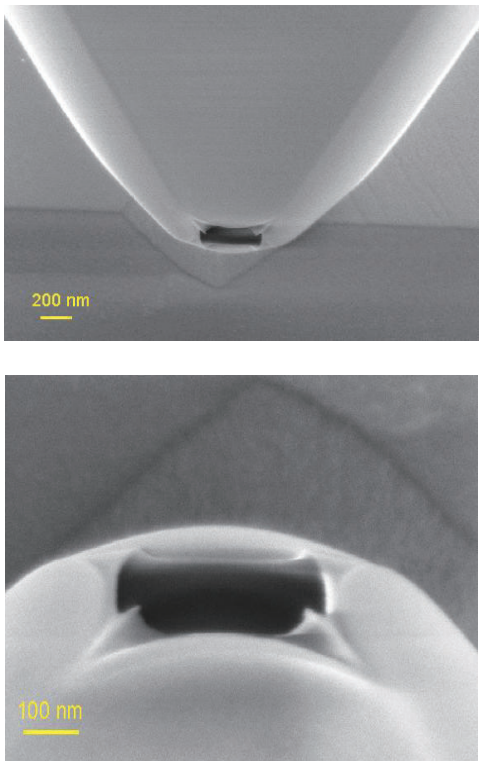


Figure 8. HRSEM micrographs fabricated nano aperture. The pyramidal nano aperture made of a 500 nm thick silicon oxide after etching and over etching 338nm silicon nitride in the concave corner.

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