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Fabrication of 2D-Extruded Fractal Structures Using Repeated Corner Lithography and Etching

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***Abstract*-We present a new wafer scale fabrication procedure for the creation of complex 2D-extruded geometries in silicon by a combination of repeated anisotropic etching of silicon and a 3D lithographic technique called corner lithography. Using corner lithography it is possible, by means of a nano-masking step, to select which corners are opened, depending on specific angles relative to the substrate normal. In this way complex 3D structures can be created in a repetitive manner. In this article we apply this procedure to the etching of trench like structures in a <100> silicon wafer. Depending on which angles open in corner lithography, it is possible to etch just downward, downward and sideward, or a sequential combination of these two options. Examples of all three routes have been created on a micron/sub-micron scale. By depositing a conformal layer, the smallest hollow features will be auto-closed, thus forming buried channels. Continuing this deposition, automatically new closed channels will be formed with increasing diameter and wall thickness. These channel structures could find application in e.g. continuous flow microreactors.**

I. Introduction

The crystalline properties of silicon allow anisotropic etching, when etchants like KOH and TMAH are used. For concave etched structures typically the cavity will be bound by slow etching of crystal planes, in silicon these are often the {111}-planes using the mentioned etchants. Recently we introduced a new nanofabrication procedure [1], where we combine repeated anisotropic etching of silicon with a new 3D-nano-patterning step called corner lithography [2-4] to create 3D-engineered fractals in a self-multiplying process (fig. 1). In corner lithography, material is left in sharp concave corners after conformal deposition and subsequent isotropic etching of the material [2]. Through an inversion this can result in the creation of apertures or slits in these corners [3, 4]. Interestingly the amount of material left in these corners depends on the angle between the intersecting planes, which means that through the isotropic etch factor one can choose in which corner material will be left. Here we use this property to control the global directionality of the etching process in a repetitive procedure, as illustrated in fig. 2. The etched structures can be closed by depositing a conformal layer as a last step. This way, one or several parallel so called buried channels [5] can be formed. Microchannels are key elements in continuous flow microreactors [6], heat pipe cooling systems [7], counterflow heat exchangers [8] and chromatographic systems (including LC, GC, CE) [9-11].

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II. Experimental

The fractal process (fig. 2) starts with a conversion of a flat (100) single crystalline silicon wafer into a surface with V-grooves bounded by two (111) planes using a grating pattern (50 μm lines with 100 μm periodicity) of SiO_2 stripes followed by KOH etching. The 100 nm thick thermally grown oxide masking layer is patterned in buffered hydrofluoric acid (BHF) using a resist mask. After stripping the resist mask, the unprotected silicon is anisotropically etched in KOH (25 wt% @ 75°C) resulting in V-grooves with a depth of around 35 μm. After stripping the remaining oxide mask (fig. 2a), the wafer is uniformly coated with 200 nm of low-pressure chemical vapor deposited (LPCVD) silicon nitride (fig. 2b). The next step of the first sequence (most left in fig 2) is corner lithography: partly remove the nitride in hot phosphoric acid (85% H_3PO_4 @ 180 °C), to leave only nitride material in the V-groove (fig. 2c). The etching time was tuned to result in 35% over-etch (etch factor 1.35). Next, silicon is locally oxidized into 80 nm SiO_2 using the nitride as a mask (fig. 2d); applying the so-called LOCal Oxidation of Silicon (LOCOS). The nitride in the V-groove is stripped (fig. 2e). Then the unprotected silicon in the V-groove is etched anisotropically for 144 min, using tetra methyl ammonium hydroxide (TMAH). This forms a single 2D

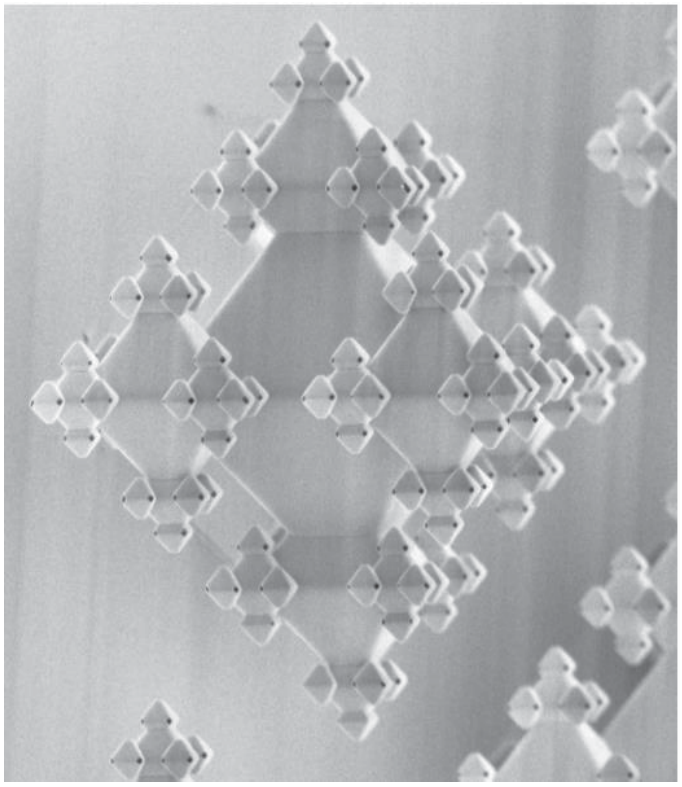

Fig. 1: Micron-sized octahedral fractal [1].

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extruded quadrangle shaped feature at the bottom of the V-groove (fig. 2f). Its size is determined by the <111> silicon etch rate (about 15–20 nm·min^{-1}). Then the LOCOS oxide is stripped and around 100 nm nitride is deposited. The process mentioned above is repeated to create the first generation or level of substructures (fig. 2 2nd and 3rd column). Two options are possible: etching down and side-ward (etch factor 1.0) or just downward (etch factor 1.35). This is determined by the angle of the different corners involved in the corner lithography step: 71° in the V-groove and 110° in the side corners. Fig. 3 illustrates the development of subsequent generations of sub-structures. The two routes can also be combined: first etching repeatedly downward, and in the final step downward and side-ward. This leads to the more complicated structure in the 3rd column of fig. 3.

To create buried channels, a wafer with a grating pattern (4 μm wide V-grooves, periodicity of 8 μm) and a first generation of substructures was coated with a conformal layer of low stress LPCVD silicon nitride. The substructures were etched in TMAH for 20 min using a corner lithography etch factor of 1.0 based on a silicon nitride thickness of 142 nm and a LOCOS layer of 50 nm. The conformal silicon nitride layer is 600 nm thick. This first closes the side ward etched features I) and II), as shown in the left image of fig. 4, because these have the smallest opening to the outside world after the corner lithography inversion step. Next, feature III) will be closed followed by the closure of feature IV). Important to emphasize is that once the buried channels are closed, the deposition in these channels will stop automatically. By measuring the thickness of the channel wall the slit size through which the material is deposited could be determined. Ideally, the slit size should be two times the wall thickness.

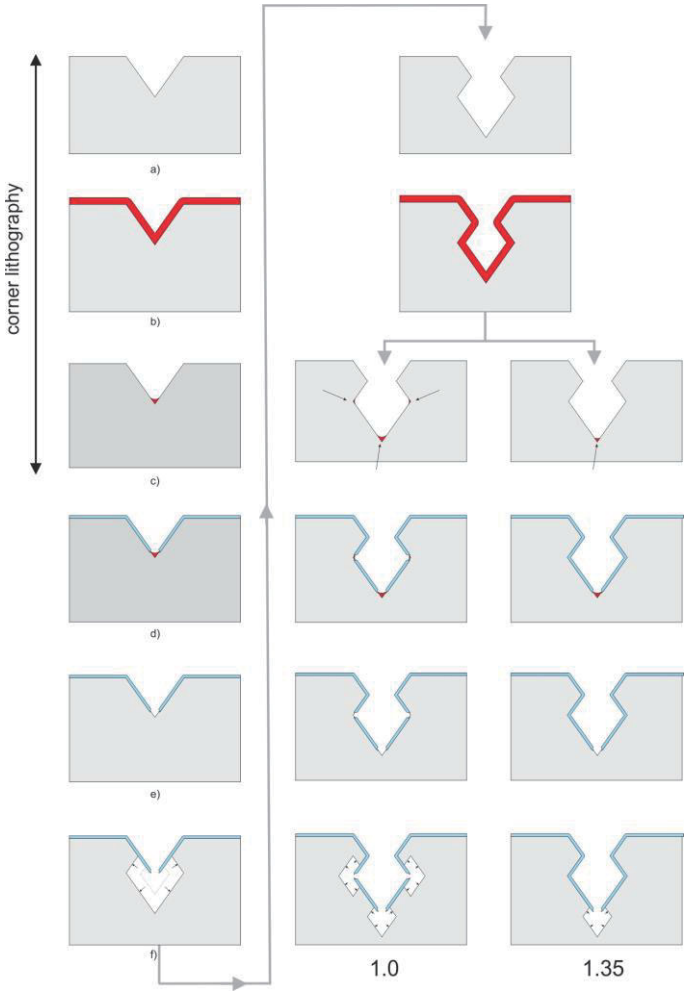


Fig. 2: Fabrication process of the first sequence (left), first generation of substructures by etching down and side-ward using etch factor 1.0 (middle) or just downward using etch factor 1.35 (right).

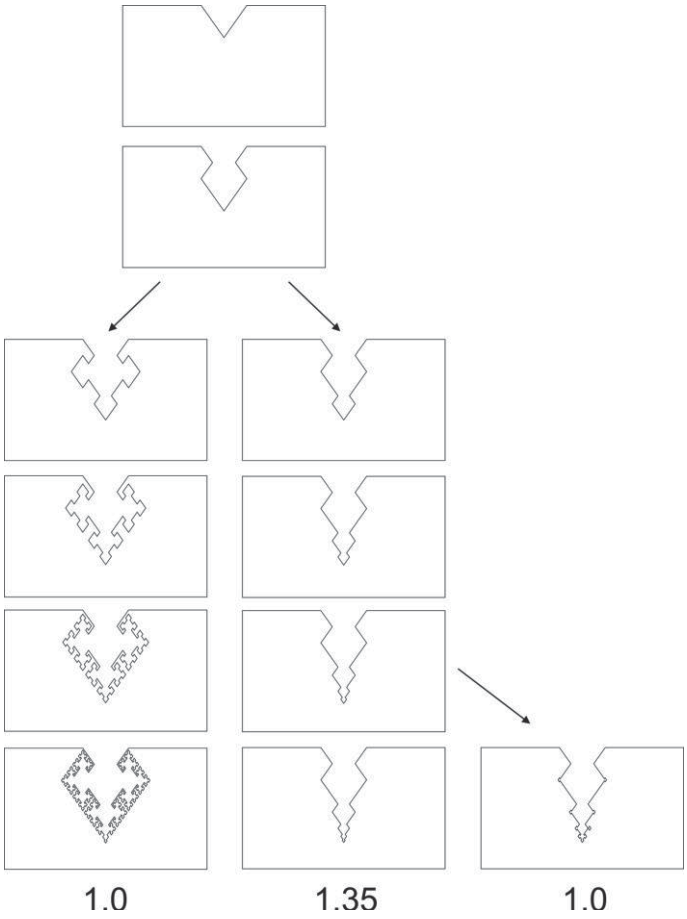


Fig. 3: Structures evolving depending on corner lithography etch factor.

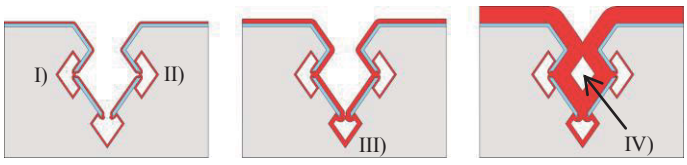


Fig. 4: Buried channels are sequentially formed by conformal layer deposition. Increasing the layer thickness will close feature I) and II) first (left), followed by III) (middle) and finally IV) (right).

III. RESULTS & DISCUSSION

Fig. 5 shows the etched structures using an etch factor 1.0 (left column) and 1.35 (right column). A close-up of a right column structure after generation 4 has been created is shown in fig. 6. The last generation quadrangle has a width of only 400 nm. Following the procedure of the 3rd column fig. 3 we continued etching this structure using a final etch factor of 1.0. The resulting structure is shown in fig. 7. Sideward etching occurs from corners in all generations of quadrangle structures as expected.

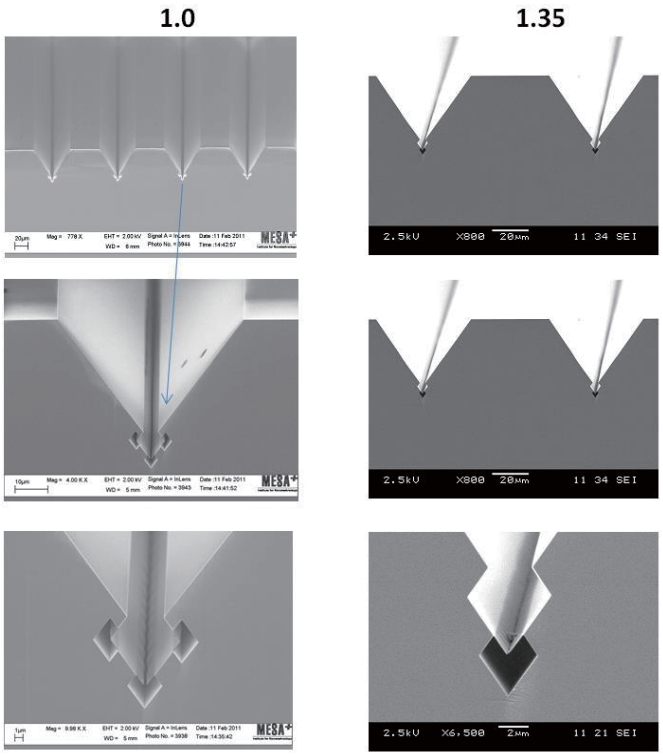


Fig. 5: Structures etched using factor 1.0 (left) and 1.35 (right).

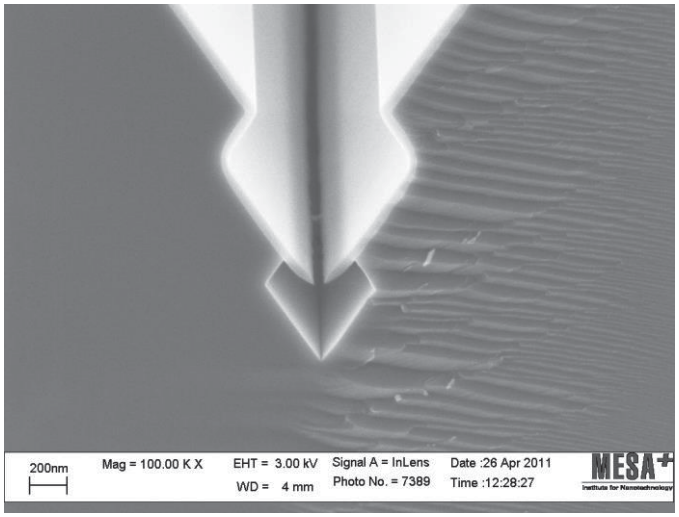


Fig. 6: 4th generation structure (etch factor 1.35).

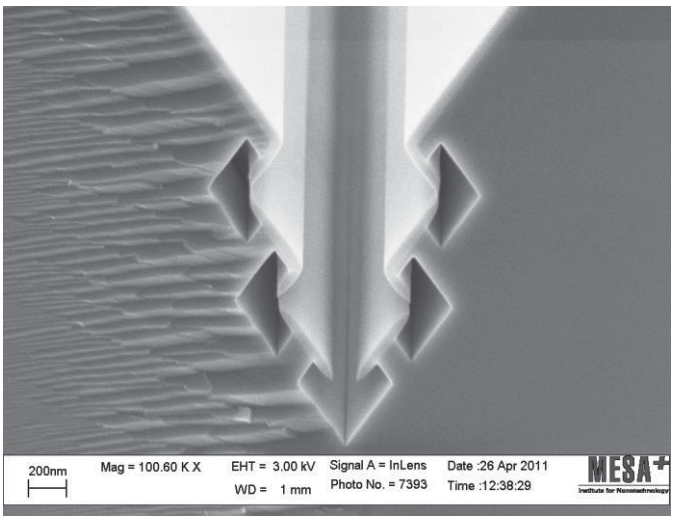
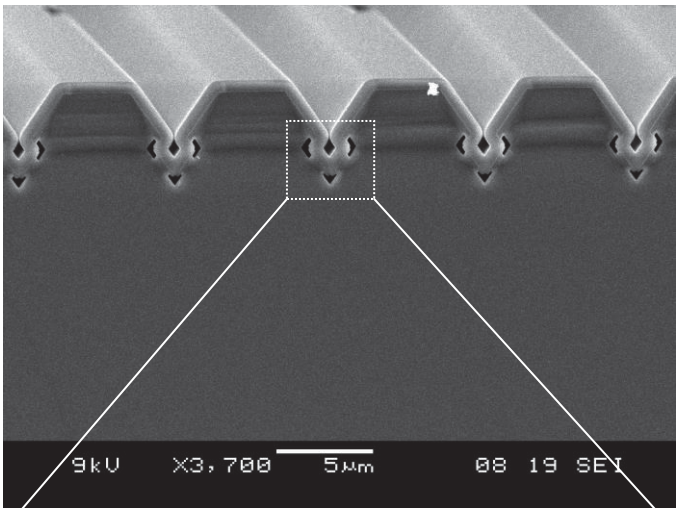


Fig. 7: Structure fig. 6 etched with etch factor 1.0 in final step.



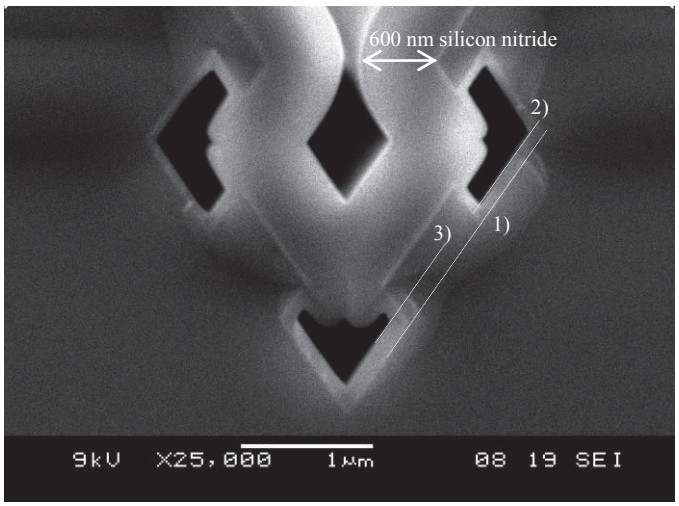


Fig. 8: Structures as shown in fig. 5 (left) after closure of the smallest sub-structures by deposition of a 600 nm silicon nitride conformal layer

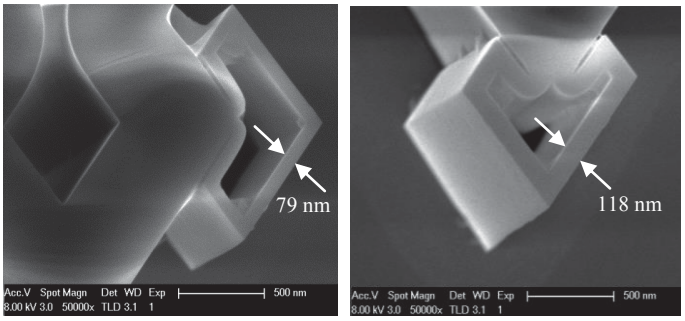


Fig. 9: Zoom-in of the side (left) and bottom (right) sub-structures after closure of the channels. Note that the thickness of the conformal coating in both sub-structures is different and seems to be related to the slit size through which the material is deposited.

To show the buried channel formation by conformal depostion, structures as shown in fig. 5 (left) are coated. Successfull closure of the smallest substructures (see fig. 4 I), II) and III)) is shown in fig. 8. Fig. 8 (bottom) shows that a deposition of 600 nm silicon nitride was not enough to close feature IV). After anisotropic etching through the oxide slit to create the first generation, both side ward and downward etched substructures are nicely in line with each other as shown by the dotted line 1). This because they are formed at the same time. The dotted lines 2) and 3) accentuate the difference in resulting thickness of the conformal closing layer for the substuctures II) and III). In fig. 9 this difference is shown in more detail. To precisely measure the layer thickness, the cross section of the features was etched in TMAH for 15 min. just after breaking the sample. According to ref. [12] the theoretical size of the width of the slit through which the material is deposited and based on etch factor 1.0 equals $a / t = (2/3)\sqrt{6}$ for the 71° in the V-groove, and $c / t = (2/3)\sqrt{3}$ for the 110° in the side corners (where t is the thickness of conformal deposited layer). The deposited nitride thickness (t) for the corner lithography step to create the first generation of substructures was 142 nm. This should result in a = 232 nm, c = 164 nm, meaning a conformal layer of 116nm and 82 nm respectively to close the channels. The measured values are around 118 nm and 79 nm. This is in reasonable agreement with the calculated values. Interestingly, through this relation between the slit size and the resulting coating thickness, wall thickness of sub-structures can be tuned independent of the wall thickness of the primary tube. For example, this enables the creation of small thin walled channels supported by a relative thick walled main channel.

IV. Conclusions

It was shown that rather complex extruded 2D structures can be generated in silicon by a combination of repeated corner lithography and anisotropic etching of the silicon. The directions in which these structures develop can be steered by the etch factor in the corner lithography steps. These structures can be closed to form so-called buried channels. We expect that these structures may find application in microchannel based reactors, lab-on-a-chip devices, and flow based heat transfer devices.

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