Nanogap Device Engineering for Electrical Characterisation of Molecular Components

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Abstract*— For the development of molecular electronics, it is essential to measure the electrical characteristics of individual molecular components without altering their structures. This work concerns engineering closely packed identical nanogap devices, that are capable of electrical characterisation of sub-10 nm molecular components. The fabrication process involves growing a GaAs-AlAs-GaAs wafer by molecular beam epitaxy, where the thickness of the AlAs middle layer determines the primary nanogap width. Mesas separated by trenches are patterned on the wafer by reactive ion-beam etching to a depth below the AlAs layer. Some of the AlAs layer is selectively etched, resulting in identical shallow cleavages on the mesa walls. Nanogap devices are constructed by evaporating a network of thin and narrow NiCr/ Au wires crossing the etched mesa cleavages. This step also controls the final nanogap width. The fabricated nanogap devices are used for electrical characterisation of 7 nm wide CdSe nanocrystals, and negative differential resistance behaviour is observed.

Keywords—molecular electronics, electrical characterisation, nanogap device, nanocrystal, negative differential resistance.

I. Introduction

There is an increasing demand for feature size reduction in electronic circuit components. However, silicon-based electronics is almost at its minimum feature size limit due to inherent physical constraints [1]. By using molecular electronics, it is theoretically possible to improve feature density since electronic switches, diodes, transistors and storage elements from single molecules would require much less space than equivalent devices made out of silicon-based materials. In addition, in molecular electronics, it is possible to change the electronic properties of a component by manipulating its chemical structure. The sensitivity of a molecular component to changes in voltage, magnetic field or light can be controlled and a desired functionality can be integrated to the circuit.

The current molecular electronic devices are mainly hybrid devices, where the junction electrodes for molecular components are made of inorganic conductors or semiconductors [2]-[4]. The main challenge to realise hybrid devices is to fabricate an electrical junction between electrical contacts, which is small and reliable enough for characterising molecules and nanometre scale structures, such as quantum dots and nanocrystals [5]. There have been many different approaches to construct nanometre scale electrical junctions, i.e. the nanogap devices, including scanning probe methods [6], electron beam nanolithography [7], selective etching [8][9], the junction break method [10], electromigration [11], and thermal evaporation [12]. However, reproducible mass-production of $\mathrm{sub}-10\,nm$ nanogap devices remains a challenge.

In this work, reproducible fabrication of closely packed identical $\mathrm{sub}-10\,nm$ nanogap devices is demonstrated. A GaAs-AlAs-GaAs wafer was grown by molecular beam epitaxy (MBE). Two mesas were etched on the wafer by reactive ion-beam etching (RIE). A network of nanogaps on the mesa walls was constructed by selective etching some of the AlAs layer, whose thickness defines the primary nanogap width. Nanogap devices were constructed by depositing nichrome (NiCr) and gold (Au) wires across the nanogaps by thermal evaporation. Therefore, the initial nanogap width was defined by MBE, but the final nanogap width was determined by thermal evaporation.

The nanogap devices were examined under an XL-30 scanning electron microscope (SEM). A bonded chip hosting a GaAs-AlAs-GaAs wafer with nanogap devices was used for electrical characterisation of $7\,nm$ wide spherical CdSe nanocrystals. The nanocrystals were anchored across nanogaps by 1,6-hexanedithiol linker molecules [12] prior to electrical characterisation, which was carried out by a Keithley 236 Source Measurement Unit (SMU) connected to the terminals of the bonded chip.

II. Fabrication Of Nanogap Devices

A. Wafer Processing and Patterning

The first step of constructing nanogap devices involves growing a wafer by MBE, which has a structure of a $500\,nm$ thick gallium arsenide (GaAs) bottom layer, a $10\,nm$ thick aluminium arsenide (AlAs) middle layer, and a $200\,nm$ thick GaAs top layer. The thickness of the AlAs layer defines the initial nanogap width, thus, MBE provides atomic precision to nanogap fabrication, and also makes it possible to manufacture closely packed identical nanogaps on a single wafer, which is essential to mass-production.

The wafer patterning process was carried out by lithography. Two mesas were patterned on a GaAs-AlAs-GaAs wafer by UV lithography and etched by RIE to a depth below the AlAs layer. The wide chip wires were patterned by UV lithography, and the nanometre-scale narrow wires were patterned by exposing a poly(methyl methacrylate) (PMMA) photoresist-covered wafer to an electron beam, in Fig. 1. There are nine narrow wires crossing over two mesas so that a wafer has 18 nanogap devices. After the patterning process, the wafer was dipped into 20% hydrochloric acid (HCl) for 15 seconds to etch away the surface oxide layers and other undesired residues. To remove HCl from the wafer surface, the wafer was rinsed with deionised water. This was followed by bonding each patterned wire on the sample to a gold pad of a wafer package at $90^{o}C$ via a gold wire. Consequently, one pad was connected to one nanogap.

In order to define the initial nanogap, the patterned wafer was immersed in buffered hydrofluoric acid (HF) for two minutes. HF selectively etches the exposed AlAs layer, forming a groove that is $10\,nm$ wide, which is determined by

the thickness of the AlAs layer. The etched wafer was then washed in deionised water and dried with nitrogen gas.

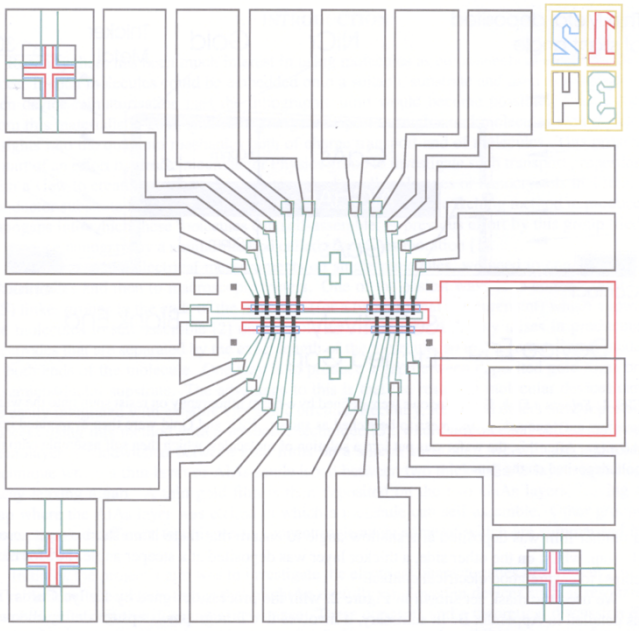

Fig. 1. The lithographic mask with the chip pattern. The red lines in the middle of the mask define the two RIE etched mesas. The small black lines on either side of the mesas are for depositing the narrow wires crossing over the mesas, defining the nanogaps on the side walls of the mesas. The large grey layers and the smaller green layers are for metal deposition to form contacts to the nanogaps. Only the small black lines are defined by e-beam lithography and the other patterns are defined by UV lithography.

B. *Depositing Nanogap Contacts*

The NiCr and Au electrodes were evaporated thermally by an Edwards Auto 306 thermal evaporator system, fitted with a rotating mechanism and an Edwards FTM-5 film thickness monitor (FTM). The latter measures the metal deposition rate and the deposited metal thickness during evaporation.

Prior to evaporation, the wafer package walls were covered by a thin copper paper. This prevents the bonding pads from getting shorted. The paper was removed after the evaporation process was completed. The first step in evaporation was to clamp the chip hosting the wafer onto the deposition stage with the correct orientation. After mounting the chip, the stage angle controller was calibrated in order to reduce uncertainty in the tilt angles. Solid nichrome particles were placed in a ceramic crucible and solid gold particles were placed in a tungsten crucible. In order to eliminate potential contamination of the nanogap devices by the impurities present in the metals, when the vacuum was better than $1x10^{-5}\ mbar$, the nichrome and gold were heated resistively one after the other until they started to evaporate, while keeping the evaporator shutter closed. The actual deposition was carried out under vacuum conditions better than $1x10^{-6}\ mbar$. For each layer deposited, five different deposition angles were used, one vertical and two oblique angles for either side of the two parallel mesas, Fig. 2. Nichrome was evaporated first and gold second. Nichrome provides adhesion between GaAs and gold wires.

When the metal deposition steps were completed, the chamber was left to return to room temperature while in vacuum before the chip was removed from the chamber. A period of 15 minutes was allowed for this cooling step. Immediately after retrieving the chip with the metallised wafer, it was immersed in acetone overnight to lift-off the remaining photoresist, before being cleaned in isopropyl alcohol and dried with nitrogen gas, ready for SEM imaging and for electrical characterisation.

C. *Deposition Geometry for The Mesa Walls*

The deposition geometry of mesa walls is shown in Fig. 2. The side where the nanogap is constructed is called the active mesa wall. The deposition angles associated with the active mesa wall are θ_1 and θ_2. The former is called the shallow angle and the latter is called the steep angle, since $\theta_2 < \theta_1$. Most of the metal deposition on the mesa wall comes from the shallow angle evaporation. The primary use for the steep angle evaporation is to improve step coverage at the mesa wall and trench junction. The relationship between the metal thicknesses, θ_1 and θ_2 is

$$h_R = t_1 \sin\theta_1 + t_2 \sin\theta_2 \quad (1)$$

$$h_G = t_1 \cos\theta_1 + t_2 \cos\theta_2 \quad (2)$$

where h_G is the total thickness of the evaporated metal on the bottom edge of the nanogap in the vertical direction, h_R is the thickness of one metal layer on active mesa wall, t_1 and t_2 are the deposition thickness readings from the FTM, associated with shallow angle evaporation and steep angle evaporation respectively.

The nanogap needs to be wider than a given critical deposition height (h_C) on the bottom edge of the gap in the vertical direction such that

$$h_{G\,|\,Au} + h_{G\,|\,NiCr} < h_C \quad (3)$$

where $h_{G\,|\,Au}$ is the gold deposition thickness on the bottom edge of the nanogap in the vertical direction and $h_{G\,|\,NiCr}$ is the nichrome deposition thickness on the bottom edge of the nanogap in the vertical direction. This lower limit to nanogap width depends on the tunnelling current and on the size of the nanocrystals used for electrical characterisation inside the nanogap. The nanogap should be wide enough that the tunnelling current across the nanogap is negligible. In addition, the nanogap needs to be wide enough to accommodate a nanocrystal with linkers attached to it. For given angles and for given values of $h_{G\,|\,Au}$ and $h_{G\,|\,NiCr}$, t_1 and t_2 for gold and t_1 and t_2 for nichrome can be calculated from (1) and (2), while ensuring that (3) is satisfied.

The shallow and steep angles for the other side of the mesa wall, called passive wall, are θ_3 and θ_4 respectively, Fig. 2. The equations for the passive wall, are analogous to (1) and (2), such that

$$h_{R|\,pass} = t_3 \sin\theta_3 + t_4 \sin\theta_4 \quad (4)$$

$$h_{G|\,pass} = t_3 \cos\theta_3 + t_4 \cos\theta_4. \quad (5)$$

The etched groove on the passive side needs to be electrically shorted in order to have a continuous wire. Therefore, for an etched groove that is $10\ nm$ wide, the condition for the wire continuity is

$$h_{G\,|\,pass\,|Au} + h_{G\,|\,|\,pass\,|\,NiCr} > 10\ nm. \quad (6)$$

The evaporation values used are

$$\theta_1 = 65^o, \theta_2 = 10^o, \theta_3 = -15^o, \theta_4 = -60^o \quad (7)$$

$$h_{G\,|\,Au} = h_{G\,|\,NiCr} = 2\ nm \quad (8)$$

$$h_{G\,|\,pass\,|Au} = h_{G\,||\,pass\,|\,NiCr} = 5\ nm. \quad (9)$$

By using the values given above, it can be shown that

$$h_{G\,|\,Au} + h_{G\,|\,NiCr} = 3\ nm \quad (10)$$

$$h_{G\,|\,pass\,|Au} + h_{G\,||\,pass\,|\,NiCr} > 10\ nm. \quad (11)$$

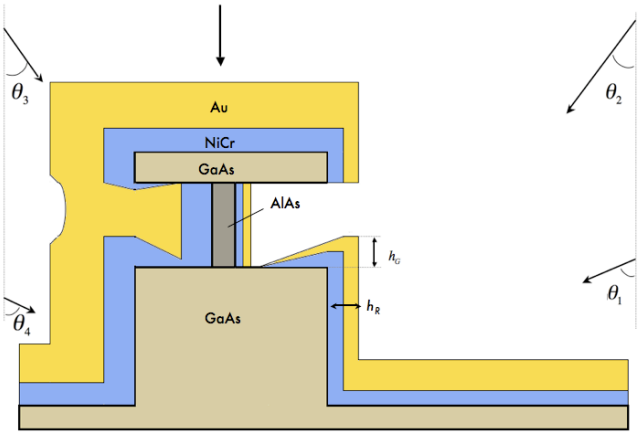

Fig. 2. The schematic of deposition geometry used for processing active and passive walls of a nanogap. The angles shown are the five different deposition angles used for each layer of metal. The fifth angle is for the vertical evaporation (vertical with respect to the mesa-top surface), i.e. it is equal to zero.

Equation (10) shows that the nanogap width at its narrowest point is $7\ nm$. This is wide enough for the tunnelling current to be negligible, since the tunnelling current is an inverse exponential function of this distance. This nanogap width is not expected to present any problems for accommodating a $7\ nm$ wide CdSe nanocrystal with $1.2\ nm$ linker molecules on either side, since the nanocrystals do not need to be completely inside the nanogap for electrical characterisation. In addition, (11) shows that the etched groove on the passive wall is completely filled, ensuring wire continuity.

D. Effects of The Lift-off Process

The narrow electrodes contacting the nanogaps are only a few nanometres thick and $10 - 40\ nm$ wide. Thus, the lift-off critical during the fabrication process. Two different nanogap samples are shown in Fig. 3. In the first sample, Fig. 3 (a), the deposition rates (D) were kept at minimum possible values at $D_{Au} \leq 0.1\ nm/s$ for gold and $D_{NiCr} \leq 0.1\ nm/s$ for nichrome. It is clear that the lift-off was not successful for this sample, since the thin wire was stripped off. The slow deposition rate means that the sample was exposed to the hot crucibles for a much longer time than usual, causing the photoresist to flow. This could have closed the narrow gap between the wires before much metal was deposited, so the rest could have got lifted off.

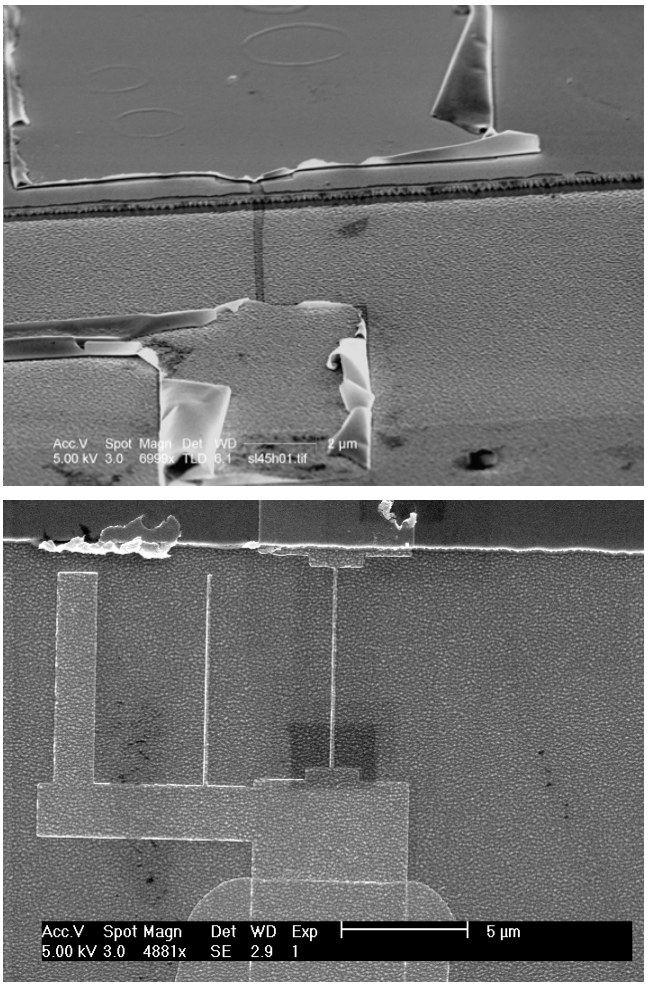

Fig. 3. Two different nanogap samples after the lift-off process. (a) Evaporation with the gold deposition rate of $D_{Au} \leq 0.1\ nm/s$ and with the nichrome deposition rate of $D_{NiCr} \leq 0.1\ nm/s$, both at $300\ K$. (b) Evaporation with $D_{Au} = 0.1\ nm/s$ and $D_{Au} \leq 0.2\ nm/s$, both at $300\ K$.

In the second sample, Fig. 3 (b), the metal deposition rates were $D_{Au} = 0.1\ nm/s$ and $D_{NiCr} \leq 0.2\ nm/s$. For these deposition rates, the wires survived the lift-off step. The subsequent yield of narrow wires was quite high, on average more than 14 out of 18 per wafer. Notice that only one narrow wire per terminal is required. Therefore, only the narrow wire on the rightmost-hand side is used for electrical conduction. The other two wires, one narrow and one slightly wider, were patterned for examining the effects of lift-off process. This is why they are not forming continuous wires.

In some samples, the narrow wires were shifted away from the active mesa wall in the direction orthogonal to the mesa wall, Fig. 4. Consequently, a section of the wide metal wire was crossing the active wall instead of the narrow wire. This is due to the misalignment during the e-beam process, since the positioning of the narrow wires is determined by e-beam. In the misaligned samples, the wide wires are forming the nanogap devices rather than the designated narrow wires. The wider the wire crossing over the nanogap, the higher the probability of fluctuations in the nanogap size and the more likely that the nanogap is short-circuited. The electron beam alignment is thus crucial in nanogap device fabrication. It requires accurate alignment marks, detection of these marks and a very precise pattern placement.

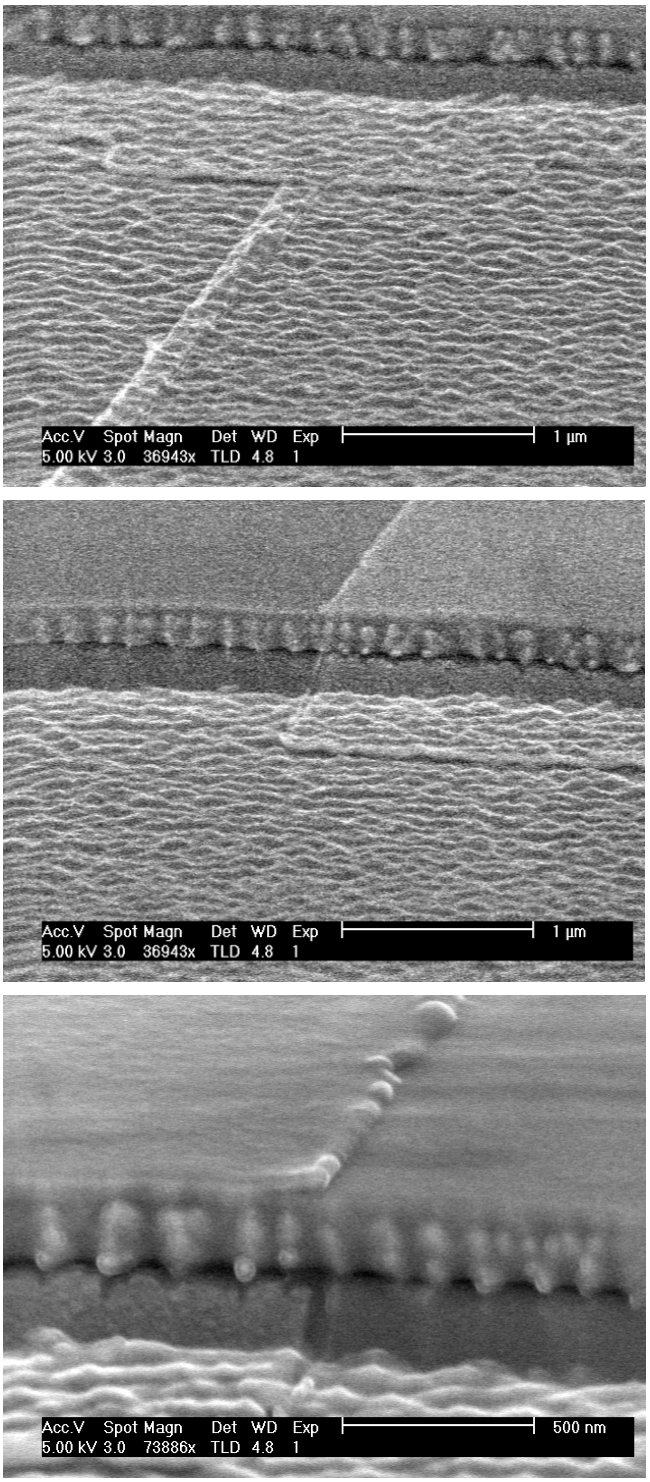

Fig. 4. The fluctuations in the nanogap edges. These are SEM images from the sample evaporated with $D_{Au} = 0.1\ nm/s$ and $D_{Au} \leq 0.2\ nm/s$, both at $300\ K$. The e-beam was misaligned for this sample. In (a) the narrow wire is clearly visible. In (b) both metallised and non-metallised regions of the mesa wall are visible. In (c), the difference in smoothness on the lower half of the mesa wall between the metallised region on the left-hand side and the non-metallised region on the right-hand side are visible.

In general, the size variation along the nanogap is not likely to influence the current-bias voltage response of the nanogap device, provided that there is no short-circuit between the two metal layers on either side of the nanogap. This is because the tunnelling current depends exponentially on nanogap width and it requires a very narrow gap to have any effect on the current readings. However, the misaligned samples were not used for electrical characterisation measurements.

The trench surfaces of the wafer shown in Fig. 4, appear to be very rough. This is very likely to be due to RIE. The mesa tops are protected by a mask during the RIE process and they appear to be very smooth. There is a difference in the roughness levels of the top half and the bottom half of the mesa walls, the former being much rougher. The blob-like features on the rough top half of the mesa walls might be due to the polymer deposition during the RIE. These features may cause fluctuations in the size of the nanogaps.

A bonded chip containing 18 nanogap devices is shown in Fig. 5.

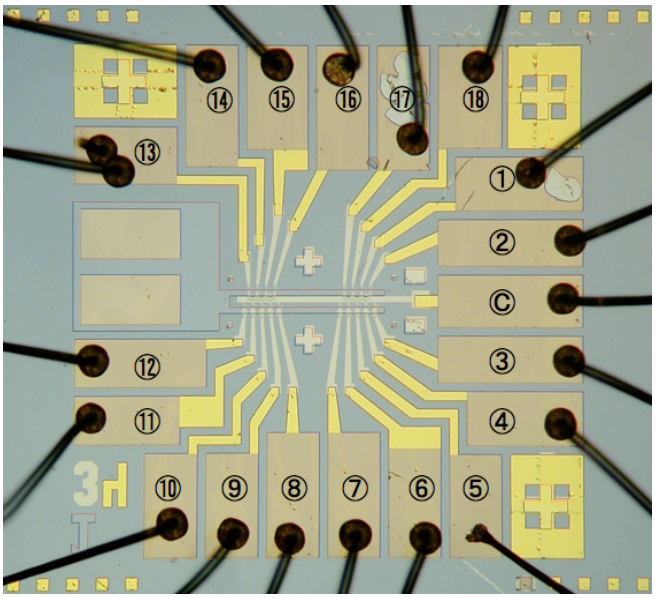

Fig. 5. A bonded chip after evaporation and lift-off processes. Every channel associated with a nanogap is numbered. The common lead is labelled with ©.

E. Trapping CdSe Nanocrystals to Nanogaps

After the metal evaporation and lift-off processes carried out, 1.2 *nm* long 1,6-hexanedithiol molecules were used as linkers to anchor them to the gold wires, so that CdSe nanocrystals got assembled into the nanogaps. First, the chip was immersed in a solution of 1,6-hexanedithiol in isopropanol (IPA) for approximately 20 hours in the dark at room temperature. During this step, the bifunctional linker molecules self-assemble on the gold surfaces of the wafer. Then the wafer was rinsed with IPA prior to being immersed in a solution made of toluene and trioctylphosphine oxide (TOPO) covered CdSe nanocrystals for another 20 hours. During this step, the exposed thiol end-groups bind to the surface of the nanocrystals, displacing some of the TOPO molecules there. This was followed by rinsing the wafer with IPA again, and then by drying the chip. After this step, the spherical CdSe nanocrystals got linked to the self-assembled monolayer of 1,6-hexanedithiol on the gold wires.

When a nanocrystal is anchored by at least two linker molecules on either side of a gap, they end up bridging it, Fig. 6. These nanocrystals can then be characterised electrically by using the SMU.

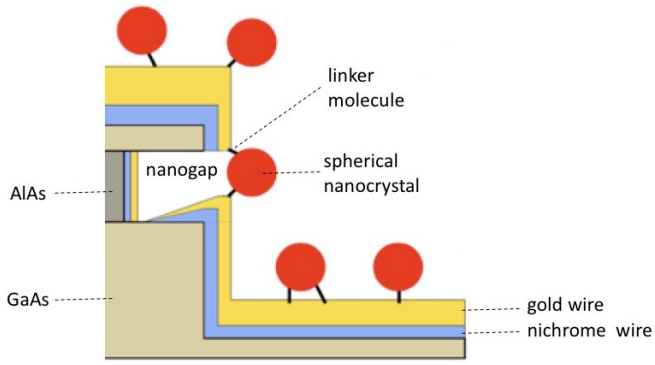

Fig. 6. The schematic representation of a nanogap that is exposed to linker molecules and spherical CdSe nanocrystals.

III. Electrical Characterisation Of CdSe Nanocrystals By Nanogap Devices

A. Electrical Characterisation Set-up

After the fabrication process, the electrical characterisation of a bonded chip was carried out. Since a nanogap is a passive device, it needs to be stimulated first and then its response to the stimulus needs to be measured. A Keithley SMU, with a pre-set current compliance of 500 nA was configured to source the voltage to the chip. If this compliance value were exceeded, then the SMU would have automatically started to act as a constant current source so that its output level would have been the pre-set current value. In this way, potential damage to the chip under test was prevented.

In order to carry out electrical characterisation, firstly, the chip was placed inside the holder of a current-voltage measurement probe so that individual electrical contacts were made to each pad of the chip. Each of these contact pads was linked to a terminal in a junction box. Each of these terminals was controlled by a double-pole-double-throw (DPDT) switch that was connected to the SMU with a coaxial cable. The DPDT switches were only used when inserting the chip into the holder of the probe, during which they were shorted to ground to prevent damage due to static electricity. In this configuration, the SMU provided the voltage input to the nanogap devices through the common lead and the current response of each nanogap was read through the associated terminal.

There is a Keithley Scanner between the SMU and the output terminals of the nanogap devices. It has relays that connect one output at a time to the input, leaving the others floating. Therefore, there is no sudden voltage change when the relay disconnects a device. One terminal was measured at a time, with all the others set to zero. The SMU voltage sweep range used was between $-2\ V$ and $2\ V$ for the forward sweep, and the same for the reverse step. A single sweep runs from $0\ V$ to $2\ V$, then back down to $-2\ V$, before returning to zero. After clamping the chip to the probe and setting above voltage sweep rate and range, the bonded chip was immersed in liquid nitrogen so that the measurements were carried out at the cryogenic temperature of 77 K in order to reduce the thermal fluctuations within the chips during electrical characterisation.

B. Current-Voltage Characteristic of CdSe

Fig. 7 shows the current-voltage (IV) characteristic of a channel of the bonded nanogap chip with CdSe nanocrystal(s), where a reproducible negative differential resistance (NDR) is observed.

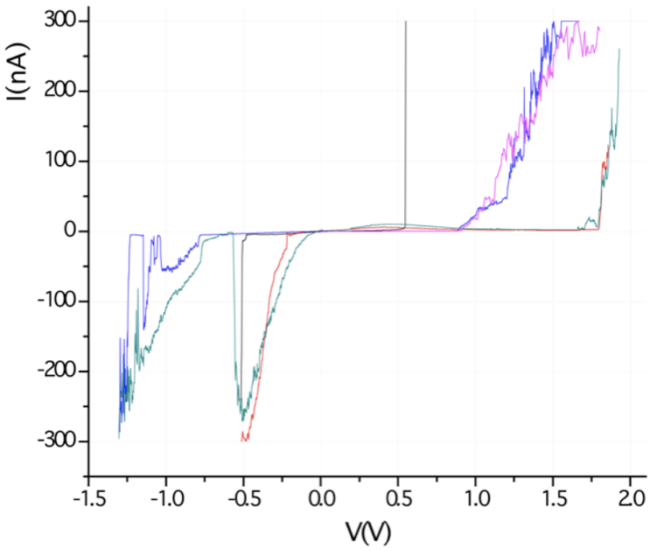

Fig. 7. The superimposed current-voltage (IV) plot from different measurements taken across the same nanogap with self-assembled 7 nm wide spherical CdSe nanocrystal(s) at 77 K, showing negative differential resistance behaviour.

NDR is well-documented behaviour for nanoscale devices [16]-[19]. It is caused by bias driven electronic structure change from one kind of insulating phase to another through a highly delocalised conducting phase [20]. In devices made of small molecules or nanocrystals that are in contact with semiconducting electrodes, when the discrete energy level of the nanodevice goes below the bottom edge of the semiconductor band of the electrode then a sharp negative differential resistance is observed. The NDR behaviour can also be observed with the metallic electrode contacts, if multiple nanocrystals are trapped between metal electrodes in series to one another. In this way, at least one of the nanocrystals acts like a semiconducting electrode to another nanocrystal.

There are several other alternative mechanisms that might be responsible for the observed NDR output. For example, a reproducible NDR could be the result of a memory effect, where the device holds on to a particular setting until a certain voltage value triggers another setting, causing reproducible loops on the IV plots. These loops could also be due to the nanocrystal being connected and disconnected from one electrode mechanically to and fro, since such a cyclic mechanical process is reproducible. However, this is not very likely, since the linker molecules anchor nanocrystals to the electrodes firmly. But more study is required to verify that the linkers keep the nanocrystals strongly attached to the electrodes throughout the entire measurement process. It can be also speculated that the sudden drop of the current after the NDR peaks might be due to the gap getting broken somewhere as a result of a high electric field inside the nanogap. However, this is not very likely either, since the current increases dramatically again during the sweep in the opposite direction. Therefore, there exists a cycle of current getting lowered and increased back and forth, which cannot be sustained once a breakage occurs inside the nanogap.

IV. Conclusion

This work shows that it is possible to reproducibly fabricate closely packed identical sub $-$ 10 nm nanogap devices that are capable of electrical characterisation of sub $-$ 10 nm molecular components. In addition, the nanogap

device design and fabrication technique discussed here have the potential to be a success in direct applications of molecular electronics. For example, in theory, a nanogap can be operated as a single electron transistor due to its favourable geometry. The AlAs layer can be doped during MBE growth phase so that it can be used as a gate.

V. Acknowledgement

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