Analog Integr Circ Sig Process (2014) 81:657–666
DOI 10.1007/s10470-014-0423-9

A 2.4-GHz low power polar transmitter for wireless body area network applications

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Received: 31 March 2014 / Revised: 30 August 2014 / Accepted: 30 September 2014 / Published online: 14 October 2014

Abstract A 2.4 GHz low power polar transmitter is proposed in this paper. A dynamic biasing circuit, controlled by a digital envelope signal, is used as a direct digital-to-RF envelope converter. It effectively linearizes the input-output characteristic of the overdriven cascode class-C power amplifier used as the output stage, by dynamically adjusting the bias voltage of the cascode transistor. An equivalent baseband model of the transmitter is presented and used to optimize system parameters and give initial assessment of the achievable performance in terms of efficiency and linearity. Based on these simulations, parameters for transistor-level implementation of the bias circuit are derived. The transmitter is designed in a 65 nm CMOS technology. The post layout simulations indicate that the transmitter successfully meets the requirements of the IEEE 802.15.6 standard for wireless body area networks. The simulated amplifier consumes 4.75 mA from a 1.2 V supply while delivering 1.45 dBm of output power with a peak efficiency of 24 %. The entire transmitter, including the PLL, consumes 7.5 mA.

Keywords WBAN · Polar amplifier · Low power · Dynamic biasing · Baseband model

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1 Introduction

The increasing use of wireless networks and the constant miniaturization of electronic devices has enabled the development of wireless body area networks (WBAN). These are highly localized wireless networks that can support a variety of medical applications, from tracking vital signs to monitoring the operation of implants. Battery life is a critical issue in BAN node design. The need for frequent replacement or recharging of batteries is undesirable for wearable nodes and unacceptable for many implantable nodes. Devices utilized in these applications have to meet the demands for low power consumption in order to allow for unobstructed use. In addition, small size and low fabrication cost are highly desirable. The new IEEE 802.15.6 standard is optimized to meet the demanding low energy needs of WBAN [1], while preserving the required quality of service. The design of an efficient transmitter, as one of the most power hungry blocks, remains an important issue in WBAN devices.

Exhaustive research has already been done in the area of power amplification [2–5]. However, most publications concerning the high efficiency amplifiers are dealing with power levels much higher than those needed in the WBAN applications, which allows more freedom in the design. In such cases the power consumed in preprocessing and driving circuits remains negligible compared to the output power. Additionally, an output combining/matching network usually occupies a large die area or requires off-chip components making it impractical for low-cost devices. Well known techniques such as outphasing or Doherty amplification are therefore not well suited to WBAN applications.

The low power transmitters reported in [6, 7] rely on a direct conversion architecture employing a class A power

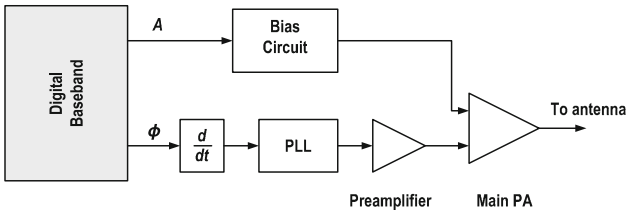

Fig. 1 Architecture of the transmitter

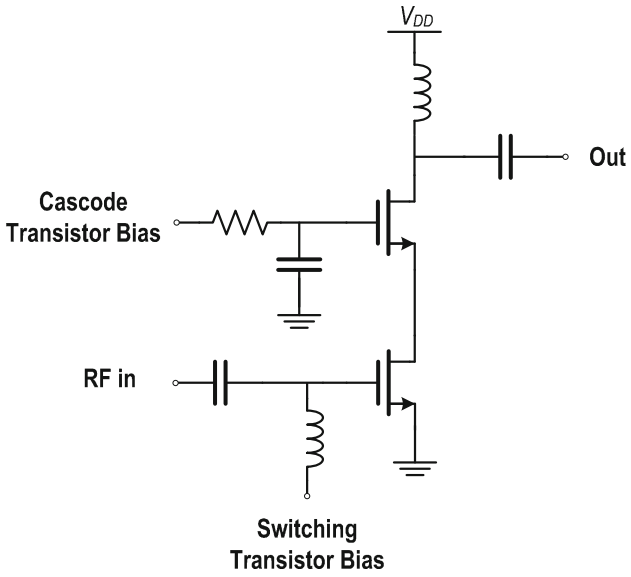

Fig. 2 Schematic of the main power amplifier

amplifier (PA). Even though the architecture is not highly efficient, its simplicity allows for only a few mA of consumption. In addition, the small area occupied by the transmitter enables the integration, hence reducing the overall cost of the system. In [8] a polar transmitter using a supply voltage modulator is presented. Although being more complex, it achieves higher efficiency compared to the traditional quadrature architectures. The downside of this approach is the fact that it requires an off-chip inductor for the output matching network. Another polar architecture has been presented in [9]. Instead of a supply voltage modulator, this transmitter uses a direct digital-to-RF envelope converter that turns on or off different number of PA sections to allow amplitude modulation. It achieves better efficiency, higher linearity at low supply voltage and well controlled envelope path delay. The transmitter presented in [10] uses injection-locking, avoiding the PLL and thus achieving faster frequency settling time and lower power consumption. Although targeting the same standard, it is designed for frequencies around 400 MHz which generally allows higher efficiency, but requires off-chip passive components. In addition, it does not support amplitude modulation, which simplifies the overall design.

This paper describes the design of a 2.4 GHz low power transmitter with emphasis on linearization techniques applied to ensure compatibility with the IEEE 802.15.6 standard. Section 2 gives an overview of the transmitter architecture. An equivalent baseband model, used to optimize system level parameters, is discussed in Sect. 3. Details of transistor level implementation are given in Sect. 4. Finally, key simulation results are given and summarized in Sects. 5 and 6.

2 Transmitter architecture

The proposed transmitter utilizes a direct-modulation polar architecture. The block diagram is presented in Fig. 1. The complex baseband signals, the in-phase and quadrature signals, are converted to envelope and phase components in digital domain. The phase signal is applied directly to the input of the frequency synthesizer, which generates a phase modulated RF signal. The latter is first amplified by the single-ended class AB preamplifier and then fed to the main PA.

The schematic of the main PA is presented in Fig. 2. It is a single ended cascode class C power amplifier driven by the full swing RF signal. The bottom transistor will therefore behave like a switch, effectively shorting the source of the cascode transistor to ground while in the conducting state. As long as the cascode transistor stays in saturation, it will behave as a current source, producing pulses whose amplitude will be determined by the gate voltage. The output power can therefore be regulated in two ways. First is to dynamically adjust the bias voltage of the switching transistor, which will effectively determine the conduction angle and the current pulse width. The second option is to dynamically adjust the bias voltage of the cascode transistor and in such manner control the amplitude of the pulses. This work focuses on the second method. A digital envelope signal will be used to regulate the gate voltage of the cascode, and subsequently modulate the amplitude of the transmitted signal. At the same time, the maximum output power level can be adjusted by setting the gate voltage of the switching transistor.

Compared to similar linearization techniques, the proposed architecture offers several advantages when it comes to low-power design. The polar amplifier described in [5] uses a supply modulator to adjust the supply voltage of the output PA. Due to high driving requirements, efficient supply modulator is hard to implement and will finally limit the overall efficiency of the transmitter. More importantly, when the output power is close to 0 dBm, such a circuit will present a significant overhead in both power and area. On

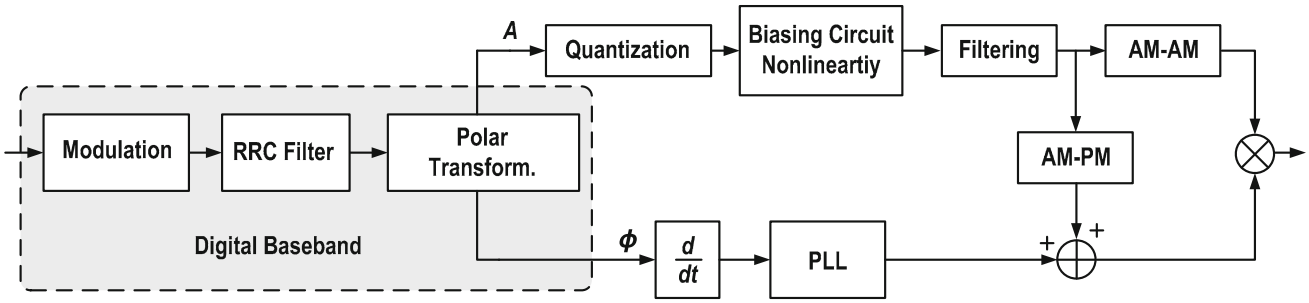

Fig. 3 Transmitter model, along with digital baseband

the other hand, the proposed design exploits a simple digital-to-analog converter (DAC), loaded by a decoupling capacitor of the cascode transistor. The only constraint comes from the bandwidth of the amplitude signal. This constraint will be the limiting factor that sets the lower boundary for the power consumption of the biasing circuit. It nevertheless remains only a minor issue compared to the supply modulator that needs to provide the entire drain current of the output stage. This allows for a simple design, occupying a small area and consuming only a small portion of the overall transmitter power.

The parameters of the dynamic biasing circuit are unknown a priori. For this reason, the characteristics of the presented PA are first extracted and used to build a high level model that is then used to determine the design constraints, as will be shown in the next section. Further details of the transistor-level design will be addressed in Sect. 4.

3 System level design and optimization

High level simulations were performed in order to determine and optimize important system parameters. Since the emphasis of this work is on the bias circuit, this section will focus mainly on the aspects that affect its implementation, namely the number of bits necessary for the amplitude path and the range of the bias voltage required to assure a proper output and maximize the efficiency.

The IEEE 802.15.6 specifications define two important constraints which are affected by the transmitter linearity. The first is the spectrum mask which defines the power spectral density levels that must not be exceeded by the transmitted signal. The purpose of this constraint is to ensure the compatibility with other devices operating in the same frequency band. The second important constraint is the error vector magnitude (EVM), defined as the deviation between the ideal and the actual transmitted constellation points. Several different modulation schemes are supported by the standard. The transmitter presented in this work supports two phase modulations, namely the $\pi/2$-DBPSK and $\pi/4$-DQPSK modulations at 600 kHz symbol rate. In all of the performed simulations, $\pi/4$-DQPSK was used as the one with the most stringent requirements.

An equivalent baseband model of the transmitter is presented in Fig 3. The mapping, pulse shaping and polar transformation are done in the digital domain. The use of square root raised cosine filter (RRC) is required by the standard, however filter parameters can be chosen arbitrarily. In this work, a roll-off factor is chosen as 0.5, and the group delay is chosen as 3 symbol durations. Before filtering, each symbol is oversampled by a factor of 8. Transformation from cartesian to polar coordinates can be done by the CORDIC algorithm.

The behaviour of the bias circuit is modeled by two blocks which take into account the quantization and the nonlinear static characteristic of the circuit. Since the nonlinearity is unknown at this point, as it is dependent on the circuit implementation, it is assumed to perfectly compensate for the nonlinearity of the output PA. The presence of the decoupling capacitor at the gate of the cascode transistor (Fig. 2) limits the bandwidth of the envelope path. A simple first order filter is placed at the output of the bias circuit to capture this effect. On the phase path, a second order linear model of the PLL is used to model the behaviour of the frequency synthesizer at baseband frequencies.

A memoryless, nonlinear model was used to represent the behaviour of the output PA. Such a model is chosen for its low computational complexity and its high level of accuracy for narrowband systems such as the one described here. The output signal amplitude and phase characteristics, as a function of cascode transistor gate voltage have been extracted from the transistor-level simulation (Fig. 4). These curves in fact correspond to the amplitude-to-amplitude (AM–AM) and amplitude-to-phase (AM–PM) conversion curves, since the envelope signal will be driving the gate of the cascode transistor.

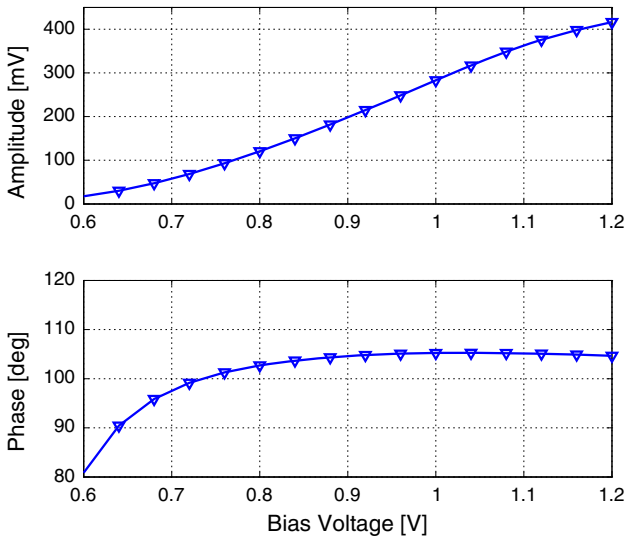

Fig. 4 Amplitude and phase characteristic as a function of bias voltage

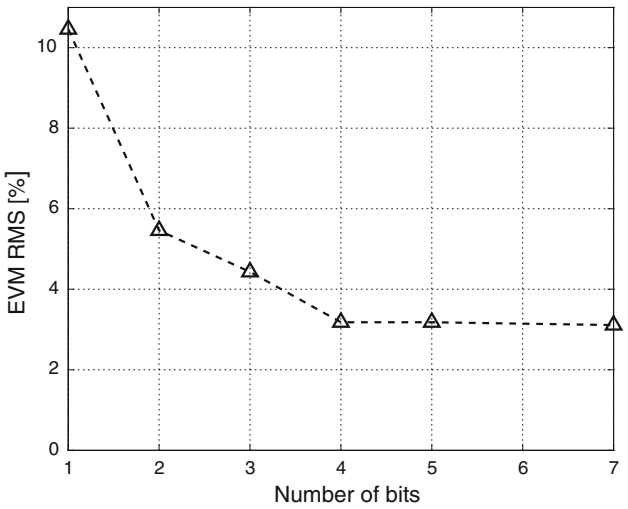

Fig. 5 Impact of envelope quantization on EVM

Since these characteristics do not vary significantly with frequency, this model can be used to describe the behaviour of the PA in the entire 2.4 GHz ISM band. Due to low peak to average power ratio (PAPR) of the transmitted signal, the bias voltage should remain in the region where the AM–PM characteristic is approximately constant. Therefore no compensation is necessary in the phase path. The AM characteristic should be compensated by the nonlinearity of the bias circuit (further explained in Sect. 4) and should hence not cause violations of the requirements defined by the standard.

An important issue concerning polar amplifiers is the fact that polar signals have larger bandwidth than the original cartesian signals. This is caused by the nonlinear mathematical relation between the envelope and phase signals and the I and Q signals. The bandwidth of the envelope path, which is determined by the bandwidth of the filter, should therefore be large enough not to cause significant spectral regrowth at the output. Another important cause of the spectral regrowth at the output is the differential delay between the two branches. It is determined by simulation that the EVM and spectrum mask remain satisfied as long as the differential delay remains smaller than 200 ns, that is, assuming the infinite bandwidth for the amplitude and phase branches. In reality, the differential delay will be caused by the different bandwidths, or equivalently different group delay between the two branches. Assuming a second order open loop transfer characteristic of the PLL, it is determined that a bandwidth of the envelope path higher than 2 MHz causes no significant spectral regrowth in the output signal, without the need for delay compensation.

3.1 Envelope quantization

Since the bias circuit is a DAC converting the input digital envelope signal to the bias voltage of the main amplifier, the number of bits is an essential parameter. Increasing the number of bits means increasing the complexity and area of the circuit. Tendency is, therefore, to reduce the number of bits as much as possible while still satisfying all the specifications imposed by the IEEE 802.15.6 standard.

The estimated impact on EVM is presented in Fig. 5. Naturally as the number of bits increases the EVM improves, to the point where it becomes dominated by other imperfections in the transmitter. It is important to notice that the defined EVM constraint of 17.78 % remains satisfied even if only one amplitude bit is used. Significant improvement can be achieved by using 4 bits, leading to the RMS value of 3.2 %. Beyond this point increasing the number of bits will not result in further improvement in terms of modulation accuracy.

The number of envelope bits will determine the quantization noise in the output signal. The level of quantization noise must be kept low enough not to cause violation of the spectrum mask. Even though it is possible to achieve this with only 2 bits, some margin should be provided to account for additional imperfections and to assure proper operation after fabrication. As can be seen from Fig. 6 just 3 bits already provide 10 dB of margin for the spectrum mask. Addition of one more bit yields slight improvement, hence 4 bits have been selected for the final implementation. Even though amplitude modulation is necessary, loose constraints imposed by the standard allow a simple implementation that should not cause significant overhead and performance degradation.

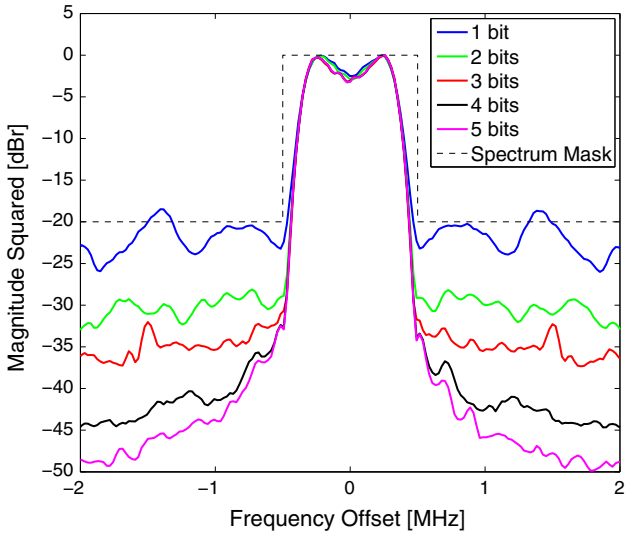

Fig. 6 Impact of envelope quantization on output spectrum

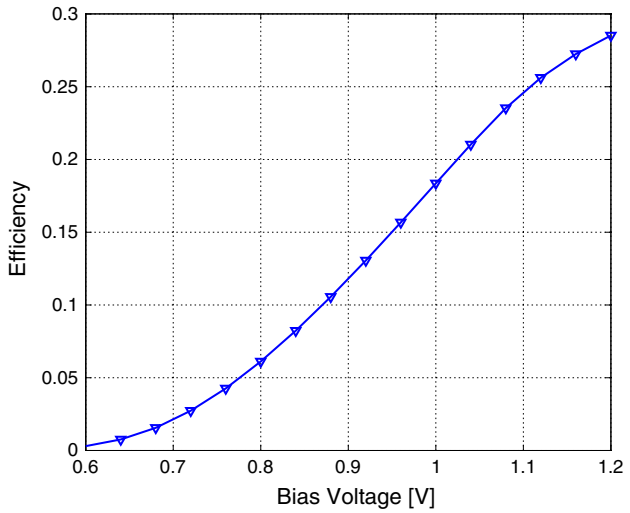

Fig. 7 Drain efficiency of the PA including power consumption of the preamplifier

3.2 Efficiency estimation

Drain efficiency of the amplifier, accounting for the consumption of the preamplifier, is calculated according to the following equation:

$$\eta = \frac{P_{OUT}}{P_{PA} + P_{PPA}}, \tag{1}$$

where P_{OUT} is the output power of the first harmonic, P_{PA} is the power consumption of the output PA and P_{PPA} is the power consumption of the preamplifier. The simulated efficiency as a function of the bias voltage is presented in Fig. 7. It is clear that the efficiency will be highest for the highest value of the bias voltage.

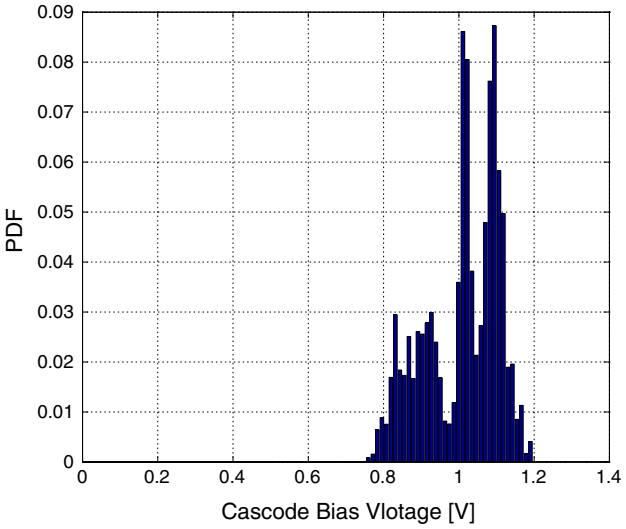

Fig. 8 Histogram of the bias voltage

Table 1 Estimated average drain efficiency

Peak bias voltage	Average efficiency
1.2 V	19 %
1.1 V	14.5 %
1.0 V	10.5 %

The average efficiency of the amplifier can be calculated using (2)

$$\eta = \int_0^{V_{MAX}} \eta(V) p(V)\, \mathrm{d}V, \tag{2}$$

where $p(V)$ is the probability density function (PDF) of the bias voltage. Depending on the implementation, the output voltage of the bias circuit will be constrained to certain boundaries. The inability to reach supply voltage will reflect in reduced average efficiency of the transmitter. Equation (2) can be used to estimate the efficiency loss. PDF of the bias voltage is approximated with a histogram obtained by simulation and used for calculation. The histogram, for the case where maximum bias voltage equals the supply voltage is presented in Fig. 8. As suggested earlier, it can also be seen that the bias voltage indeed remains in the region where the AM–PM characteristic is almost constant, justifying the assumption that no phase compensation is necessary.

Three different cases have been considered. Calculation results are reported in Table 1. As can be seen, reduction of the maximum bias voltage by 0.1 V, results in 4.5 % efficiency loss, which is considerable, especially in this case where the theoretical maximum average efficiency is 19 %. Since the maximum output voltage of the biasing

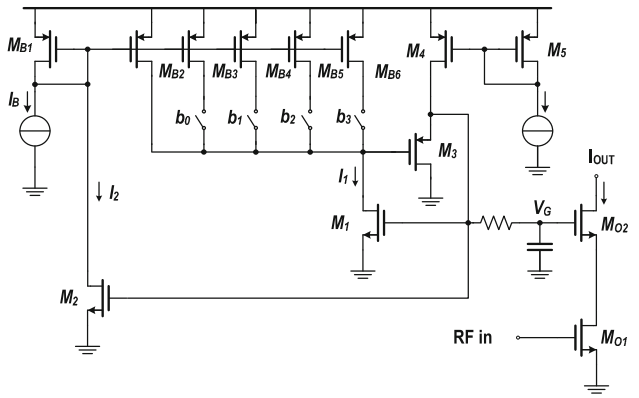

Fig. 9 Schematic of the biasing circuit

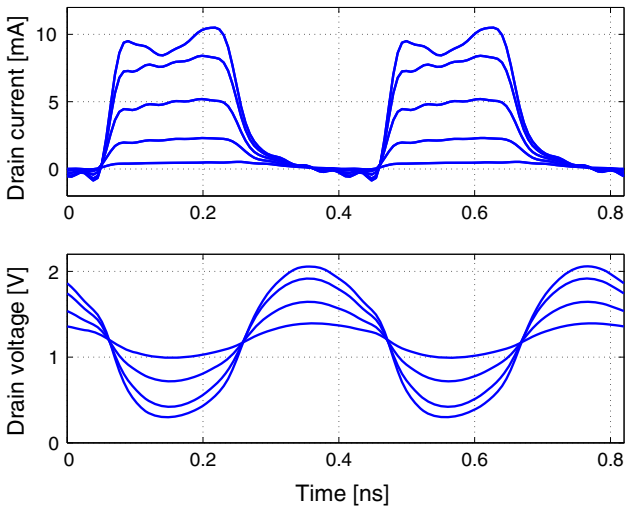

Fig. 10 Output current and voltage waveforms, for several different values of envelope

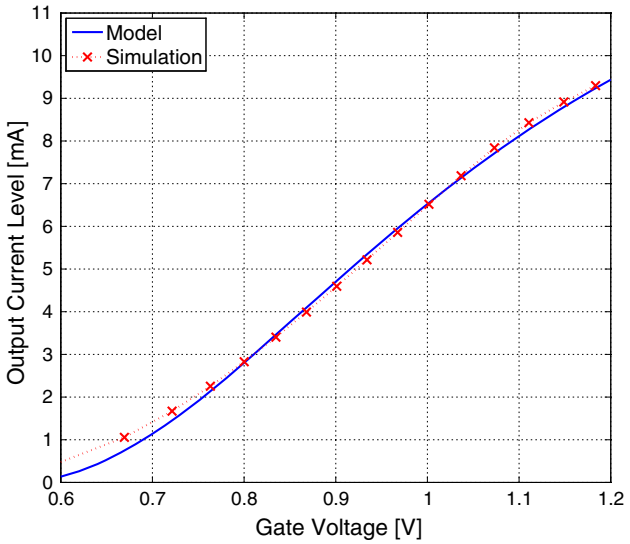

Fig. 11 Drain current level, comparison of simulation and calculation

circuit has a large influence on the overall performance of the transmitter, it must be designed such as to achieve full output swing while maintaining sufficient linearity to meet the standard requirements.

4 Implementation of the biasing circuit

The biasing circuit converts the input digital envelope signal into the bias voltage V_G of the cascode transistor. The simplified schematic is presented in Fig. 9. As stated previously 4 bits are chosen as a compromise between complexity and linearity. Transistors M_{B2}–M_{B6} operate as a binary weighted current mirror. The drain current I_1 and consequently gate voltage V_G will therefore be determined by the input codeword. The range of the bias voltage is determined by the drain current I_1 and the size of M_1.

The level shifter made of transistors M_3–M_5 serves to preserve linear relation between the input code and the current I_1 even as the bias voltage approaches the supply voltage. The drain voltage of M_1 will be lower than V_G by the gate-source voltage V_{GS3} of transistor M_3. This allows to keep transistors M_{B2}–M_{B6} in saturation across the entire range of V_G. To allow M_1 to remain in saturation, M_3 is kept in weak inversion. The decoupling capacitor at the gate of M_{O2} is charged through M_4 and discharged through M_3, therefore these two transistors must provide enough current to avoid slewing behaviour of the bias voltage. As the decoupling capacitor has to be large enough to provide steady gate voltage, this current will dominate the power consumption of the biasing circuit.

Current and voltage waveforms at the drain of the output transistor M_{O2} are presented in Fig. 10. The drain current can be roughly approximated by a square wave, whose amplitude is determined by the static characteristic of M_{O2}. While the switching transistor M_{O1} is closed, transistor pair M_1–M_{O2} should behave like a current mirror. It is therefore expected that the level of output current I_{OUT} changes linearly with current I_1, however, this is not the case. Two main causes of this nonlinearity can be identified. First is the large voltage swing at the drain of transistor M_{O2} which affects the output current, making it lower than anticipated. The second cause is the large ratio of sizes between M_1 and M_{O2}. Short channel effects will be more pronounced in M_{O2}, as it is a minimum channel device, finally resulting in discrepancies of static characteristics of the two transistors. The resulting nonlinearity of the *input code - output amplitude* is presented in Fig. 12.

Linearization of the input-output characteristic can be achieved by addition of transistor M_2. To explain the principle, the static characteristic of transistor M_{O2} will be

approximated by the following equation, used for long channel devices:

$$I_{OUT} = \frac{\beta_{O2}}{2n}(V_G - V_{T0})^2(1 + \lambda(V_{DD} - R_{EQ}I_{OUT})). \quad (3)$$

Parameters λ and R_{EQ} model the influence of the drain voltage on output current and are used here as curve fitting parameters. A comparison between the model and steady state simulation are presented in Fig. 11.

Since M_1 is a long channel device, and its drain voltage does not vary significantly, drain current I_1 can be calculated as

$$I_1 = \frac{\beta_1}{2n}(V_G - V_{T0})^2. \quad (4)$$

Combining (3) and (4) results in

$$\frac{I_{OUT}}{1 + \lambda(V_{DD} - R_{EQ}I_{OUT})} = \frac{\beta_{O2}}{\beta_1} I_1 \quad (5)$$

which clearly shows that the output current does not vary linearly with current I_1. To compensate for the existing nonlinearity, local feedback was introduced. The relation between the drain current and the input codeword $I_1 = NI_B$ changes, with the addition of the feedback transistor M_2, to become

$$I_1 = \frac{I_B N}{1 - MN}, \quad (6)$$

where M is the ratio between transistors M_2 and M_1. Plugging (6) into (4), together with (3) yields

$$\frac{I_{OUT}}{1 + \lambda(V_{DD} - R_{EQ}I_{OUT})} = \frac{\beta_{O2}}{\beta_1}\frac{I_B N}{1 - MN}. \quad (7)$$

Solving for I_{OUT} gives

$$I_{OUT} = \frac{\beta_{O2}}{\beta_1}(1 + \lambda V_{DD}) I_B N \frac{1}{1 - MN + \frac{\beta_{O2}}{\beta_1} I_B \lambda R_{EQ} N}. \quad (8)$$

The ratio M can now be set to

$$M = \lambda R_{EQ}\frac{\beta_{O2}}{\beta_1} I_B, \quad (9)$$

which results in a linear input-output characteristic $I_{OUT}(N)$

$$I_{OUT} = \frac{\beta_{O2}}{\beta_1}(1 + \lambda V_{DD}) I_B N. \quad (10)$$

The transistor-level simulation of the linearized characteristic is presented in Fig. 12. Although significantly improved compared to the original characteristic, it will not be completely linear due to several approximations introduced in the above calculation.

The power spectral density (PSD) of the transmitted signal for the two cases is presented in Fig. 13. Again, linearized characteristic provides considerable improvement, and more than 15 dB of margin for the output spectrum mask. Compared to digital predistortion, the presented linearization technique offers similar performance with the addition of just one transistor, and a lower increase in complexity and area.

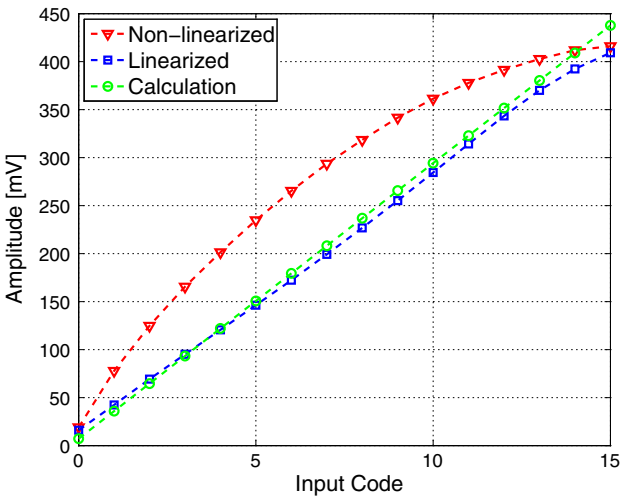

Fig. 12 Comparison of linearized and non linearized static characteristic

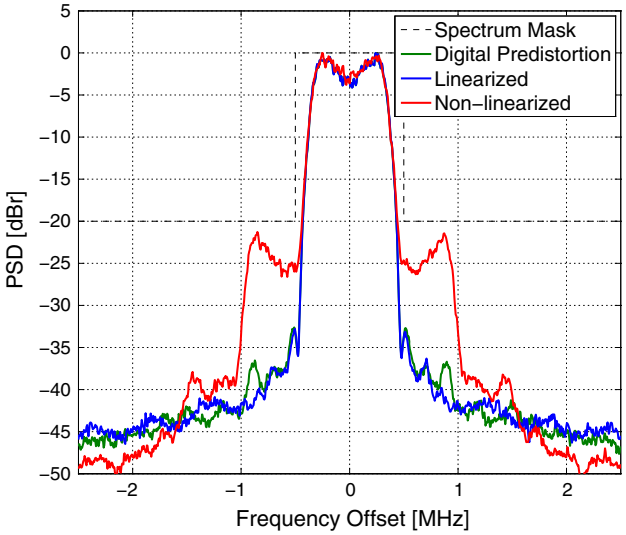

Fig. 13 Transmitted signal spectrum for different cases

5 Simulation results

The output power is depicted in Fig. 14. According to the post layout simulation, the peak output power is equal to 1.45 dBm while drawing 4.75 mA from the 1.2 V supply.

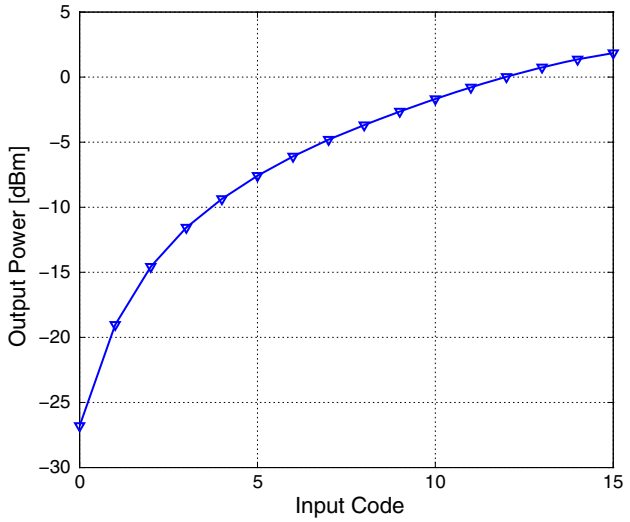

Fig. 14 Output power as a function of input code

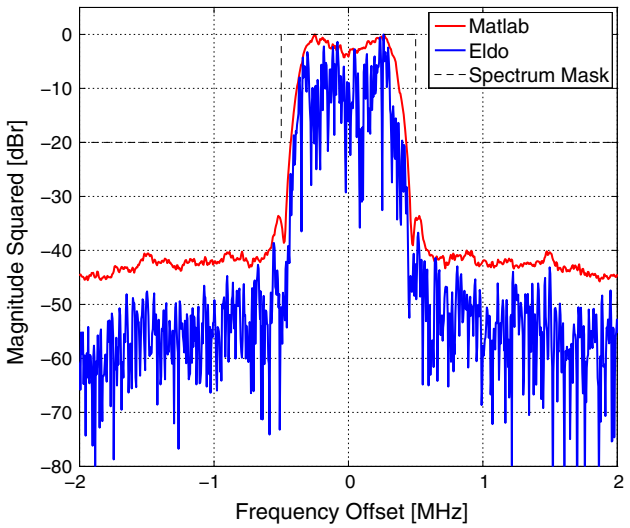

Fig. 16 Output Spectrum comparison between MATLAB model and transistor level simulation

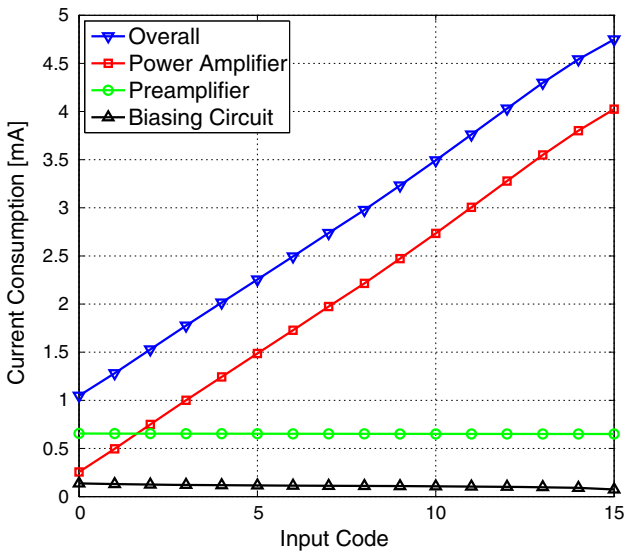

Fig. 15 Transmitter power consumption, per block and overall

The dynamic range of the proposed transmitter is 28 dB, however phase predistortion may be needed to compensate for the AM–PM nonlinearity in order to use the entire dynamic range.

The simulated current consumption, for each block and for the entire transmitter is presented in Fig. 15, as a function of the input codeword. As can be seen, the preamplifier draws a constant current regardless of the transmitted signal amplitude. For high output power, the current consumption will be dominated by the main PA, whereas for lower output power, the power consumption of the main PA becomes comparable to that of the preamplifier. The bias circuit consumes only a small portion of the overall power. A peak efficiency of the whole amplifier reaches 24 %. Accounting for the consumption of the frequency synthesizer, the overall current consumption adds up to 7.5 mA. Finally, the efficiency of the entire transmitter (excluding the digital baseband) becomes 16 %.

The spectrum resulting from system level simulations is compared to the spectrum resulting from post layout simulations in Fig. 16. The PSD obtained from system level simulations is obtained by averaging a long input sequence. The fact that the spectrum obtained from transistor level simulation stays below this level justifies the use of the presented model for the assessment of the transmitter performance. The layout of the presented transmitter is shown in Fig. 17.

Presented work is compared to the current state of the art low power transmitters in Table 2. Drain efficiency only accounts for the PA (and possibly driver) power consumption disregarding the consumption coming from preceding stages. Note that post layout simulation results are compared to measurement results here, however it is expected that these numbers do not vary significantly after fabrication.

6 Conclusion

The principle and the design of a 2.4-GHz low power polar transmitter integrated in a 65 nm CMOS technology are presented. The class C output PA is linearized through the use of a dynamic biasing circuit, which converts the digital

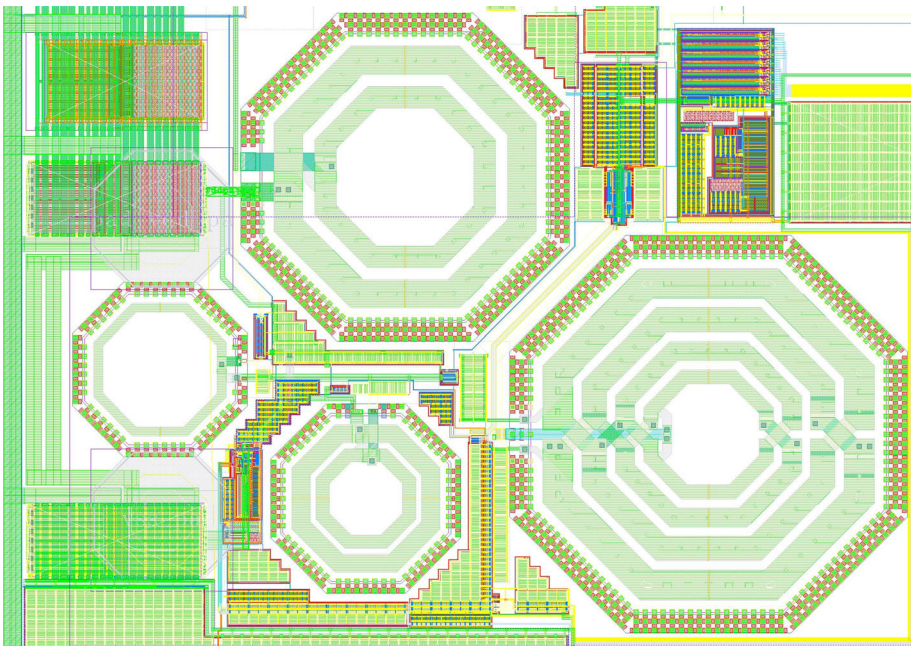

Fig. 17 PA layout

Table 2 Comparison with current state of the art

Ref.	P_{OUT} (dBm)	I_{DC} (mA)	V_{DD} (V)	DE (%)	Tech.
[6]	0	6.4	2.5	13.3	0.25 μm
[7]	0	6.0	1.8	11.1	0.18 μm
[8]	3	8.2	1.5	20.3	0.13 μm
[9]	-10	3.83	1.2	3.4	90 nm
[10]	-8	2.45	0.9	-	65 nm
Our work	1.45	7.5	1.2	24	65 nm

envelope signal into a bias voltage. The characteristics of the described circuit were further improved by introducing a local feedback to compensate for non ideal effects. An implementation utilizing 4 bits is described, but the resolution could easily be extended, using the same principle, to allow for the transmission of signals employing higher order modulation schemes, defined by other standards. The total simulated current consumption of the transmitter is as low as 7.5 mA from a 1.2 V supply, while delivering 1.45 dBm of the output power, with an amplifier peak efficiency of 24 %.

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