Integrated differential high-voltage transmitting circuit for CMUTs

Llimos Muntal, Pere; Larsen, Dennis Øland; Farch, Kjartan; Jørgensen, Ivan Harald Holger; Bruun, Erik

Published in:
Proceedings of 13th Ieee International New Circuits and Systems Conference

Link to article, DOI:
10.1109/newcas.2015.7182038

Publication date:
2015

Document Version
Peer reviewed version

Integrated Differential High-Voltage Transmitting Circuit for CMUTs

Pere Llimós Muntal*, Dennis Øland Larsen*, Kjartan Færch†, Ivan H.H. Jørgensen* and Erik Bruun*
* Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby, Denmark
† Analogic Ultrasound, BK Medical Design Center, Herlev, Denmark
plmu@elektro.dtu.dk, deno@elektro.dtu.dk, kjf@bkmed.dk, ihhj@elektro.dtu.dk, eb@elektro.dtu.dk

***Abstract*—In this paper an integrated differential high-voltage transmitting circuit for capacitive micromachined ultrasonic transducers (CMUTs) used in portable ultrasound scanners is designed and implemented in a 0.35 µm high-voltage process. Measurements are performed on the integrated circuit in order to assess its performance. The circuit generates pulses at differential voltage levels of 60 V, 80 V and 100 V, a frequency up to 5 MHz and a measured driving strength of 1.75 V/ns with the CMUT connected. The total on-chip area occupied by the transmitting circuit is 0.18 mm^2 and the power consumption at the scanner operation conditions is 0.754 mW without the transducer load and 0.936 mW with it.**

I. Introduction

Ultrasound scanners are widely used in medical applications since it is a very effective and fast diagnostic technique. The traditional static ultrasound scanners are large devices which are plugged into the grid. Therefore they have no power consumption limitation, hence the design tendency is to keep increasing their complexity to obtain better picture quality. In the last decade, high integration has enabled portable ultrasonic scanners to have comparable performance to the traditional static ultrasound scanners. However, portable scanners have power consumption, heat dissipation and area limitations. Consequently, the main target of the design of a portable ultrasound scanner is to utilize the power consumption budget and area available in the most effective way in order to achieve the best picture quality possible.

Ultrasonic scanners consist of hundreds of channels and each of them has a transducer, a transmitting circuit (Tx) and a receiving circuit (Rx). The Tx provides the high-voltage pulses that the transducer needs to generate ultrasonic waves and the Rx detects the low voltage signal induced in the transducer and it amplifies and digitizes it. The ultrasound transducers used in this paper are capacitive micromachined ultrasonic transducers (CMUTs), [1], which are composed of a thin movable plate suspended on a small vacuum gap on top of a substrate. The transducer has two terminals, one connected to the substrate and the other connected to the movable plate. By applying a voltage difference between the two terminals of the CMUT, the thin plate deflects due to an electrostatic force. The ultrasound is generated when applying high-voltage pulses in one of the terminals of the CMUT which makes the thin plate vibrate.

This paper deals with the design and implementation of an integrated differential high-voltage transmitting circuit for CMUTs, and it is an improved version of the work presented in [2].

II. Transmitting circuit specifications

The transmitting circuit needs to drive a particular CMUT, therefore its specifications come from the inherent transducer characteristics. The CMUT has been designed and modeled at DTU Nanotech, and even though the driving requirements are described here, the electrical equivalent model of the CMUT is confidential, therefore it is not presented in this paper. The CMUT, which is mainly a capacitive load, has an equivalent capacitance of 30 pF and has a resonant frequency of $f_t = 5\,\mathrm{MHz}$. In receiving mode, the transducer needs a bias voltage of 80 V and during transmission, the CMUT requires high-voltage pulses from 60 V to 100 V toggling at its resonant frequency and a driving strength corresponding to a slew rate (SR) of 2 V/ns. Ultrasound scanners transmit for a short period of time, 400 ns, and receive for a much longer period of time, 106.4 µs, hence the operation transmitting duty cycle is $1/266$ in this particular application.

III. Design and implementation of the Tx

The transmitting circuit designed in this paper consists of new and improved subcircuits structured in the same way as in [2], which is shown in Fig. 1. The Tx consists of a three-level high-voltage output stage that drives the ultrasonic transducer, which is controlled with high-voltage signals provided by the level shifters. The low-voltage signals needed for the level shifters operation are generated by the control logic block. A smaller differential output stage topology with superior performance is used together with an improved version of the level shifters which consume much less current and occupy less area. A more advanced control logic block is also used which internally synchronizes the input signals and compensates for the delay of the level shifters in order to avoid possible shoot through in the output stage by accidentally turning on several MOS devices at the same time. All the reconfigurability features presented in [2] are also removed in order to improve the power consumption and diminish the area of the transmitting circuit, hence the Tx is designed to drive the specific CMUT

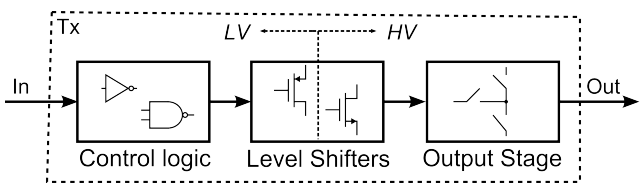

Fig. 1. Transmitting circuit block structure.

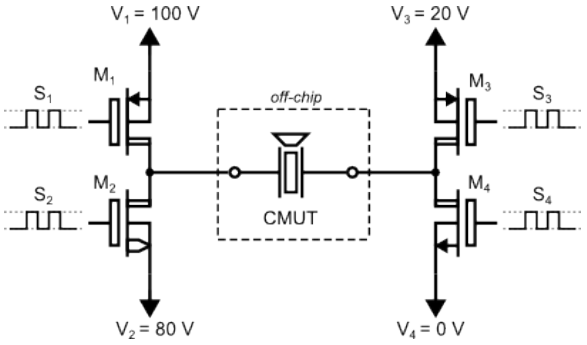

Fig. 2. Schematic of the differential output stage. Note that M_2 is an isolated NMOS located its own well.

that was described in Section II. In the next subsections the design of each block of the improved Tx circuit is presented.

A. Differential output stage

CMUTs are non-polarized devices, therefore they can be single-ended driven by pulsing one of the plates and biasing the other or differential driven by pulsing both terminals, which is the approach used in this design. The most commonly used single-ended approach [3] used also in the previous output stage [2] had some drawbacks. Firstly, two transistors were required to connect the output node to the middle voltage, an NMOS to pull down from high-voltage and a PMOS to pull up from low voltage. Secondly, two extra diode-coupled MOS devices were needed in order to avoid short circuiting voltage supplies through the body diode of the MOS transistors connected to the middle voltage. These diode-coupled MOS devices also added a small voltage drop that caused a small offset from the middle voltage level in the output node.

In order to solve the aforementioned problems and improve the area and power consumption of this block a new differential output stage topology was designed and its schematic can be seen in Fig. 2. It consists of two two-level output stages, each of them connected to one of the terminals of the transducer, that can generate three differential levels. There are several advantages of this topology. Firstly, the number of transistors used is only four, instead of the six used in the single-ended version, which translates into less area and also less parasitic capacitance. The two diode-coupled MOS devices are not used anymore so there is no voltage offset from the voltage supplies to the output node connected to the CMUT. Secondly, since CMUTs are mainly capacitive loads, the two sides of the output stage are DC voltage isolated, therefore the voltage swing that each side needs to handle is only a drain-source voltage of 20 V instead of the single-ended version where some of the MOS devices of the output stage needed to handle the full pulse swing. Since the voltage requirements are lower, the MOS devices can also be smaller and with less parasitic capacitance which improves the area and power consumption. Thirdly, since the CMUT is driven differentially, the slew rate required in each side of the output stage is reduced to 1 V/ns, which is half of the slew rate specified in Section II. The slew rate required is related to the size of the MOS devices, hence reducing the SR requirements will allow for smaller device parameters. This topology also presents potential advantages such as four level pulsing achieved by using non-symmetrical voltages. Increasing the number of voltage levels can be beneficial for the power consumption, as shown in [3]. There is one consideration to be made regarding the differential topology, which is the need of an extra pad in the integrated circuit since it needs to be connected to the two terminals of the CMUT instead of one. In principle, this would require a full extra high-voltage ESD protected pad, which occupies approximately $0.11\,\text{mm}^2$. However, the output stage transistors are significantly large, hence their inherent ESD protection was tested and proved to be enough in order to protect the integrated circuit. Only a small pad opening of $0.025\,\text{mm}^2$ placed on the top of the output stage is required to connect the transducer to the integrated circuit occupying no additional area.

The MOS devices M_1, M_2, M_3 and M_4 are sized in order to achieve the SR of 1 V/ns in each side of the differential output stage for all the different voltage transitions. The SR was measured with the CMUT connected since its impedance affects the performance of the output stage. Another consideration during the sizing of the output stage transistors is the maximum peak current. It needs to be guaranteed that each MOS device can handle the maximum peak current without being destroyed.

B. Improved pulse-triggered level shifters

The output stage contains four MOS devices, M_1, M_2, M_3 and M_4 and they are driven with different voltage levels V_{HI}: 100 V, 80 V, 20 V and 5 V. Each MOS device requires a level shifter which needs to be optimized and designed for that specific voltage. A low-power pulse-triggered topology is used for the three high-voltage level shifters and a conventional cross coupled low-voltage topology is used for the 5 V level shifter since its power consumption and area are negligible (not shown here due to its simplicity).

The previous pulse-triggered level shifters that were used in [2], even though they were functional, presented some problems such as large area due to the high gate-source voltage range, unregulated current pulse magnitude that changes the state of the latch and latch start-up state issues when ramping the high-voltage domain of the level shifter. In order to overcome some of these problems a new improved version of the pulse-triggered level shifter presented in [4] is used in this transmitting circuit and its schematic is shown in Fig. 3. The first change from the previous level shifters is a reduced gate-source voltage swing from 12.5 V to 5 V that allows for the usage of MOS devices with thinner gate oxide which are smaller and have less parasitic capacitances. Consequently $V_{LO} = V_{HI} - 5\,\text{V}$. Furthermore, using these devices, now the floating current mirror and the latch can be collected in a single deep N-well reducing significantly the area of the design. The second change is the addition of a current mirror formed by M_{1a}, M_{1b}, M_{1c} and M_{1d} that controls the magnitude of the current pulse that changes the state of the latch. This allows for a smaller magnitude of the current pulse as it can be controlled from a bias generator with reduced process, voltage and temperature dependence, hence there is no need to over-design it for the worst case process corner. The last change in the level shifters is the addition of common mode clamping transistors M_7 and M_8 to reduce the common mode current transferred to the latch when the high-voltage domain of the

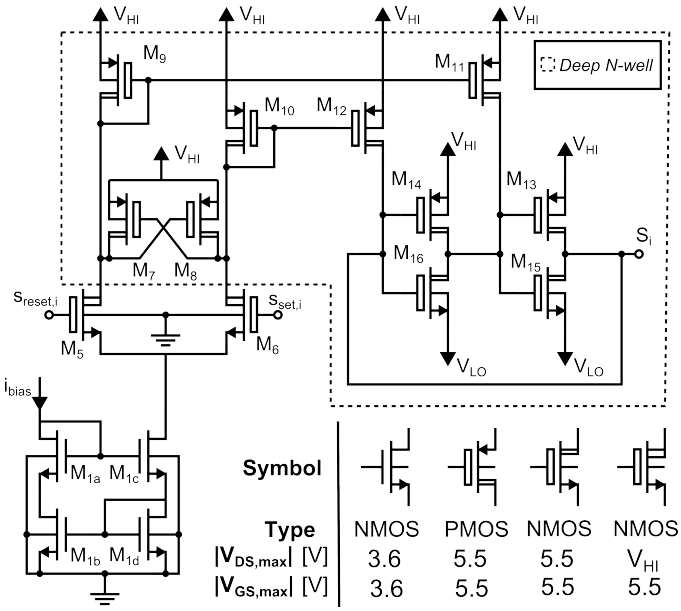

Fig. 3. Schematic of the improved level shifters.

level shifter is ramping [5]. Using these two extra MOS devices the design is more robust to high-voltage ramping. It is worth to mention that since each level shifter is designed for a different voltage level, the delay from the input to the output of each of them is different. Consequently the delays needs to be compensated in the low-voltage control logic block, to avoid shoot through in the output stage.

C. Low-voltage control logic

The low-voltage control logic consist of three parts which are shown in Fig. 4: Synchronization, delay compensation and pulser. Firstly, the input signals, s_i, are synchronized to avoid any effect of external routing and also ensure 50% pulsing duty cycle even if the input signals s_i are not exact. The synchronization is performed on-chip using standard cell flip-flops clocked at double frequency of the pulses, $f_{clk} = 2f_t = 10\,\text{MHz}$. Secondly, the synchronized signals $s_i{}'$ are separately delayed in order to compensate for the different delays of the level shifters and also a common delay is added as dead time to avoid shoot through in the output stage by having two MOS devices on at the same time. The delays are implemented with standard cell minimum size inverters for area reduction and power consumption purposes. Finally, the synchronized and delay-compensated signals, $s_i{}''$, are converted into pairs of set/reset signals, $s_{set,i}$ and $s_{reset,i}$, to properly drive the pulse triggered level shifters. The pulsing circuit used is the same mentioned in [2].

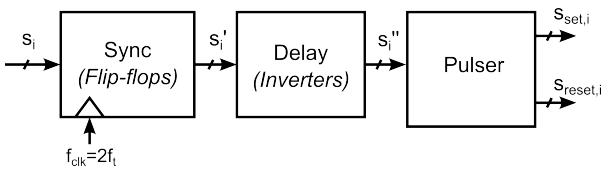

Fig. 4. Block structure of the low voltage control logic.

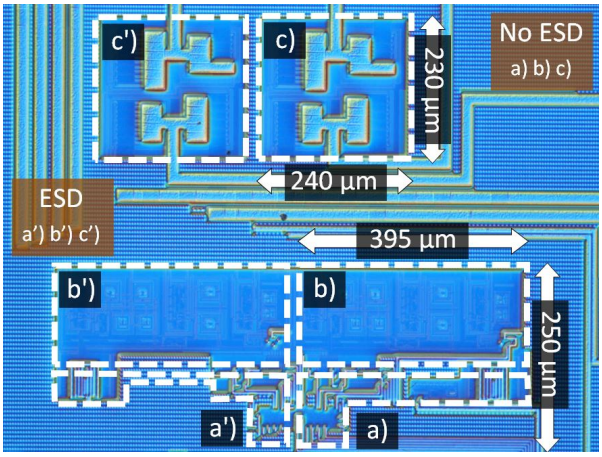

Fig. 5. Picture of the taped-out differential transmitting circuit.

IV. Measurement Results

After the design, the transmitting circuit was taped out and fabricated in a 0.35 µm high-voltage process, and a picture of the integrated circuit die taken with a microscope can be seen in Fig. 5. Two full transmitting circuits were included in the die, one with ESD protected pads and a second one with just pad openings, in order to assess the inherent ESD protection of the output stage. The inherent ESD protection proved to be sufficient, therefore the measurements were performed with the transmitting circuit without ESD protected pads. The low-voltage control logic is located in area a) with an area of $0.01\,\mu\text{m}^2$, the level shifters are situated in area b) with an area of $0.059\,\text{mm}^2$ and the differential output stage is located in c) and occupies an area of $0.055\,\text{mm}^2$. The total area of the transmitting circuit accounting also for the routing is $0.18\,\text{mm}^2$.

In order to assess the performance of the transmitting circuit a PCB was built to test it. The measurement setup used is shown in Fig. 6. Two Hewlett Packard E3612A voltage supplies were used to generate 20 V and 100 V, and from those voltages the on-board linear regulators generate the rest of the voltage levels used in the integrated circuit, 5 V, 15 V, 80 V, 85 V and 95 V. During the current measurements, only the current from each voltage level fed into the chip was accounted, hence the current sunk by the linear regulators was not considered. The low-voltage input signals and the low-voltage supply were generated using an external Xilinx Spartan-6 LX45 FPGA with a maximum clock frequency of 80 MHz and 3.3 V operation. The voltage outputs of the Tx connected to the CMUT and the current consumption were measured using a Tektronix MSO4104B oscilloscope and a Tektronix TCP202 current probe.

Using the described setup, the integrated circuit was tested with pulses from 60 V to 100 V, frequency of 5 MHz, a receiving bias voltage of 80 V and ultrasound scanner transmitting duty cycle of $1/266$. The measured voltage of the two terminals of the CMUT and the differential voltage between the plates of the CMUT can be seen in Fig. 7. The bias voltage is stable around 80 V when receiving and it toggles according to the input signals supplied between 60 V and 100 V at a measured frequency of 4.995 MHz when transmitting.

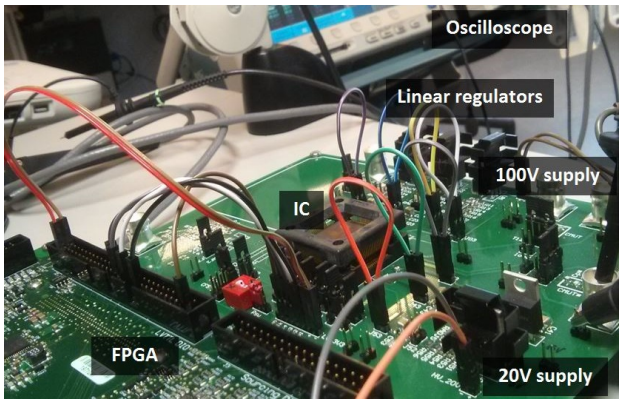

Fig. 6. Setup for the integrated circuit measurements.

The minimum slew rate measured in the high-voltage terminal of the Tx is 0.92 V/ns and the slew rate measured in the low-voltage terminal is 0.83 V/ns, which are a bit below the specified 1 V/ns. This slightly reduced slew rate is attributed to the parasitic capacitance of external routing and the probe capacitance used to measure. In order to measure the power consumption, the currents from all the voltage levels supplying the integrated circuit were measured both for the unloaded Tx and also for the Tx with the equivalent electric model of the CMUT connected. The measurements are shown in Table I. The currents measured from the 5 V, 15 V, 85 V and 95 V supplies were negligible compared to the ones measured in the other voltage supplies, so they are accounted as zero and are not shown in the table. Using these current measurements, the power consumption can be calculated obtaining 0.754 mW for the unloaded Tx and 0.936 mW once loaded.

V. Discussion

The design presented can not be compared directly with state of the art transmitting circuit since the references found either do not specify the driving conditions, area and power consumption or only the full channel consumption, including the receiving circuitry, is stated [6], [7]. A comparison with the previous Tx presented in [2] is performed. However, the operation conditions on the previous Tx were different: The pulse voltage swing was 50 V and the duty cycle was 50%. In order to compare the topologies, the same operating conditions should be defined. The conditions chosen are the ones closest to the operation of an ultrasound scanner such as the ones defined in this paper: pulse voltage range of 40 V, pulsing frequency of 5 MHz, and a transmitting duty cycle of 1/266. Adjusting the power consumption in the previous Tx to the operation conditions of an ultrasound scanner, a comparison can be performed and a summary is shown in Table II. The power consumption corresponds to the non-loaded transmitting circuits, and a probe with the same 15 pF capacitance was used in both cases. The improved differential Tx presented in this paper achieves a very significant area reduction of 80.8% and the power consumption is reduced 58.2%.

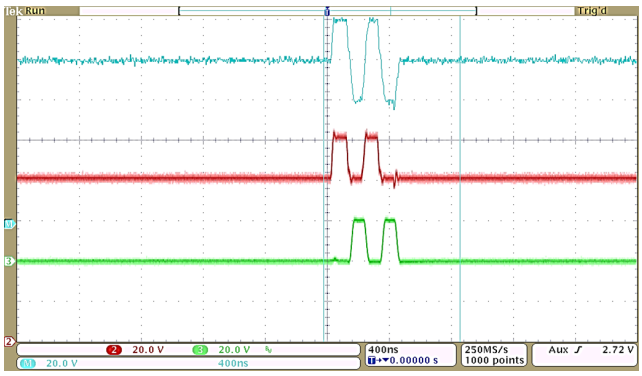

Fig. 7. Measurements of the output terminals of the differential transmitting circuit. The red trace and green trace are the voltage measured at the high-voltage and low-voltage terminals of the Tx respectively. The cyan trace is the differential voltage between them.

TABLE I. Current measurements on the IC

V_{supply} [V]	100	80	20
$I_{no\text{-}load}$ [µA]	14.3	-12.2	15.0
I_{load} [µA]	30.6	-34.9	33.4

TABLE II. Transmitting circuit performance comparison

	[2]	this work	%
On-chip area [mm^2]	0.938	0.18	-80.8
Power no-load [mW]	1.8	0.754	-58.2

VI. Conclusions

In this paper a differential integrated high-voltage transmitting circuit for CMUTs is designed and implemented in a high-voltage 0.35 µm process. The circuit supplies pulses with a frequency of 5 MHz, voltage levels of 60 V, 80 V and 100 V and a measured slew rate of 1.75 V/ns. The transmitting circuit is measured under the operation conditions of an ultrasound scanner in order to accurately assess the performance of the circuitry. The non-loaded total power consumption measured on the integrated circuit is 0.754 mW and the circuit occupies an on-chip area of 0.18 mm^2, which represent an improvement of 58.2% and 80.8% respectively from the previous design.

References

[1] Butrus T. Khuri-Yakub and Ömer Oralkan, "Capacitive micromachined ultrasonic transducers for medical imaging and therapy" in *Journal of Micromechanics and Microengineering*, Vol. 21, pp.1-11 (2011)

[2] P. Llimós Muntal, D. Ø. Larsen, I. H.H. Jørgensen and E. Bruun, "Integrated Reconfigurable High-Voltage Transmitting Circuit for CMUTs" in *32nd Norchip Conference* (2014)

[3] K. Chen, H-S. Lee, A.P. Chandrakasan and C.G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver" in *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 11, pp.2734-2745 (2013)

[4] D. Ø. Larsen, P. Llimós Muntal, I. H.H. Jørgensen and E. Bruun, "High-voltage Pulse-triggered SR Latch Level-Shifter Design Considerations" in *32nd Norchip Conference* (2014)

[5] H. Ma, R. van der Zee, and B. Nauta, "Design and Analysis of a High-Efficiency High-Voltage Class-D Power Output Stage" in *Solid-State Circuits, IEEE Journal of*, vol.49, no.7, pp.1514-1524 (2014)

[6] I.O. Wygant, X. Zhuang, D.T. Yeh, . Oralkan, A.S. Ergun, M. Karaman and B.T. Khuri-Yakub, "Integration of 2D CMUT Arrays with Front-End Electronics for Volumetric Ultrasound Imaging" in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 55, No. 2, pp.327-342 (2008)

[7] G. Gurun, P. Hasler and F.L. Degertekin, "A 1.5-mm Diameter Single-Chip CMOS Front-End System with Transmit-Receive Capability for CMUT on-CMOS Forward-Looking IVUS" in *IEEE International Ultrasonics Symposium Proceedings*, pp.478-481 (2011)