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Design of Fully Integrated Resonance Switched Capacitor Converters in FDSOI Technology

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***Abstract*—The integration of power supplies has the potential to reduce the form factor and cost of electronic systems. The resonance switched capacitor (ReSC) converters show a promising performance as it overcomes the charge-sharing losses in switched capacitor (SC) converters. However, the used inductors need an additional manufacture process. This paper investigates the design of ReSC using an integrated air-core inductors in 28 nm FDSOI technology. Different interleaved topologies are discussed using inductance around 1 nH. The flying and bypass capacitors are implemented using MOM capacitors on-chip. With an inductor quality factor around 6-8 and 1 mm^2 silicon, the ReSC converter shows 30 % lower losses with respect to the SC converter at power density of 0.1 W/mm^2. Although the integrated inductor has a relatively poor quality factor, the fully integrated ReSC converters improve the efficiency of the SC converters. It can be seamlessly implemented in the pre-existing technologies.**

I. Introduction

The monolithic integration of power supplies is increasingly attractive to reduce the number of discrete components and the pin count of system on chip (SoC). Switched capacitor (SC) converters have been considered the best candidate for the fully integrated power supplies along with technology scaling that allows the miniaturization of the capacitances with higher density [1], [2]. However, SC converters suffer from charge-sharing losses and its switching frequency is considerably high to lower the output resistance.

The resonant switched capacitor (ReSC) converters are recently studied in power on-chip context [3], [4]. They employ the same topology of the SC converter but adding an inductor in the charging and discharging paths to create an adiabatic energy transfer which improves the efficiency and increases the power-density. The resonance operation allows, on one hand, the reduction of conduction losses by adopting the zero current switching. On the other hand, it reduces the switching losses by working at significantly lower frequencies with respect to SC converters with the same area while having the same output resistance. In the prior state-of-the-art [5], [6], the ReSC converters are only implemented with discrete inductors usually bumped on top of the die. Since the performance of ReSC is strongly dependent on the inductance quality factor (Q), the usage of the discrete inductor with quality factor about 10-20 would be an optimal solution. However, the extra manufacturing step of mounting the inductor could be a burdensome and expensive process for mass production which limits the interests in these type of converters *in fully integrated context*.

This paper investigates the design of a fully integrated ReSC converter in 28 nm FDSOI technology to quantify the achievable performance. Different architectures of ReSC converters are considered, for example, single phase, multiphase with multiple inductors, and multiphase with single inductor. For each architecture, we estimate its output resistance, the feasibility for fully integration and the immunity to the parasitic access inductance.

The paper is organized as follows, Section II discusses the implementation of the integrated inductor. Section III explains the FDSOI technology for implementing power converters. Different topologies of the resonance switched capacitor converters are elaborated in Section IV. Transistor-level simulation results are reported in Section V.

II. Integrated inductor design

The output resistance of the ReSC converter is directly proportional to the total resistance of the charging or discharging paths [7]. Hence, it is desirable to minimize the inductor resistance, and consequently increase its quality factor, to reach high power densities. To reduce the area overhead, the last two metal layers are used to implement the inductor. We assume that the inductor is a planar square with only one turn to minimize the series resistance. From the modified Wheeler formula [8], the inductance and the resistance of the planar square inductor can be expressed as follows:

$$L = K_1.\sqrt{\varepsilon} \quad , \quad R_{ind,dc} = K_2 \tag{1}$$

where K_1 and K_2 are constants depending on the geometrical aspects of the inductor and the used metal sheet resistance and ε is an area scaling factor. For example, assume we have an iductance L has an area A. If the area is scaled with half ($\varepsilon = 1/2$), then the inductance becomes $L/\sqrt{2}$. However, the resistance of the inductor is independent of the geometrical scaling. Hence, the quality factor can be expressed as

$$Q = K_3.\varepsilon^{1/4} \tag{2}$$

where K_3 is a constant depending on the inductance value, the series resistance, and the parasitic capacitance. From equations 1, and 2, it is clear that scaling down the inductors's area would reduce the inductance value and its quality factor.

Consequently, for a fixed die area, the chip should comprise the minimum number of inductors in order to achieve a relatively high quality factor and reduce the mutual coupling between the on-die inductors.

In this design, we have arbitrarily considered that the inductor occupies an area of 1 mm^2. We used the CAD tool ASITIC to estimate the inductance value and its resistance. The results are shown in Table I. The quality factors of integrated inductors are relatively low compared to discrete ones. As previously mentioned, the main issue concerning the discrete inductors is its mounting on the die which is a separate process that raises the converter's manufacturing cost.

TABLE I: Extracted parameters of integrated inductors using ASITIC at 200 MHz versus a discrete inductor with 0302 CS package

	L1	L2	Discrete	Units
Inductance	1.59	1.15	1.7	nH
Series Resistance	0.230	0.226	0.038	Ω
Area	1	0.5	0.46	mm^2
Metal trace width	250	176.78	-	μm
Unloaded quality factor	8.68	6.39	20-30	-
Self resonant frequency	0.7	1	-	GHz

III. FDSOI Technology in Power Converter

The technology 28 nm fully depleted silicon on insulator (FDSOI) is emerging significantly in the digital applications. This technology allows the body biasing that acts as a back gate. For switch operation, it is also convenient to modulate the on-state resistance using this back gate voltage.

Table II shows the transistor specifications with different body voltages. It is noticed that when the body is connected to the gate, we obtain low leakage current when the transistor is off and low on-state resistance when it is on. Hence, the switch becomes less susceptible to parasitic noise when it is off and is able to supply high currents when it is on.

TABLE II: NMOS transistor specifications with different bulk connections

Bulk bias	0 V	VDD	V_G
Channel resistivity density λ_R ($\Omega.\mu m$)	554	465	466
Gate capacitance density λ_c (fF/μm)	1	1.1	1.2
Leakage current density (pA/μm)	44.6	365×10^3	38.6

The challenge in the FDSOI technology is the absence of the body diode of the transistors. This issue can be solved by mixing an FDSOI technology with a bulk technology on the same die. The bulk technology section can be used to implement the necessary body diodes to protect the circuit when a drift occurs in the inductor zero current switching.

The implementation of capacitors in FDSOI can be done in different ways. Table III shows different technology parameters. We used MOM capacitors for flying capacitor as they do not need additional masks and are not depending on voltage.

TABLE III: FDSOI 28 nm technology parameters

Number of metal layers	10 + Top metal
MOM capacitance density (M1 - M5)	$4\,fF/\mu m^2$
MOM bottom plate capacitance coefficient	3%
MOM max. applied voltage	1.8 V
MIM capacitance density	$15.9\,fF/\mu m^2$
MIM capacitance additional masks	3
MIM max. applied voltage	1.1 V
MOS capacitance density	$8\,fF/\mu m^2$
MOS bottom plate capacitance coefficient	8%

IV. 2:1 RESC converter topology

The 2:1 ReSC converters topologies can be generally categorized into single-ended and multiphase topologies. In each category, the circuits can be classified based on the inductor position [9]. The indirect and direct toplogies are depicted in Figure 1 (a) and (b), respectively. In the direct topology, the current of the inductor is in the same direction in charging and discharging phases. Hence, a DC current component exists which indicates that the power spectral density of the current is divided mainly between the DC and the switching frequency components [5].

Using a discrete inductor, the direct topology outperforms the indirect one since the inductor current has an appreciable DC current component that reduces the effect of the inductor resistance on the average. For the integrated inductors, the conductor width is comparable to the skin depth that causes the domination of the DC resistance across the operating frequency range. Hence, the difference in the performance between direct and indirect topology would not be significant.

In presence of a large parasitic inductance, which results from the bonding wires, large supply input current variations affect the single-ended converter supply voltages that could degrade the overall system efficiency. This issue is solved by using the multiphase topology. The multiphase ReSC converters comprise parallel stages of direct or indirect topologies as shown in Figure 1 (a) and (b). The phase shift between N-phases is conventionally equal to 360°/N. The current drawn from the supply is relatively constant which reduces the supply voltage variations in the presence of parasitic inductors.

Consider single and two phases indirect topologies similar to the ones shown in Figure 1 (a) and (c), the supply current I_{in} can be generally expressed as follows:

$$I_{\text{in}}(t) = I_{\text{Load}}/2 + \sum_{j=1}^{N} I_{\text{Lj}}(t)/2 \tag{3}$$

where I_{Load} is the average load current and I_{Lj} is the inductor current in the j-phase. In case of one phase, we have only one inductor, hence, the variations in its current is similar to the variation in the input current. Since the peak inductor current depends on the average load current, the variations in the input current become significant with large load currents. In the case of two phases, the inductor currents (I_{L1} and I_{L2}) are out-of-phase by 180° which results in almost a DC current

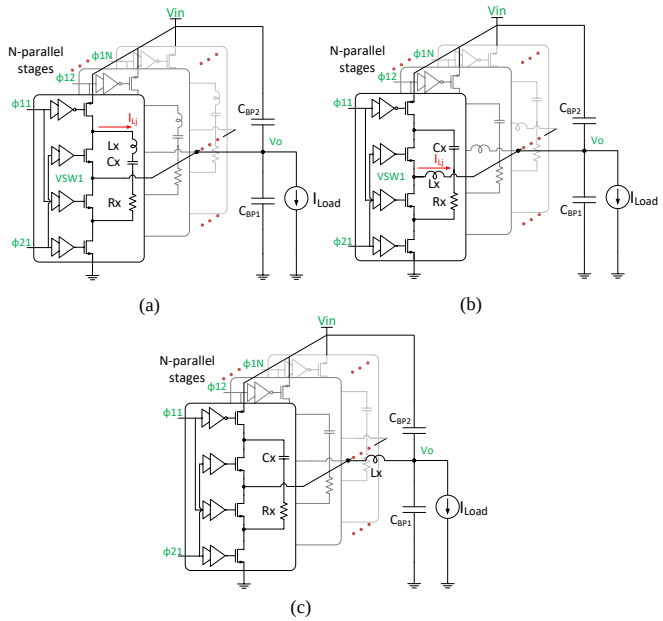

Fig. 1: ReSC converter topologies: (a) multiphase with indirect topology stages, (b) multiphase with direct topology stages, and (c) merged direct multiphase topology.

drawn from the source. Consequently, the supply variation in the presence of parasitic inductance is significantly reduced. Such conclusion can impose a constraint on the integrated resonance converter to have at least two phases to guarantee proper functionality of the system in the presence of inductive power access.

In the multiphase direct circuit, the inductors can be merged into one inductor [5] as shown in Figure 1 (c). To compare between the performance specifications of the indirect and merged direct topologies, we consider an area A that will be used for the flying capacitor (C_{Fly}). Table IV shows the comparison between the multiphase indirect and merged direct referenced to the single-ended converter. In the single-ended converter and assuming a negligible damping factor, the resonance frequency can be expressed as follows:

$$f_x \approx \frac{1}{2\pi\sqrt{L_x C_x}} \tag{4}$$

where L_x and C_x are the inductor and flying capacitor occupying an area A. The quality factor of the circuit is ($Q_x = R_{tot}^{-1}\sqrt{L_x/C_x}$). The converter's output resistance can be expressed as follows:

$$\begin{aligned} R_{eff} &= \frac{\pi R_{tot}}{4m\sqrt{1-m^2}} \cdot tanh\left(\frac{\pi m}{2\sqrt{1-m^2}}\right) \\ &\approx \frac{\pi^2}{8} \cdot \frac{R_{tot}}{1-m^2} \approx \frac{\pi^2}{8} \cdot R_{tot} \end{aligned} \tag{5}$$

where m is the damping factor ($m = 1/(2Q_x)$) and R_{tot} is the total resistance in the charging and discharging path which is equal to ($R_{tot} = R_x + 2R_{SW}$) where R_{SW} is the switch resistance.

For simplicity, we assume that the inductor's resistance is dominating. The efficiency of the converter, considering only the conduction loss, can be expressed as:

$$\eta = 1 - \frac{I_{DC}}{v_{oNL}} \cdot \frac{\pi^2}{8} \cdot \frac{R_{tot}}{1-m^2} \tag{6}$$

where v_{oNL} is the no-load output voltage and I_{DC} is the DC output current. For a certain load current, the efficiency is inversely proportional to the damping factor m and hence, it is directly proportional to the quality factor of the circuit.

In case of 2-phase indirect topology, the area of the capacitance is scaled by half ($\varepsilon = 0.5$) and hence, the capacitance value is scaled by 0.5 but the inductance is scaled by $1/\sqrt{2}$ and its resistance remains constant as shown in equation 1. Its resonance frequency is higher than the resonance frequency of the single-ended converter. However, the output resistance of the converter is reduced by the number of interleaved phases. In case of 2-phase merged direct topology, the inductor is kept occupying the whole area while the capacitance only is scaled by 0.5. The resonance frequency and the output resistance are kept approximately the same as the single-ended topology, however, the quality factor is doubled.

TABLE IV: Comparison between different ReSC topologies with a fixed design area (A)

	C_{Fly}	L	R_L	f_{sw}	Q	R_{out}
Single-ended	C_x	L_x	R_x	f_x	Q_x	R_o
2-phases indirect	$C_x/2$	$L_x/\sqrt{2}$	R_x	$1.68f_x$	$1.189Q_x$	$R_o/2$
2-phases merged direct	$C_x/2$	L_x	R_x	$\sim f_x$	$2Q_x$	R_o

Therefore, the 2-phases indirect topology outperforms the 2-phases merged direct topology in case of high load currents due to its lower output resistance and consequently, lower conduction loss. The 2-phase merged direct topology outperforms the indirect topology in case of low load currents as it has a lower switching frequency which results in lower switching losses.

V. Transistor-based simulation results

The design specifications of the proposed converters are shown in Table V. The die area is shared between the bypass and flying capacitors. All the capacitors are considered to be implemented using MOM capacitors only. The inductor is assigned to occupy 80% of the die area.

TABLE V: ReSC converter design specifications

V_{in}	1.8 V	V_o (min.)	0.7 V
Area	1.25 mm^2	Inductor Area	1 mm^2
C_{Fly}	2×1.25 nF	C_{BP}	2×1.25 nF

Figure 2 shows the simulation results in case of ideal switches with on-resistance of 50 mΩ. The switching frequencies of the single-ended, merged direct, and indirect topologies are 78, 111, and 131 MHz, respectively. It shows that in the

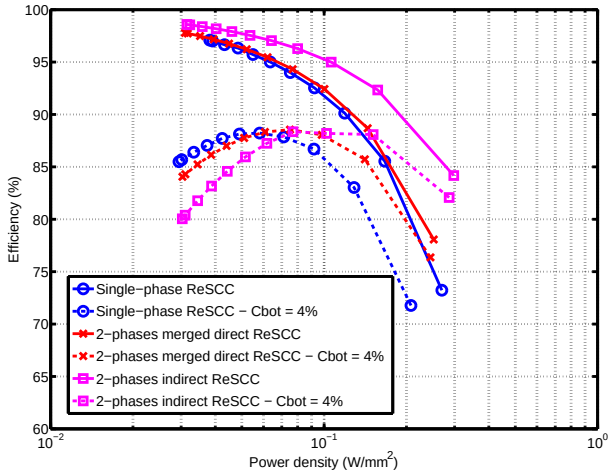

Fig. 2: Efficiency versus power density for different ReSC topologies.

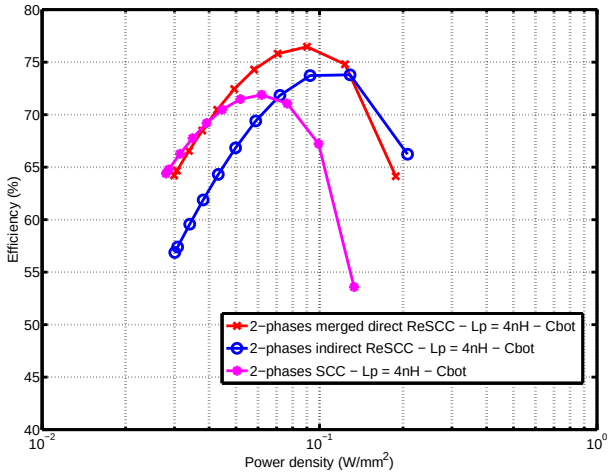

Fig. 3: Comparison between 2-phase indirect and merged direct ReSC converter and a switched capacitor converter.

absence of the switching losses, represented by the bottom plate capacitance of the flying capacitor, the 2-phases indirect topology has the highest efficiency as its output resistance is the lowest. However, when the bottom plate capacitor is considered, the 2-phases merged direct topology outperforms the 2-phases indirect one at the light loads. The single-ended shows a comparable performance to the merged direct topology but this performance is severely deteriorated in the presence of a parasitic inductor in series with the supply as previously explained.

In Figure 3, a comparison between the switched capacitor and the resonance switched capacitor converters on transistor level is depicted. The switched capacitor converter has two phases and its switching frequency is 125 MHz optimized to minimize the losses at DC output current of 150 mA. The resistance series with the capacitance is 20 mΩ. The sizes of the switches are optimized to achieve the highest efficiency at 100 mW/mm^2. In the simulations, we consider the presence of the bottom plate capacitance and a parasitic inductance of 4 nH. At a power density of 100 mW/mm^2, the merged direct has about 30% lower losses with respect to the switched capacitor converter. The merged direct has the highest peak efficiency of 76% at 90 mW/mm^2. The switched capacitor shows a comparable performance to the merged direct at light loads.

VI. Conclusion

The fully integrated implementation of the resonance switched capacitor converters using an on-chip aircore inductors in a recent CMOS node has been investigated. This implementation outperforms the conventional switched capacitor converter even with the poor quality factor of the integrated inductor. It alleviates the extra-manufacturing process to mount the discrete inductors on top of the die. On a die of 1 mm^2, the merged direct topology has a peak efficiency of 76.4% at a power density of 90 mW/mm^2. It has about 30% lower losses compared to the fully switched capacitor converter. The results highlight the potential for its seamless implementation into this promised CMOS technology.

References

[1] S. R. Sanders, E. Alon, H. P. Le, M. D. Seeman, M. John, and V. W. Ng, "The Road to Fully Integrated DC-DC Conversion via the Switched-Capacitor Approach," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[2] G. Pillonnet and N. Jeanniot, "Effect of CMOS Technology Scaling on Fully-Integrated Power Supply Efficiency," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, Mar. 2016, pp. 1–5.

[3] K. Kesarwani, R. Sangwan, and J. T. Stauth, "4.5 A 2-phase resonant switched-capacitor converter delivering 4.3w at 0.6w/mm2 with 85% efficiency," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 86–87.

[4] C. Schaef, K. Kesarwani, and J. T. Stauth, "20.2 A variable-conversion-ratio 3-phase resonant switched capacitor converter with 85% efficiency at 0.91w/mm2 using 1.1nh PCB-trace inductors," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb. 2015, pp. 1–3.

[5] K. Kesarwani and J. T. Stauth, "The direct-conversion resonant switched capacitor architecture with merged multiphase interleaving: Cost and performance comparison," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2015, pp. 952–959.

[6] L. G. Salem and P. P. Mercier, "A single-inductor 7+7 ratio reconfigurable resonant switched-capacitor DC-DC converter with 0.1-to-1.5v output voltage range," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2015, pp. 1–4.

[7] S. Pasternak, C. Schaef, and J. Stauth, "Equivalent resistance approach to optimization, analysis and comparison of hybrid/resonant switched-capacitor converters," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2016, pp. 1–8.

[8] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of solid-state circuits*, vol. 34, no. 10, pp. 1419–1424, 1999.

[9] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant-Switched Capacitor Converters for Chip-Scale Power Delivery: Design and Implementation," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6966–6977, Dec. 2015.