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***Abstract*— The design of a fully digital tunable sub-GHz Ultra-wide band (UWB) pulse generator is presented. The pulse generator has been implemented in a 0.13µm CMOS technology. Post-layout simulation shows that the proposed pulse generator achieves UWB pulses with a 900mVpp magnitude while consuming 27pJ by pulse under 1.2V supply voltage. The tuning capabilities allow the center frequency setting between 400MHz and 610MHz.**

***Keywords*—CMOS, UWB, Fully digital, sub-GHz, pulse generator**

I. INTRODUCTION

Ultra-Wide Band (UWB) communications are regulated by the Federal Communications Commission (FCC) Since 2002 [1]. Ultra-Wide-Band Impulse Radio (IR-UWB) is a well-known technique based on the transmission of short duration pulses which demonstrated great potential for high and low data rates in short range wireless communications in the 3.1-10.6GHz bandwidth [2]. The IEEE 802.15.4a standard [3] also allows the use of the sub-GHz UWB bandwidth. In addition of the IR-UWB advantages which have been demonstrated in the 3.1-10.6GHz bandwidth such as low power consumption and high data rate capabilities, the use of the sub-GHz UWB band allows low transmission path loss and potentially better performance regarding the power consumption because active components are working far away from their cutoff frequency even when low cost technologies are used.

Very few works regarding pulse generators have been published in the UWB sub-GHz band. In [4] a relaxation oscillator followed by a power amplifier is used to generate the pulses. The pulse generator is tunable and shows a power consumption of 78pJ/bit. In [5], a pulse generator, which uses a finite impulse response (FIR) digital filter, demonstrates a very low power consumption of 30pJ/bit but no solution is implemented to compensate Process Voltage and Temperature (PVT) variation. In [6] a tunable architecture based on a delay line and an elementary pulse combiner is proposed, but the output magnitude (337mV_{pp}) does not exploit the full range of the allowed peak power limitation of the sub-GHz band.

In this paper, we present a fully digital and tunable pulse generator for the sub-GHz UWB channel of IEEE 802.15.4a. Post-Layout simulations in a 0.13µm CMOS technology show that IEEE 802.15.4a compliant pulses of 900mV_{pp} magnitude with a center frequency of 500MHz and a 650MHz -10dB bandwidth could be generated. The power consumption is 2.7mW at 100MHz that gives an energy consumption of 27pJ by pulse. The power consumption reduces at 192µW for 100 kHz data rate. The simulated center frequency tuning range is 200 MHz allowing PVT compensation.

This paper is organized as follows. In section II an analysis of Ultra-Wide Band communications regulations in the UWB sub-GHz band of the 802.15.4a standard gives relationship between data rate and the maximum allowed pulse magnitude. Section III presents the architecture and the design of the fully digital tunable generator in a 0.13µm CMOS technology. Post layout simulation results are given in section IV.

II. ULTRA-WIDE BAND COMMUNICATIONS REGULATIONS ANALYSIS IN THE UWB SUB-GHZ BAND

The IEEE 802.15.4a standard [3] defines an UWB sub-GHz channel of 499.9MHz -3dB bandwidth centered on 499.9MHz. Its -10dB (resp. -18dB) bandwidth is about 650MHz (resp. 800MHz) as shown in Fig. 1.

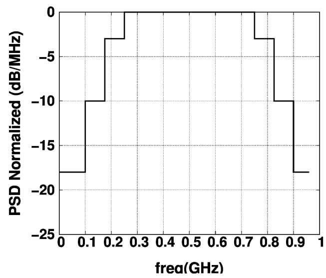


Fig. 1. IEEE 802.15.4a standard UWB sub-GHz channel.

As shown in [7], and presented in Fig. 2 in the case of a 5.3 GHz bandwidth UWB pulse, a pulse s(t) could be approximated by a combination of elementary pulses:

$$s(t) = \sum_{n=1}^{N} A_n p_n (t - \sum_{p=1}^{n-1} \tau_p) \quad (1)$$

where $p_n(t)$ is the mathematical expression of the elementary pulse which has a magnitude A_n and a duration τ_n (with $\tau_0 = 0$). In [7], a method to approximate Gaussian-like pulse is presented. This method uses N sinusoidal elementary pulses $p_n(t)$ with a constant duration τ.

The pulse length τ in this simplified case is:

$$\tau = \frac{1}{2.f_0} \qquad (2)$$

where f_0 is the central frequency of the channel.

In order to define N, the number of elementary pluses, the following equation of Gaussian pulse is used :

$$s(t) = A.\exp(-\alpha t).\sin(2\pi f_0 t + m.\frac{\pi}{2}) \qquad (3)$$

where A is the magnitude of the Gaussian pulse and α is related to the $-X_{dB}$ bandwidth as follows:

$$\alpha = \left(\frac{-\pi.BW_{-XdB}}{2.\ln(10^{X/10})} \right) \qquad (4)$$

In (3) m=1 for an odd oscillation number and m=0 otherwise. Because a Gaussian pulse has an infinite duration, for practical design consideration s(t) is bounded in this work to oscillations having a magnitude greater than 10% of the Gaussian pulse magnitude. Using this approximation, (3) and (4) the minimum number of elementary pulses N defined in (1) is 3 if m=0 and 4 otherwise for the sub-GHz UWB IEEE 802.15.4a channel.

The magnitudes of elementary pulses and their durations are given in Table I for the sub-GHz UWB IEEE 802.15.4a channel for N=3 and N=4. The corresponding time domain waveforms are given in Fig. 3.

Peak power magnitude and average power magnitude of UWB communications are regulated by FCC which sets a peak value of -7.9dBm and an average value of -49.1dBm/MHz for the PSD in the sub-GHz band [8]. While the peak PSD value depends only on the UWB pulse shape and magnitude, the mean PSD value depends also on the data rate. Fig. 4 gives the allowed maximum magnitude as a function of the data rate for the Gaussian pulse defined in (3) to comply with FCC regulation in the sub-GHz UWB band. Fig. 4 shows that the UWB pulse peak to peak magnitude should not exceed 0.9V even at low data rates.

In this work, we choose to design a pulse generator using four elementary pulses. Indeed using four elementary pulses instead of three enables more setting capabilities in the architecture which allow an easier control of the pulse shape in order to be compliant with the IEEE802.15.4a standard.

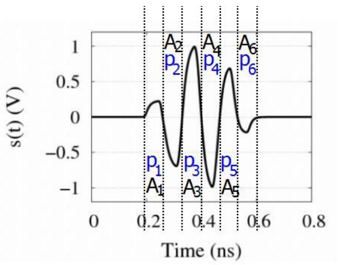


Fig. 2. Example of Gaussian 5.3 GHz UWB pulse formed by N=6 elementary pulses[7].

TABLE I. ELEMENTARY PULSES PARAMETERS FOR A GAUSSIAN PULSE APPROXIMATION IN THE SUB-GHZ IEEE 802.14.4A BAND.

n	1	2	3	4
τ (ns)	1	1	1	1
A_n (N=3)	-0.537	1	-0.537	/
A_n (N=4)	0.260	-1	1	-0.260

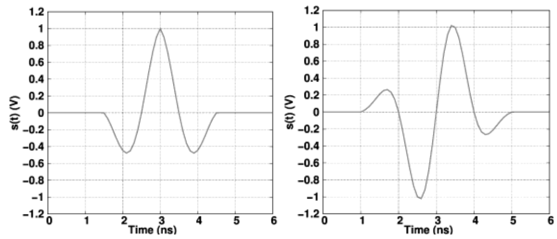


Fig. 3. Time domain waveform for a 3 and 4 elementary pulses Gaussian approximation

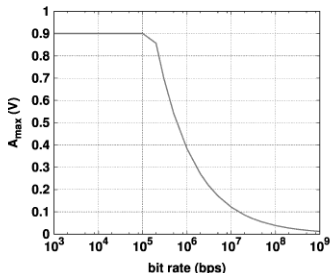


Fig. 4. Maximum peak to peak magnitude of the UWB pulse as a function of data rate allowed for sub-GHz UWB communications

III. DESIGN OF FULLY DIGITAL UWB SUB-GHZ PULSE GENERATOR

The UWB pulse generator architecture is given in Fig. 5. It is composed of two main functions: an elementary pulse generator and a pulse combiner. The elementary pulse generator provides the four elementary square pulses $p_{sqn}(t)$ when it receives a trigger edge. From the outputs of the elementary pulse generator, the pulse combiner gives the four oscillations $p_n(t)$with the right magnitude of the UWB pulse and drives the 50 Ω antenna.

A. *Elementary pulses generator*

The elementary pulses generator is composed of a voltage control delay line (VCDL) followed by a logic edge combiner. The VCDL is based on tunable delay buffers as shown in Fig. 5. The delay cells are built up of two CMOS inverters loaded by a capacitor C in series with a NMOS as shown in Fig.5. The widths of elementary pulses could be modified thanks to the variation of the voltage VCTRL applied on the MOS in series with the capacitor. C is sized to achieve a delay of 500ps (C=850fF) when VCTRL is equal to its nominal value 0.7V. The other part of the VCDL is built up with high speed inverters, which are used as buffers for each output. Phantom cells are inserted to keep a constant load between each elementary delay cells.

The second part of the elementary pulses generator is the logic edge combiner circuit, which combines the five edges given by the VCDL. As shown in Fig. 5, the negative pulses $p_{sq1}(t)$ and $p_{sq3}(t)$ are generated thanks to a NXOR-function. The edges OUT_1 and OUT_2 form $p_{sq1}(t)$ while $p_{sq3}(t)$ is generated by the combination of the edges OUT_3 and OUT_4. The positive pulses $p_{sq2}(t)$ and p_{sq4} (t) are generated by a XOR function. The edges OUT_2 and OUT_3 will form $p_{sq2}(t)$ while p_{sq4} (t) is generated by combining the edges OUT_4, OUT_5. Each logic gate is followed by a buffer to reduce the rise time.

B. Pulses combination circuit

In order to generate a Gaussian-like UWB pulse, elementary pulses should have a sinusoidal shape. Thus the square pulses $p_{sqn}(t)$ must be transformed into sinusoidal ones. To achieve this transformation, the drive capacities of the pulses combination circuit inputs buffers have been reduced by choosing a W/L ratio smaller than the one of the output buffers of the logic edge combiner (W_1/L). Finally each elementary pulse is injected to a common source transistor in order to set its magnitude as shown in Fig. 5.

Transistors sizes ratios are chosen in a way to achieve the magnitude to comply with the FCC IEEE mask and to be able to drive the 50Ω antenna. A capacitor of 5pF is added at the end of the pulse combination circuit for the DC isolation of the antenna.

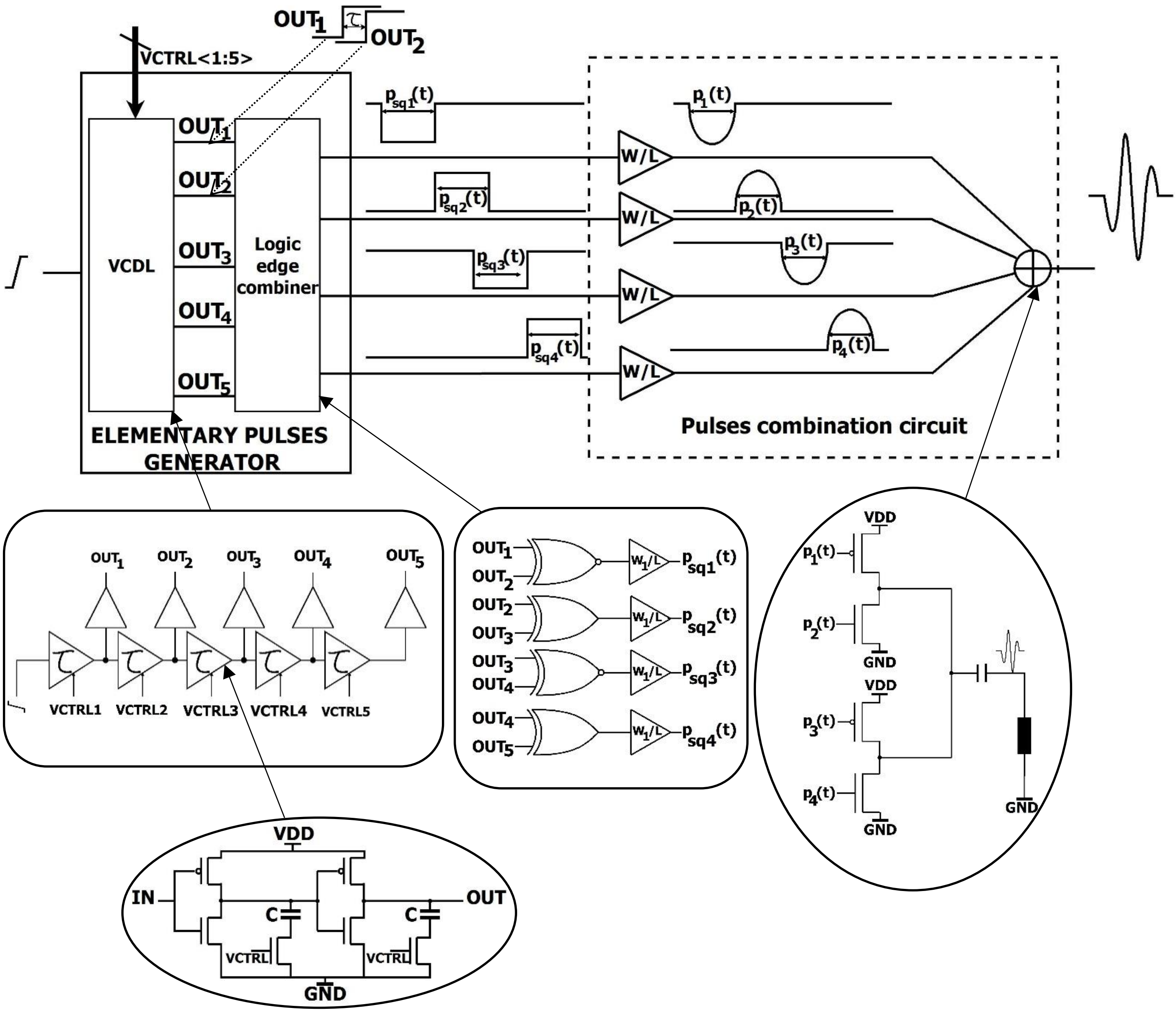


Fig. 5. Pulse generator architecture

IV. POST-LAYOUT SIMULATION AND COMPARISON

The UWB pulse generator has been implemented in a 0.13µm STMicroelectronics technology. The layout, given in Fig. 6, shows a core size of 390µm by 370µm. Post-layout simulations have been made using the software Cadence for a supply voltage of 1.2V.

Fig. 7.a represents the time domain UWB pulse generated using nominal settings (VCTRL=700mV). The peak to peak voltage magnitude which is about 900mV reach the maximum allowed peak value as indicated in Fig 4. Fig. 7.b shows the spectrum of the UWB pulse generated. The central frequency is 496MHz and the -10dB and -18dB bandwidths are 629.76MHz and 792.5MHz respectively. The average current consumption of the generator, simulated for a PRF of 100MHz, is 2.24mA with a supply voltage of 1.2V. That gives a 2.7mW average power consumption and a 27pJ energy consumption by pulse for this data rate. A figure of merit η is introduced to achieve a comparison of the energy consumed by pulse regarding the pulse magnitude:

$$\eta = \frac{E}{V_{pp}} \qquad (5)$$

The proposed pulse generator shows a simulated value of η of 30pJ per pulse and by Volt which compares favorably with other published UWB sub-GHz pulse generators as shown in table II. The VCDL is controlled by external tuning voltages, which give the possibility to adjust each delay time (pulse length and central frequency) in order to correct PVT variations. The central frequency could be tuned from 400MHz to 610MHz when the VCTRL varies from 500mV to 900mV as shown in Fig. 7.b. Simulated performances of the proposed sub-GHz pulse generator are summarized and compared to other published results in Table II. The pulse generator presented in this work has the lowest energy per pulse (27pJ/pulse) and presents the largest peak to peak output voltage.

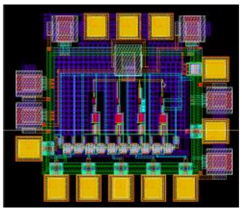
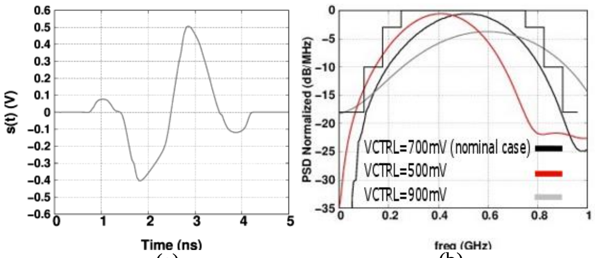


Fig. 6. Pulse generator layout



(a) (b)

Fig. 7. Time domain waveform of the sub-GHz pulse (a) and its spectrum normalized for different VCTRL settings (b)

TABLE II. SUMMARY AND COMPARAISON WITH STATE OF ART

Reference	[4]	[5]	[6]	This work
Technology (µm)	0.13	0.18	0.5	0.13
V_{DD} (V)	2.5	1	3	1.2
V_{pp} (mV)	120	-	372	900
E (pJ/pulse)	78	30	130	27
BW_{-10dB} (MHz)	550	150	500	629.76
Consumption (mW) @ PRF(MHz)	0.078 @ 1	1.5 @ 50	1.3 @ 10	2.7 @ 100
η (pJ/pulse/V)	650	-	349	30

V. CONCLUSION

In this paper, a fully tunable UWB pulse generator has been designed and implemented in a 0.13µm CMOS technology. Post-Layout simulation results show its ability to generate sub-GHz UWB pulses with a peak to peak magnitude voltage of 0.9V. The pulse generator consumes only 27pJ/pulse and allows a central frequency tuning range from 400MHz to 610MHz.

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