An Accurate kTC Noise Analysis of CDS Circuits

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***Abstract*—This work presents an analytical analysis of the thermal noise in widely used correlated double-sampling (CDS) circuits. The objective is to provide designers with simplified noise formulas essential for the design and optimization of such blocks. The obtained analytical results are confirmed with SpectreRF noise, SpectreRF transient noise and ELDO transient noise simulations.**

***Keywords*—Noise, CDS, kTC, PSD, SNR, offset, thermal.**

I. Introduction

In IC design, reducing the low-frequency noise and DC offset has become mandatory given the reduction of the dynamic range resulting from the suppy voltage reduction. Several circuit techniques have been proposed as solutions to the above-mentioned challenge, such as the autozero (AZ), the correlated double-sampling (CDS) and the chopper stabilization (CHS) [1]. CDS is a very effective technique for offset and low frequency noise cancellation. Similarly to AZ, CDS is a sampled-data technique, except that the signal is sampled twice and eventually the difference between these two samples is taken, within the same clock period. Mathematically, the CDS transfer function imposes a zero at the origin of frequency which cancels any offset and drammaticaly reduces the low frequency noise [1]. Historically, the CDS technique has been originally introduced to reduce the noise generated in charged-couple devices (CCDs) [2]. Progressively, CDS has been extensively used in sampled-data systems and switched-capacitor (SC) circuits, in an increasing variety of possible applications, such as CMOS image sensors (CIS) [3] or analog front-end (AFE) for biomedical applications [4].

Despite CDS circuits reduce dramatically the low frequency noise, they remain limited by circuit non-idealities. Indeed, CDS circuits are mainly limited by analog switches non-idealities (on and off resistances), charge injection and thermal noise, the latter usually referred to as kTC noise [5]. The sampled noise voltage variance (kT/C) is, by definition, inversely proportional to the capacitance. On the contrary, both power and silicon area are directly proportional to the capacitance, resulting into a noise/power-area trade-off [6]. From a design perspective, it is necessary to be fully aware of the capacitances ultimately limiting the circuit performance. kTC noise analysis of SC circuits is never a simple task, considering that the noise transfer function, for these circuits, changes in time. Modern CAD simulators are useful in the estimation of the overall noise features, despite they require a very high accuracy set-up, resulting into extremely long simulations. Moreover, they don't provide simple analytical expressions to optimize the SC circuit noise.

In this perspective, this paper presents a simple and comprehensive kTC noise analysis of three different CDS circuits. It is organized as follows: Section II overviews the three proposed CDS structures, namely, a fully-passive CDS, a voltage buffer-based CDS and an amplifier-based CDS. Section III presents a detailed kTC noise analysis of each proposed CDS circuit. Section IV presents the noise simulations, showing a good match with the analytical calculations of Section III, and compares the three proposed structures. Section V concludes the paper.

II. CDS Circuits

The three proposed CDS circuits are depicted in Fig. 1, namely, a fully-passive CDS, Fig. 1(a), a voltage buffer-based CDS, Fig. 1(b), and an amplifier-based CDS, Fig. 1(c). The circuit of Fig. 1(a) embeds passive elements only. Referring to the timing diagram shown in Fig. 1(d), a generic input signal voltage, V_1, is first sampled on the capacitor C_1, at the end of phase ϕ_1. Secondly, at the end of phase ϕ_2, a second input signal voltage, V_2, is sampled on the capacitor C_2. During the third phase ϕ_3, the charge conservation principle leads to an output voltage equal to

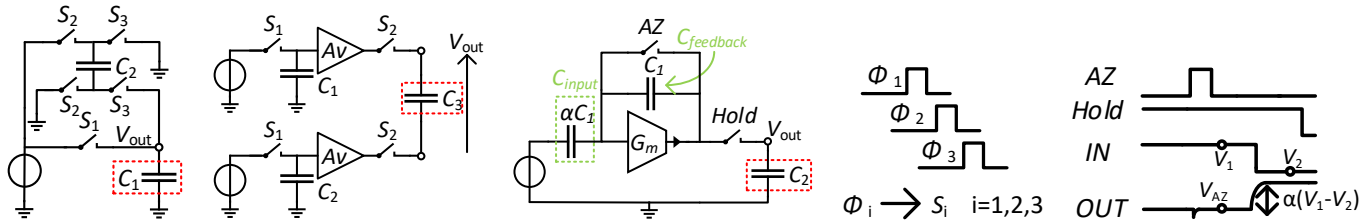
$$V_{out} = \frac{V_1 C_1 - V_2 C_2}{C_1 + C_2} = \frac{V_1 - V_2}{2}, \tag{1}$$

assuming that $C_1 = C_2$. Eq. (1) results into a CDS action, with a loss equal to two. From now on, we will refer to the fully passive CDS of Fig. 1(a) as CDS_1.

The circuit depicted in Fig. 1(b) consists of a voltage buffer-based CDS. Referring to the timing diagram shown in Fig. 1 (d), two independent input signals V_1 and V_2 are sampled on C_1 and C_2, respectively, during phase ϕ_1. In the next phase ϕ_2 the charge previously stored in C_1 and C_2 is transferred, through the two voltage buffer of gain A_v, to the output capacitor C_3. At the end of this phase, the voltage across C_3 is

$$V_{out} = A_v \left(V_1 - V_2 \right). \tag{2}$$

Referring to (2), A_v is the gain of the voltage buffer. In case of source follower stages, featuring body effect, $A_v = 1/n$, where n is the slope factor (larger than one), this accounting for the body effect in MOS transistors, [7]. A_v takes values closer to one for source to bulk connected devices. As in the previous case, Eq. (2) represents a CDS, with a loss accounting for the source follower non-idealities, i.e. $n > 1$. From now on, we will refer to the CDS of Fig. 1(b) as CDS_2.



(a) (b) (c) (d) (e)

Fig. 1. Schematic of the three proposed CDS circuits with the timing diagrams: (a) fully-passive CDS, (b) voltage buffer-based CDS, (c) amplifier-based CDS, (d) timing diagram for (a) and (b), (e) timing diagram for (c).

Fig. 1(c) shows an amplifier-based CDS. Referring to the timing diagram of Fig. 1(e), the amplifier (transconductor) is first autozeroed. This phase, i.e. AZ, reduces the low frequency noise and the offset of the amplifier [1] and resets the feedback capacitor C_1. After this phase, in the scenario that the input signal, to the amplifier, toggles between the level V_1 and the level V_2, the amplifier output variation, i.e. ΔV_{out}, results in

$$\Delta V_{out} = \alpha \left(V_1 - V_2 \right), \tag{3}$$

being $\alpha \cong -C_{input}/C_{feedback}$ the closed-loop gain. As in CDS_1 and CDS_2, Eq. (3) shows the difference of the input signal levels, so a CDS. From now on, we will refer to CDS of Fig. 1(c) as CDS_3.

III. Noise Calculation in CDS Circuits

Objective of Section III is to derive the detailed kTC noise for each CDS circuit. It is important to remember that for a thermal noise source, having a constant Power-Spectral Density (PSD) S_n, its corresponding noise variance is equal to

$$V_n^2 = S_n \cdot NB, \tag{4}$$

where NB is the noise bandwidth, defined as

$$NB = \left(1/H_n^2\left(0\right)\right) \cdot \int_0^\infty \left|H_n(f)\right|^2 df. \tag{5}$$

In (5), $H_n(f)$ is the noise transfer function. The noise transfer functions encountered in this work are of three types: 1^{st}-order low-pass (LP), 2^{nd}-order LP (with zero) and 2^{nd}-order band-pass (BP)

$$H_n|_{1^{st}}(f) = \frac{1}{1+\frac{jf}{f_c}} \qquad H_n|_{2^{nd}LP}(f) = \frac{1+\frac{jf}{f_z}}{1+\frac{jf}{f_0 \cdot Q}+\left(\frac{jf}{f_0}\right)^2}$$

$$H_n|_{2^{nd}BP}(f) = \frac{\frac{jf}{f_0}}{1+\frac{jf}{f_0 \cdot Q}+\left(\frac{jf}{f_0}\right)^2}, \tag{6}$$

for which the NB is equal to

$$NB|_{1^{st}} = \frac{\pi}{2} f_c \qquad NB|_{2^{nd}LP} = \frac{\pi}{2} f_0 Q \left[1+\left(\frac{f_0}{f_z}\right)^2\right]$$

$$NB|_{2^{nd}BP} = \frac{\pi}{2}\frac{f_0}{Q}, \tag{7}$$

respectively. Eq. (7) will be extensively used throughout the work.

1) CDS1: due to the thermal noise originating from the on-resistance of the switches, two uncorrelated kTC noise charge are injected in the switched capacitors C_1 and C_2 at the end of phase ϕ_1 and ϕ_2, respectively. In both phases ϕ_1 and ϕ_2, the on-resistor, R_{on}, of the switches and the capacitor form a RC low-pass filter. Applying (4), (6) and (7) to this case and considering $S_n = 4kTR_{on}$ results into noise variances equal to

$$V_{nC_1}^2|_{\phi_1} = \frac{kT}{C_1} \qquad V_{nC_2}^2|_{\phi_2} = \frac{kT}{C_2}. \tag{8}$$

During the third phase ϕ_3 the two capacitors share both their signal and uncorrelated noise charge, resulting into a noise voltage variance at the output node equal to

$$V_{nC_1}^2|_{\phi_3} = \frac{\left(C_1^2 kT/C_1 + C_2^2 kT/C_2\right)}{\left(C_1+C_2\right)^2}. \tag{9}$$

At the end of phase ϕ_3, due to the switch S_3, an additional kTC noise charge, uncorrelated with the one generated in the previous phases, is injected in C_1 [5], resulting into an overall output voltage variance equal to

$$V_{n_{out}}^2 = \underbrace{\frac{\left(C_1^2 kT/C_1 + C_2^2 kT/C_2\right)}{\left(C_1+C_2\right)^2}}_{\text{shared noise from } \phi_1,\, \phi_2} + \underbrace{\frac{kT}{C_1}\frac{C_2}{C_1+C_2}}_{\text{added noise from } \phi_3} = \frac{kT}{C_1}. \tag{10}$$

2) CDS2: under the assumption that $C_1 = C_2$ and exploiting the fully-differential structure, the small signal schematic of $CDS2$, from a noise perspective, simplifies to the half circuit shown in Fig. 2(a). The total output noise voltage variance of the circuit of Fig. 1(b) is then simply equal to twice the output voltage variance of Fig. 2(a). With refer to the small signal schematic, three noise sources have to be accounted for: the on and off resistances of the two switches, S_1 and S_2, and the saturated MOS transistor in the source-follower. The noise coming from the off-resistor R_{off} can be neglected as long as the corresponding time constant is much larger than the fraction of the period over which it is integrated (typically 1/3). The thermal noise (current) PSD of the saturated MOS transistor is $4kT\gamma G_m$, where $\gamma \triangleq G_m R_n$ is the thermal noise excess factor (R_n is the input referred thermal noise resistance) [7] and G_m the transconductance. Referring to Fig. 2(a), the voltage-controlled current source nG_mV_2 accounts for the additional transconductance due to the body effect [7]. During phase ϕ_1, R_1 is equal to the on-resistor, R_{on}, while R_2 is equal to the off-resistor, R_{off}. Evaluating the noise transfer functions related

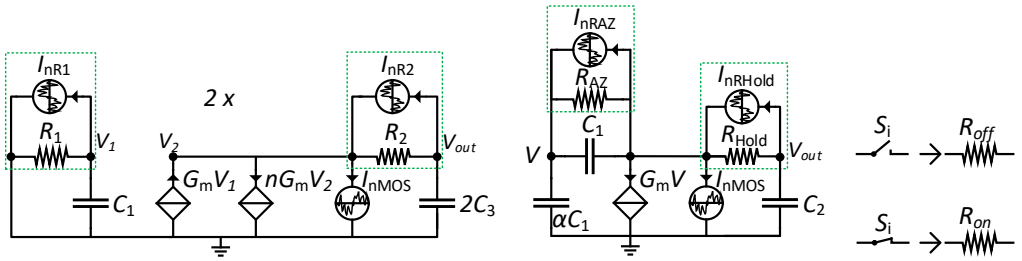


Fig. 2. Noise small signal schematic of CDS2 and CDS3: (a) CDS2, (b) CDS3, (c) switch equivalent model.

to the noise sources I_{nMOS}, I_{nR1} and I_{nR2} and applying (4), (6) and (7) leads to (considering the differential structure)

$$V^2_{nC_1}|_{\phi_1} \cong \underbrace{\frac{2kT}{C_1}}_{S_1\ R_{on}}. \tag{11}$$

Repeating the same procedure during phase ϕ_2 and exploiting again the differential structure results into a voltage variance on C_3

$$V^2_{nC_3}|_{\phi_2} \cong \underbrace{\frac{\gamma kT}{nC_3}\left(\frac{1}{1+nG_mR_{on}}\right)}_{\text{MOS channel}} + \underbrace{\frac{kT}{C_3}\left(\frac{nG_mR_{on}}{1+nG_mR_{on}}\right)}_{S_2\ R_{on}}. \tag{12}$$

In this case, R_1 is equal to the off-resistor, R_{off}, while R_2 is equal to the on-resistor, R_{on}. C_3 accounts for any additional parasitic contribute too, despite these have been neglected. Eventually, assuming that the noise on C_1 in ϕ_1 and on C_2 in ϕ_2 are uncorrelated, and that $G_mR_{on} \cong 0$, the overall kTC variance on the output capacitor C_3 is

$$V^2_{n_{out}} = A_v^2 V^2_{nC_1}|_{\phi_1} + V^2_{nC_3}|_{\phi_2} \cong \frac{2kT}{C_1} + \frac{\gamma kT}{nC_3}. \tag{13}$$

3) CDS3: this stage operates in two phases, namely, the AZ phase and the amplification phase, during which the amplifier provides a closed-loop gain α. In both phases, the overall kTC noise at the output of CDS_3 consists of two terms, both caused by the AZ and Hold switch resistance and the saturated MOS devices of the transconductor (OTA). First, the overall noise generated during the AZ phase which is frozen in αC_1 and eventually transferred to the feedback capacitor during the Amp phase. Secondly, the one generated in the amplification phase. Both noise variances add to the output, contributing to the overall kTC output thermal noise variance. Note that the frozen noise generated during the AZ phase could be canceled by a second CDS stage. The noise sampled on αC_1 at the end of the AZ phase can be calculated from the schematic shown in Fig. 2(b). In this case, R_{AZ} and R_{Hold} represent the on-resistor, R_{on}, of the switch AZ and $Hold$, respectively. Evaluating the noise transfer functions related to the noise sources I_{nMOS}, I_{nRAZ} and I_{nRHold} and applying (4), (6) and (7) leads to

$$V^2_{n\alpha C_1}|_{AZ} \cong \underbrace{\frac{\gamma kT}{\alpha C_1 + C_2}}_{\text{MOS channel}} + \underbrace{\frac{kT}{\alpha C_1}\frac{C_2}{\alpha C_1 + C_2}}_{\text{Hold } R_{on}}. \tag{14}$$

Referring to (14), it can be shown that the noise contribution of R_{AZ} is negligible with respect to the R_{Hold} one. Repeating the same procedure during the Amp phase results to

$$V^2_{nC_2}|_{Amp} \cong \underbrace{\frac{\gamma kT\left(1+\alpha^2\right)}{\alpha C_1 + C_2\left(1+\alpha\right)}}_{\text{MOS channel}} + \underbrace{\frac{kT}{C_2}\frac{\alpha C_1}{\alpha C_1 + C_2\left(1+\alpha\right)}}_{\text{Hold } R_{on}}. \tag{15}$$

In this case, R_{AZ} represents the off-resistor, R_{off}, of the switch AZ, whilst R_{Hold} the on-resistor, R_{on}. As in CDS2, the off-resistor contribution can be neglected. Assuming that the noise given by (14) and (15) are uncorrelated, the overall kTC variance at the output capacitor C_2 is then given by

$$V^2_{n_{out}} \cong \alpha^2 V^2_{n\alpha C_1}|_{AZ} + V^2_{nC_2}|_{Amp}. \tag{16}$$

As above-mentioned, at the end of the AZ phase, the noise variance (14) gets frozen in the input capacitor, αC_1, and simply added, multiplied by the square of the closed-loop gain, to the one generated in the next phase. In the above analysis, the parasitic capacitors are neglected. Note that the expression of the total output noise variance given by (16) includes the effect of the switches on-resistance which is usually neglected in the literature.

IV. Simulation Results

In order to confirm the analytical noise calculations presented in Section III we have performed noise simulations. All the presented CDS circuits have been simulated by using SpectreRF Noise and Transient Noise simulations and Eldo Transient Noise simulations. SpectreRF Noise performs AC small-signal analysis, deriving the noise transfer functions, for all the noisy elements, and eventually integrating the result (multiplied by the PSD, as in (4)) over the chosen frequency span. This is the same approach as reported in the analytical analysis of Section III. Indeed, all the analytical formulas reported in Section III have been validated, for each phase, by the means of SpectreRF Noise simulations. On the contrary, both Eldo and SpectreRF Transient Noise simulations model each noise source as a sum of sinusoids over the frequency range of interest, with random phase, and with amplitude equal to the given noise PSD [8]. Transient noise simulations become particularly useful when the noise is large or the circuit highly nonlinear. Moreover, these simulations are the best ones to assess how the noise evolves in time, which means in the most realistic

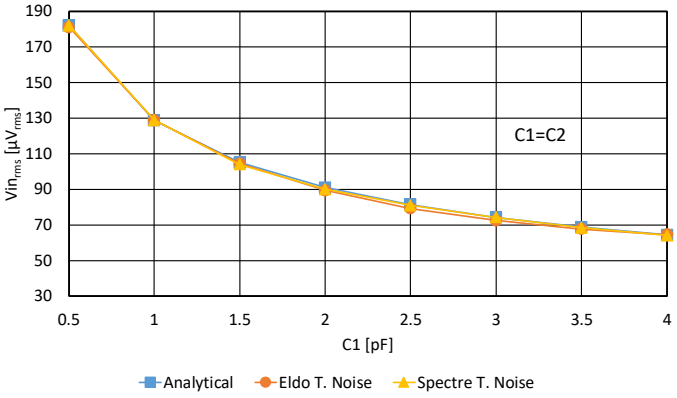


Fig. 3. Simulated and calculated RMS noise vs C_1 for CDS1.

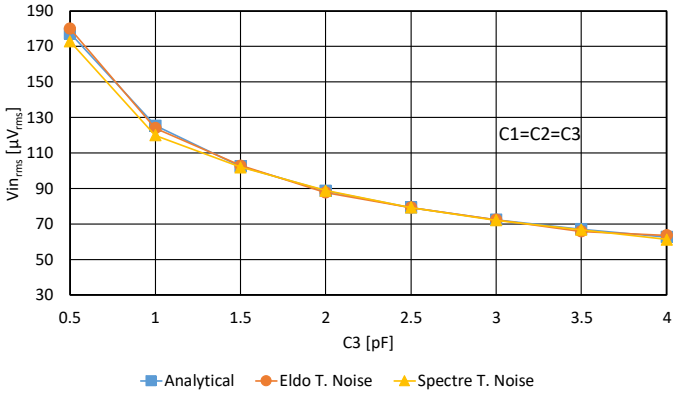


Fig. 4. Simulated and calculated RMS noise vs C_3 for CDS2.

condition. All the capacitors and switches of the circuits meet the condition $f_{th,max} \gg 1/(2\pi R_{on} C)$, where $f_{th,max}$ is a simulation parameter setting the maximum noise frequency. The simulation results, for the three CDS circuits, are shown in Figs. 3 to 5: both SpectreRF and Eldo match very well with the calculated noise. Particularly, for $CDS3$, Fig. 5 shows the effect of neglecting the switches on-resistance in the final computation, showing that they usually cannot be neglected. The noise is reported input-referred (output noise rms divided by the gain). The simulations are performed with $f_{th,max} = 8\ GHz$, 100 noise simulations, $T = 300\ K$, $\gamma = 1.5$, $n = 1.2$ and $G_m = 20\ \mu S$.

V. Conclusions

A noise analysis of three different CDS circuits is presented. Both Eldo Transient noise and SpectreRF Transient and noise simulations show a very good match with the results obtained analytically. The fully passive features of CDS1 make it particularly suitable for ultra-low power applications, despite the signal-to-noise ratio (SNR) is affected by the intrinsic signal loss due to the charge sharing mechanism. Moreover, it is not affected by any signal saturation, the latter usually due to active elements. One of the main advantages of this implementation is that the SNR can be improved without limiting the input

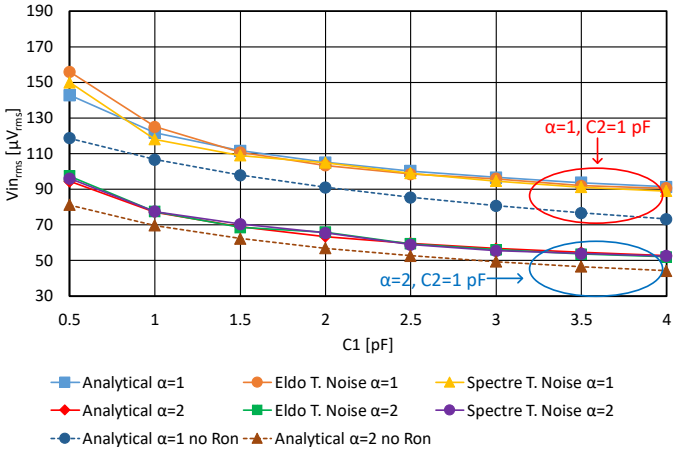


Fig. 5. Simulated and calculated RMS noise vs C_1 for CDS3.

signal range and only at the cost of more silicon area (larger capacitors). On the contrary, the amplifier-based CDS3 features an input-referred noise inversely proportional to the gain which depends directly on the size of the input capacitor. Hence, a lower noise is obtained at the cost of a lower input range, larger silicon area and power consumption. The advantage of CDS1 over CDS3 becomes even more obvious for values of γ larger than two. CDS3 remains a good solution for combining amplification with CDS. The voltage buffer-based CDS2 shows roughly the same noise performance than CDS1 at the cost of more power, area and non-linearity.

In addition, the presented work highlights the impact of switches on-resistance which are usually neglected. This is even more true whenever the designer needs to minimize as much as possible the noise due to active elements.

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