# Automated Information Flow Analysis for Integrated Computing-in-Memory Modules

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Abstract-Novel non-volatile memory (NVM) technologies offer high-speed and high-density data storage. In addition, they overcome the von Neumann bottleneck by enabling computingin-memory (CIM). Various computer architectures have been proposed to integrate CIM blocks in their design, forming a mixed-signal system to combine the computational benefits of CIM with the robustness of conventional CMOS. Novel electronic design automation (EDA) tools are necessary to design and manufacture these so-called neuromorphic systems. Furthermore, EDA tools must consider the impact of security vulnerabilities, as hardware security attacks have increased in recent years. Existing information flow analysis (IFA) frameworks offer an automated tool-suite to uphold the confidentiality property for sensitive data during the design of hardware. However, currently available mixed-signal EDA tools are not capable of analyzing the information flow of neuromorphic systems. To illustrate the shortcomings, we develop information flow protocols for NVMs that can be easily integrated in the already existing tool-suites. We show the limitation of the state-of-the-art by analyzing the flow from sensitive signals through multiple memristive crossbar structures to potential untrusted components and outputs. Finally, we provide a thorough discussion of the merits and flaws of the mixed-signal IFA frameworks on neuromorphic systems.

*Index Terms*—information flow analysis, neuromorphic computing, confidentiality

## I. INTRODUCTION

Non-volatile memory (NVM) technologies, such as spintorque transfer memory (STT-RAM/MRAM), phase-change random access memory (PCRAM), or redox-based random access memory (ReRAM), are promising candidates to substitute traditional RAM. NVMs offer dense storage with low leakage power, and enable computing-in-memory.

Combining conventional CMOS with NVMs results in complex high-performance designs referred to as neuromorphic systems. In modern design processes, electronic design automation (EDA) tools are used to assist the designer in the intricate implementation. However, the EDA tools need to be equipped to facilitate mixed-signal designs incorporating NVM-based accelerators. Furthermore, novel technologies introduce new security vulnerabilities (see Fig. 1) [1]-[3]. These new vulnerabilities are particularly worrying, because neuromorphic systems are a promising candidate for future applications, such as autonomous driving. Consequently, EDA tools need to be adapted to enforce security properties for mixed-signal designs, enabling a security-aware design flow in both the digital and analog domain. Availability, confidentiality, and integrity are the three cornerstones of hardware security that must be considered during the design process. While most research focuses on the integrity property [4], [5],



Fig. 1: Exemplary data leakage paths in a SoC using a CIM module (1T1R crossbar). Sensitive data flows from the trusted source (RISC-V) to untrusted peripherals or shared memories.

we concentrate in our work on the confidentiality property. Information flow analysis (IFA) is the state-of-the-art technique to enforce the confidentiality and integrity property in a design. IFA can track the flow of information from sensitive sources, such as encryption keys, to untrusted components, such as outputs or third-party intellectual property (IP). The analysis can be conducted statically to ensure confidentiality of a signal for every possible input combination. Although some work has been published supporting mixed-signal designs, no work has been released to the best of our knowledge that discusses the information flow for NVMs. Consequently, our work extends currently available IFA tools for neuromorphic mixed-signal systems and discusses its merits and shortcomings.

The major contributions of this paper are: (1) Development of information flow policies for NVM components. (2) An introduction of a crossbar driver masking scheme to *forbid* sneak paths in hardware. (3) A demonstration of the limitations of current mixed-signal IFA tools for neuromorphic systems.

## II. BACKGROUND

#### A. Information Flow Analysis

Information flow analysis represents the state-of-the-art technique to enforce the integrity and confidentiality property in a hardware design. The security analysis requires the hardware to be divided and labeled in different security classes. For instance, third-party IP, shared resources, or the output ports of the design are labeled untrustworthy. IFA determines whether information from high-security parts affects lower-security areas. The analysis relies on the non-interference property, aiming to prove that a change in sensitive values does not lead to an observable change in the untrustworthy components. The sensitive signals do not interfere with insecure components. Enforcing the properties during every step of the design



Fig. 2: Information flow (red arrows) in a memristor for different operational modes.

process, avoiding security vulnerabilities that threaten sensitive data, such as encryption keys or user data.

#### B. VeriCoq-IFT

The majority of IFA frameworks are designed to handle digital hardware. In contrast, the VeriCoq-IFT framework [6] introduces the capabilities to process mixed-signal designs when analyzing the information flow [7]. The analysis indicates whether sensitive information is leaked to the design's output signals. First, all output ports of the design must be labeled untrustworthy. Second, the user marks the sensitive signal in the design description and assigns it a sensitivity score. The conservative approach of VeriCoq-IFT propagates the sensitivity score of a signal at every signal assignment in Verilog. A variable receives the highest sensitivity score of all its inputs. Furthermore, operations can be labeled a sensitivity reducer, so that every time the sensitive signal passes the designated operation, the sensitivity score is reduced. If the signal reaches an output before it reaches a sensitivity score of zero, a data leakage is detected. The score system can be used to enforce that, e.g., the plaintext passes an AES round at least 12 times before it reaches the design's output as the ciphertext. Nevertheless, information flow rules for memristors have not been introduced yet.

## C. Non-volatile memories (NVMs)

NVMs represent a novel memory technology that takes advantage of the memristors. A memristor is next to a capacitor, a resistor, and an inductor, the fourth fundamental electrical component and stores information in the form of resistance. The resistance which can be set or reset using voltage pulses represents different states, which are called low resistive state (LRS) and high resistive state (HRS). To achieve high densities, memristors are organized in crossbar structures consisting of horizontal word and vertical bit lines, with a memristive cell at each cross point. These so-called passive crossbars suffer from sneak-path currents based on parasitic effects between the memristive cells limiting their reliability and retention. Consequently, more advanced cells have been proposed incorporating an active component, i.e., transistor, to connect/isolate the memristor from the remaining crossbar. However, as these novel devices have not been discussed in the VeriCoq-IFT framework yet [7], information flow policies need to be developed and implemented to enable the analysis of information flows of neuromorphic systems.

## III. THREAT MODEL

The developed framework aims to identify undesired information leakages in neuromorphic mixed-signal designs. The



Fig. 3: Functionality of VeriCoq-IFT [6] and the CoqIDE [10] in this work.

static analysis is conducted on register transfer level for the digital components, and transistor-level for the analog parts. We assume the attacker has access to the complete hardware description and intends to leak information via a direct flow of information at the primary outputs, no matter whether those outputs lie in the analog or digital domain. Side-channels are not considered. We assume the hardware vulnerabilities are already present at the design stage. It is not considered whether the observations of the primary outputs are obtained via remote access or physical access.

## IV. RELATED WORK

Khan et al. elaborate on possible attacks on information leaks on emerging non-volatile memories by using side channels caused by supply noise when writing and reading sensitive data [8]. Furthermore, current research has shown that datadependent write latencies can be exploited as a side-channel to leak sensitive information. By observing the time to access a memristor, information about the current content can be derived. The analysis regarding this vulnerability has also been conducted manually [2]. In addition to side-channels through the supply noise and the write latency, the supply current can be observed to gather information about sensitive signals [1].

Although multiple vulnerabilities in NVMs have been identified, no work has been presented to automate the identification of such vulnerabilities. Automated security-aware EDA tools are required to assist a hardware designer, inexperienced in hardware security, in identifying security vulnerabilities while maintaining a competitive design process.

#### V. FRAMEWORK

Therefore, we develop information flow rules for NVMs and integrate them in known IFA frameworks. Fig. 2 illustrates the direction of voltage and current for the three operational modes of a memristor: *set*, *read* and *reset*. For *set* and *read* the memristor is accessed from the terminal *ae*, so the current and voltage directions aim at the other terminal, called *oe* in this work. Fundamentally, the memristor requires a fourth mode to initialize the device after manufacturing. However, we do not consider this mode in our work because of its limited attack surface compared to the remaining other operational modes.

As stated in [7], for analog components, information is carried by voltage *and* current. Therefore, when setting the voltage at *ae*, the information can be read at both terminals of the memristor via the current. Due to the bidirectional behavior of a memristor [9], the information flow behaves bidirectionally, as illustrated with the red arrows in Fig. 2 for the three access modes.

```
// Mimicking the information flow
1
  // in memristors
2
  module memristor (ae, oe);
3
       inout ae, oe;
4
5
       assign ae = ae
                          oe;
6
       assign oe = ae
                          oe;
  endmodule
8
```

Fig. 4: High-level definition of a Verilog memristor module modeling the information flow.

We integrated the derived policies in VeriCoq-IFT and combined the framework directly with the CoqIDE [10] to provide an automated IFA framework. The tool flow of the combined VeriCoq-IFT and CoqIDE framework used in this work for the evaluation is depicted in Fig. 3. Although VeriCoq-IFT was introduced for third-party IP as proof-carrying hardware IP, it is solely used for the IFA in this work. VeriCoq-IFT has two operational modes: 1) It processes the Verilog-A/MS description of the complete design or 2) The designer provides a Verilog description of the digital domain, combined with Verilog modules of the analog modules that mimic the information flow of the device. The latter is required for the early design stages, when no Verilog-A/MS of the memristor is yet available. Then, Verilog modules mimicking the information flow of a memristor need to be introduced. The model does not depict the actual behavior of a NVM device, but models the information flow. Fig. 4 depicts the Verilog module mimicking the information flow of a memristor. Both terminals ae and oe are labeled 'inout'-ports. Additionally, each of the two ports depends on both terminals (line 6 & 7). The type of operation performed on the right side of the Verilog assignment is irrelevant, as only a flow of information needs to be modeled, not the functionality. This allows the framework to handle analog memristors in the digital domain.

Secondly, modern EDA tools allow the export of mixedsignal design into the language Verilog-A/MS. The analog and digital behavior of the components is embedded into a single description. A small number of Verilog-A/MS devices are available online [11]. VeriCoq-IFT processes the design to generate a design description in the language Coq, and theorems and proofs of the information flow rules. These rules are generated for all signals labeled sensitive in the design description. In this work, all sensitivity labels are set to 1 and no sensitivity reducers are instantiated, enforcing the noninterference property [12]. Therefore, every output port that can be influenced by the sensitive signal is labeled a leakage point. The three auxiliary files are forwarded to the theorem prover in the CoqIDE. If the theorems and proofs pass for the hardware description in Coq, no leakage is detected, otherwise VeriCoq-IFT identifies undesired flows of information.

## VI. DEMONSTRATION

In this work, we present the functionality and limitations of the presented framework using three individual integrated NVM-based mixed-signal designs. We assume the NVM block is integrated on a system-on-chip (SoC) accelerator. We focus our evaluation on the analog domain to illustrate the capabilities and shortcomings of the implemented framework. Fig. 5 illustrates the analog domain of the SoC and marks one identified leakage path in red. The surrounding circuitry enables in this example design the orchestration of both passive and active crossbar arrays. Following, we conduct three experiments to highlight the obstacles of IFA to neuromorphic systems and ultimately the shortcomings of the IFA framework. The internals of both crossbar structures are shown in Fig. 5 (b) and (d). The two crossbar structures can each be integrated into the circuitry (Fig. 5(a)) by replacing the blue abstract crossbar. Furthermore, we propose a masking mechanism that enforces the intended usage of the NVM module (see Fig. 5 (c)), which would replace the drivers shown in Fig. 5 (a).

## A. 1R Crossbar Accelerator

The memory cell of a passive crossbar consists of a single memristor. Hence, the crossbar itself acts like a network of resistances, allowing a bidirectional information flow. The digital domain limits the information flow based on the implemented output signals, i.e., to compute a vector-matrix multiplication, or to communicate the result by an input signal. Fig. 5 (b) exemplifies in red one possible information leakage path additionally to the intended flow of information. In addition to the intended flow of information from A to B, the undesired sneak paths are identified too (see A to O) [13]. Overall, the information flow in passive crossbars is considered complex, since there is no clear direction and the information can be transferred alternating between the analog and digital domain.

## B. 1T1R Crossbar Accelerator

While passive crossbar introduces sneak path currents limiting their usability, active crossbar aims to solve this by extending the NVM cell by an active component [13]. Fig. 5 (d) illustrates an active crossbar using a transistor as a selector component to separate unselected cells from the crossbar. However, our experiments show that the information flow, determined by VeriCoq-IFT, of an active crossbar matches the flow of a passive crossbar. *VeriCoq-IFT performs a static analysis of the design which does not take into account the "intended" usage of the selector transistors. Consequently, the framework classifies the NVM module as leaky.* 

## C. Active Crossbar Accelerator with Access Mask

To secure the information flow through crossbar arrays, we propose a hard-wired *access mask* enforcing the intended usage of the selector transistors. We implement this *access mask* within the driver circuitry of the NVM block. The mask allows only a fixed set of driver voltages to be applied to the crossbar, as shown in Table I and is implemented with a lookup table (see Fig. 5 (c)). The lookup table forbids operational modes that can simultaneously write to multiple rows, thus omitting sneak paths. For instance, if the memristor in row m and column n (green) is accessed, all other word and bit lines are set to GND (orange), blocking potential sneak paths.

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Fig. 5: The demonstration setup: (a) The computing-in-memory module and its interface to the digital domain with a generic crossbar (blue), (b) a 1R crossbar that can be integrated in the CIM on the left for the generic crossbar, (c) a LUT for the drivers that forbids certain voltage combinations, and (d) a 1T1R crossbar that can be integrated in the CIM module on the left. The red lines indicate exemplary leakages for a sensitive signal in the digital domain, identified by our VeriCoq-IFT setup.

The results of the VeriCoq-IFT analysis are illustrated with the red leakage paths (Fig. 5 (d)), which are the same as for the previous two hardware designs.

## VII. DISCUSSION

The VeriCoq-IFT analysis of the 1R crossbar accurately depicts the behavior of the sneak paths, so that the framework identifies possible data leakages. On the contrary, active crossbars solve the influence of sneak path currents by incorporating active components, such as transistors. As a static analysis cannot depict the difference between active and passive crossbars, the information flow did not change. Although an access mask in the control circuitry must lead to a change in the identified information flow, VeriCoq-IFT's conservative analysis is not capable of differentiating between the three designs' flows, leading to false positive identifications. Specifically, the SoC designs with a CIM module, which allows continuous information flow between the analog and digital domain, require a less conservative approach to reduce the high number

TABLE I: Rules for the allowed access masks to set or reset the crossbar at (k,l) when using a (m,n)-crossbar.

SET	RESET
$V_{WL,k} = V_{SET}$	$V_{WL,k} = V_{RES}$
$V_{SL,l} = V_{GAT}$	$V_{SL,l} = V_{GAT}$
$V_{BL,l} = GND$	$V_{BL,l} = GND$
$V_{WL,1:k-1} = GND$	$V_{WL,1:k-1} = GND$
$V_{SL,1:l-1} = GND$	$V_{SL,1:l-1} = GND$
$V_{BL,1:l-1} = GND$	$V_{BL,1:l-1} = GND$
$V_{WL,k+1:m} = GND$	$V_{WL,k+1:m} = GND$
$V_{SL,l+1:n} = GND$	$V_{SL,l+1:n} = GND$
$V_{BL,l+1:n} = GND$	$V_{BL,l+1:n} = GND$

of false positives. Less conservative approaches are already available for the digital domain [14], but are yet missing for the analog domain. The accurate frameworks consider inter-signal dependencies, the actual functionality of an operation, and the accurate value of a signal, which is not done by VeriCoq-IFT. Thus, a framework needs to be developed that considers the mentioned features in the analog by processing the information in the Verilog-A/MS description.

#### VIII. CONCLUSION

This work presented an evaluation of the state-of-theart information flow analysis framework VeriCoq-IFT for integrated CIM modules. As demonstrated, derived Verilog models could be implemented to enable an early stage IFA for trending memristor crossbars, a crucial building block for neuromorphic systems. The functionality of the mixed-signal IFA was demonstrated using three system designs. However, the conservative nature of the current analog information flow theorems leads to many false positives, which make a practical static analysis of the confidentiality property in CIM modules infeasible. In future work, the framework could be extended to allow a less conservative analysis of the information flow [14] or even a quantification of the information flow, so that negligible flows can be ignored [15], [16].

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