A Neural Recording System with 16 Reconfigurable Front-End Channels and Memristive Processing/Memory Unit

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***Abstract*—This paper proposes a neural recording system that supports recording of action potentials (APs), local field potentials (LFPs), or full-band neural signals (APs plus LFPs) by exploiting 16 reconfigurable front-end channels. To store and process the recorded signals, an off-chip 1 transistor 1 memristor (1T1R) crossbar array with optimized row/column selection logic is employed. The crossbar array is divided into four allocatable memory zones. The front-end channels are designed to filter the input signals to the bands of interest with a programmable gain of 100x or 1000x. Each front-end channel comprises an AC-coupled low-noise amplifier (LNA) which has an inherent high-pass filter (HPF), a passive first-order low-pass filter (LPF), and a variable gain amplifier (VGA). The VGA also acts as a buffer to interface with the memristor array. A reconfigurable pseudo-resistor is used to set variable high-pass corner frequencies for different recording modes. The total input-referred integrated noise of the entire channel is less than 5.6μV$_{rms}$ in the AP band (500-10kHz) and less than 4.55μV$_{rms}$ in the LFP band (1-500Hz). Implemented in a standard 180nm CMOS process, each channel occupies 0.035 mm^2 chip area and consumes 20.4μW with a 1.8V power supply. The memristor array is post-processed on the CMOS back-end-of-line (BEOL) in-house, which will be used to process and encode the channel outputs into memristive states.**

I. Introduction

Electrophysiological recordings of neuronal activities including the LFPs and APs are instrumental for studies of the nervous system, leading to a deeper understanding of brain functions which may translate to new methods and technologies to treat neurological conditions [1–4]. Furthermore, it inspires the development of next-generation AI platforms [5]. The implementation of a large-scale recording system for acquiring massive neural signals requires the front-end channels to be predominantly scalable. Most conventional platforms are based on CMOS technology and the performance is enhanced either by using more advanced technology nodes or through design optimizations throughout the circuit hierarchy [6, 7].

As CMOS technology approaches its physical limits, new technologies begin to emerge and open new opportunities for innovations in microelectronics circuits and systems design. Among these emerging technologies, the memristor has been viewed as a competitive candidate due to its non-volatility, area and power efficiency, and compatibility with CMOS technology. Distinct from conventional CMOS memory, memristors manifest a multi-state memory ability, rendering them capable of process-in-memory applications [8, 9]. By exploiting these properties, a more compact memristive memory can be implemented, improving both power and area efficiency when compared to traditional dynamic random-access memory [10]. It was demonstrated that memristors can be used to process and encode neural spikes with their intrinsic resistive switching thresholds, leading to promising designs of low-power and real-time neural signal processing systems [11, 12] and oppor-

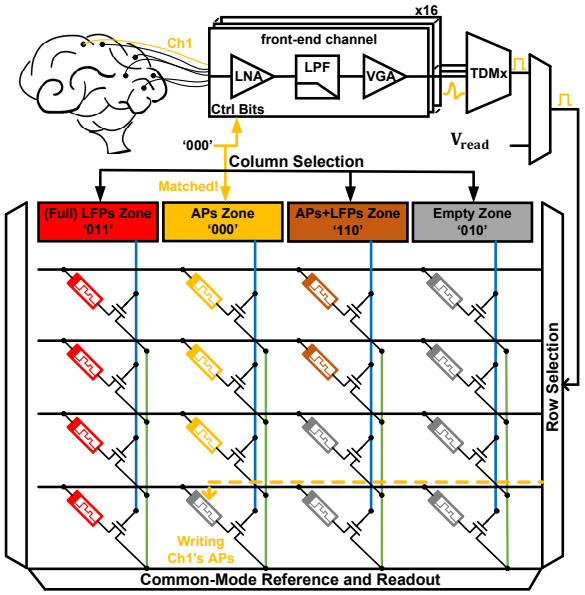

Fig. 1: The proposed neural recording system with 16 front-end channels and a 4x4 memristive processing/memory unit. This figure shows an example of the APs recording process of channel 1 (Ch1). The incoming neural signal is processed by the channel and a time-division multiplexer (TDMx), after a quick comparison between the control bits and the allocatable zone's status marker, the neural signal is then written to the allocated memristor. If all the status markers fail to match the control bits, an empty zone ('010') will be activated for the incoming neural signals. Blank memristors without any data are marked grey in the figure.

tunities to interface biological neurons with artificial spiking neural networks [13, 14]. However, the previous studies were all based on pre-recorded neural datasets and relied on pre-processing in software. In this paper, we present the design of a compact, low-power, and low-noise multichannel neural recording front-end which is essential for interfacing the memristors with neurons in vitro or in vivo, and apply the design in the Memristive Integrating System (MIS) to conduct the real-time recording of the neural signals [15]. In our proposed architecture, an off-chip memristor array, which functions as a processing/memory unit, is categorized into 4 allocatable memory zones to record mixed neural signals. The proposed front-end channel can be reconfigured to achieve multi-mode recording characteristics.

The rest of the paper is organized as follows: Section II introduces the methodology of the proposed neural recording system. Section III presents the circuit-level design of the front-end channel. Section IV shows the simulation results and the layout of the reconfigurable front-end channel. Section V concludes the paper and envisages future work.

II. Memristive Neural Recording System

A. Mixed Neural Signals Recording Logic

By leveraging 16 reconfigurable front-end channels and a memristor crossbar array, a neural recording system capable of recording mixed neural signals simultaneously is implemented as shown in Figure 1. The neural signals are first processed by the 16 channels and then serialized by a time-division multiplexer (TDMx) with a clock rate of 320kHz (20kHz Nyquist sampling rate for each channel). The sampled neural signals are then fed to write the corresponding memristors through row/column selection logic. Neural data stored in the memristive processing/memory unit can be read through circuitry which comprises transimpedance amplifiers (TIAs) and analog-to-digital converters (ADCs) [10].

The mixed neural signals recording is achieved by selecting columns in Figure 1 dynamically. In this design, 3 control bits are used to select the recording mode of the front-end channels. Every 4 channels share the same set of control bits and thus operate in the same recording mode. A 4x4 memristive array is divided into 4 allocatable memory zones, and each zone is assigned a 3-bit status marker reflecting its current states. The encoding logic is correlated to the control bits assignment of the reconfigurable front-end channel, and the correspondence of each status will be discussed in Section II-B. The status markers are compared with the control bits when allocating a memristor to be written. An example of an in-progress recording (highlighted in yellow) is demonstrated in Figure 1. Recorded APs at Channel 1 (Ch1) are serialized and sampled by the TDMx, whilst the system matches the control bits with the status marker ('000') to locate the corresponding zone, and then the sampled APs are fed to write the allocated memristor. Apart from mixed-mode recording, the system can still be configured to record pure APs, LFPs or full-band neural signals by programming all the channels with the same control bits, which further extends the applicability of the system.

Figure 2 shows the off-chip one transistor one memristor (1T1R) crossbar array adopted in the design to be used as the processing/memory unit. In this 1T1R array, memristors are applied onto a CMOS chip for monolithic integration. The interface logic between the front-end chip and the crossbar array will be implemented using a dedicated instrumentation platform which was developed in house for memristor array interfacing [16].

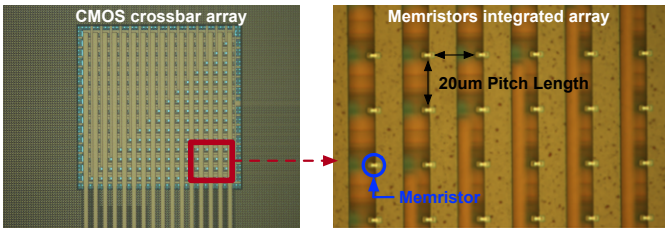

Fig. 2: 1 transistor 1 memristor crossbar array. The memristors are laid on the top of a CMOS crossbar array

B. Reconfigurable Front-End Channel

3 control bits are used to configure the channel's operating mode, details of the control logic are shown in table I, this is correlated to the status markers shown in table II. Since the 1000x gain is disabled when amplifying LFPs, the corresponding states '011' and '010' are used to indicate full and empty status respectively.

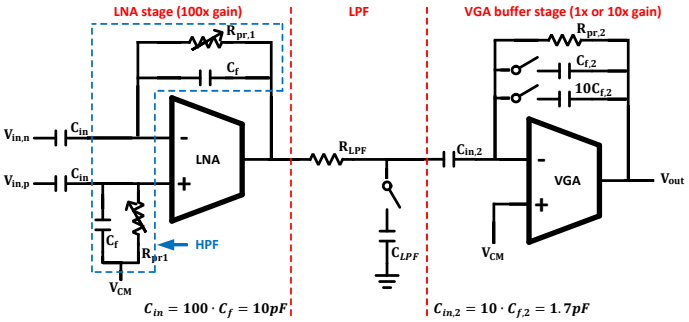

Fig. 3: Schematic of the front-end channel. From left to right is the LNA stage with the HPF, first-order RC LPF, and the VGA buffer stage.

TABLE I: Reconfigurable Front-end Channel Controlling Logic

Control Bit	Logic 1	Logic 0
Gain (2nd Digit)	100x overall gain	1000x overall gain
HPF (1st Digit)	1Hz high pass corner frequency	500Hz high pass corner frequency
LPF (0th Digit)	500Hz low pass corner frequency	10kHz low pass corner frequency

TABLE II: Status Markers of the Allocatable Zone

3-bit status marker	Zone Status
010	Empty
011	Full
000	APs
110	LFPs+APs
111	LFPs

The channel shown in Figure 3 comprises three modules: an LNA with the high-pass filtering function, a first-order RC LPF, and a VGA which also acts as a buffer. The LNA has a 100x constant gain, the reconfigurable pseudo-resistor $R_{pr,1}$ along with C_f provides a selectable 1Hz or 500Hz high-pass corner frequency, and the RC filter provides a 500Hz or 10kHz low-pass corner frequency. The VGA buffers the signals with a programamble 1x or 10x gain. For LFP recording, code '111' is loaded to the control bits and the channel filters the signal to the 1-500Hz bandwidth with a 100x gain; for AP recording, code '000' is used to filter the signal to the 500-10kHz bandwidth with a 1000x gain; for both APs and LFPs recording, code '110' is used to select the 1-10kHz signal bandwidth with a 100x gain. The channel also provides a quick transition feature for mode-to-mode switching with only a maximum reset period of 1ms, rendering the channel able to switch operating modes in real-time.

III. Front-End Channel Circuit-level Design

A. Operational Transconductance Amplifiers

Two operational transconductance amplifiers (OTAs) are designed for the LNA and the VGA respectively, and their schematics are shown in Figure 4 (a) and (b). C_{in} in Figure 3 is chosen to be 10pF as a result of tradeoff between input impedance and shaping of the noise from the pseudo resistors. As shown in Figure 4 (a), source degenerated current mirrors are adopted to suppress the flicker noise of M_3 and M_4, I_{d1} is scaled to 10 times of $I_{d9,10}$ to reduce $g_{m9,10}$. Currents are all biased to sub-200nA except for the input branches to minimize power consumption. Noise contributed by the LPF and VGA are neglected since they are attenuated by the 100x LNA gain when referred at the channel input. The VGA designed in Figure 4 (b) adopts a similar topology to the LNA, while a translinear loop class-AB output stage is used to achieve faster settling, and thereby the 16 channels' output can be multiplexed and sampled to improve the write speed of the memristive memory and also the channel's resistive loads driving capability. To compensate the additional pole incurred by the class-AB stage, indirect compensation is exploited to emerge a left-hand plane zero, leading to better unity gain frequency at more than 1MHz [17].

B. High-Pass Filter with Reconfigurable Pseudo-Resistor

A dual-resistance reconfigurable pseudo-resistor topology in Figure 5 is proposed to provide two configurable resistances. Both resistors are implemented with a back-to-back structure to achieve less variations [18, 19]. 2-volt and 5-volt PMOS devices are used to provide 3GΩ and 2TΩ equivalent resistance, forming a 500Hz and a 1Hz high-pass corner frequency respectively.

IV. Simulation Results

The proposed reconfigurable front-end channel is designed using a 180nm CMOS BCD process. Figure 6 shows the transient simulation result of the channel operating in different modes. The channel is tested with a two-tone input signal

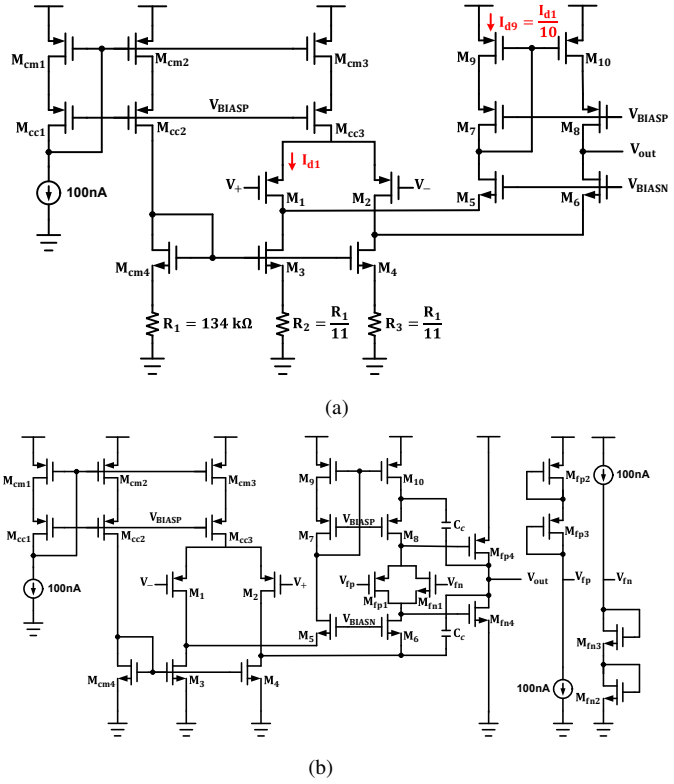

Fig. 4: (a) LNA schematic. (b) VGA schematic.

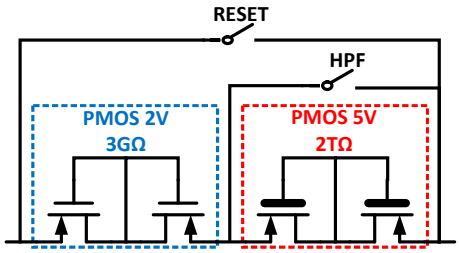

Fig. 5: Dual-resistance reconfigurable pseudo-resistor schematic.

combining a 100Hz, 6mV$_{pp}$ sin-wave representing the LFPs, and a 2kHz, 200μV$_{pp}$ sin-wave representing the APs. A 1ms reset is applied during the power-on phase, and the channel starts to record both LFPs and APs with a 100x gain. The channel is then switched to LFPs recording mode with another 1ms reset period, such that only the low-frequency component remains. In the final phase, the channel enters the APs recording mode and amplifies the high-frequency signals with a 1000x gain, part of the low-frequency signal remains due to the limitation of the first-order high-pass filtering. As shown in Table III, the noise performance of the front-end channel is better than the established neural recording technologies that have been widely used in the neuroscience community [1, 2], which proves the feasibility of the design for the target application.

The design is applicable for the Memristive Integrating System (MIS) reported in [11]. The basic MIS concept states

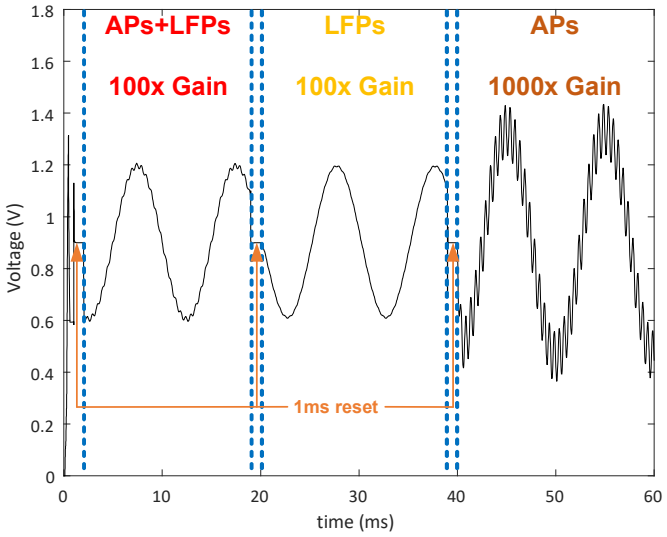

Fig. 6: Front-end channel transient simulation results. By changing the control bits, the channel switches between APs plus LFPs recording mode, LFPs recording mode, and APs recording mode. A 1ms reset period is required for mode switching and power-on initialization.

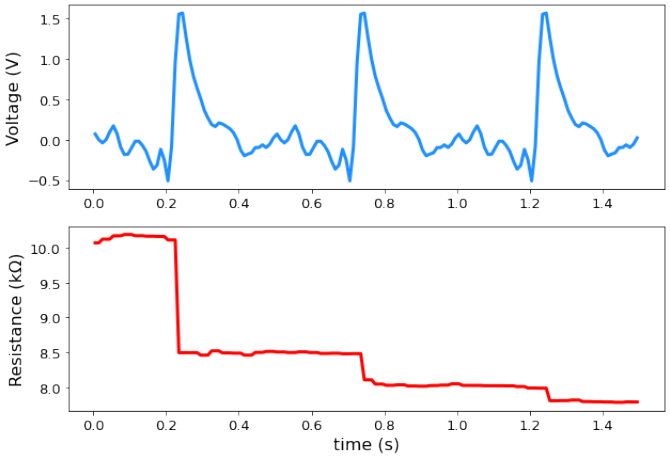

Fig. 7: MIS concept: Neural spikes present in an electrophysiological trace (top panel) cause non-volatile resistive state transitions in a memristive device's resistive state (bottom trace) whilst noise leaves it unaffected.

that waveforms containing appropriately high magnitude voltage spikes can cause a resistive state displacement in a non-volatile memristive device, whilst lower magnitude noise will have no similar effect. Figure 7 presents a direct result of the thresholded resistive switching phenomenon observed in many memristive devices. In the original work [11], it was made clear that signals being processed by the MIS must match the memristive device's voltage characteristics (most notably its practical switching threshold), which would require reasonably high-fidelity pre-amplification. This is precisely what the proposed front-end channel seeks to present. As shown in TABLE III and Figure 6, the proposed design can cover the base specifications required by a neural front-end for MIS in terms of amplification factor and output swing (that is: approx. 1V output swing and the ability to amplify a signal of

TABLE III: Performance of the Proposed Front-end Channel

Parameter	Post Layout Simulation result
Mid Band Gain	39.5dB 59.56dB
Input-Referred Noise	6.88μV$_{rms}$ (Full Band) 4.55μV$_{rms}$ (LFP) 5.6μV$_{rms}$ (AP)
DC Power Consumption	20.34μW
Bandwidth	0.388Hz-10.63kHz (Full Band) 0.388Hz-556Hz (LFP) 571Hz-10.93kHz (AP)
Maximum Signal Amplitude (1% THD)	8mV$_{pp}$
Maximum Signal Output Swing	1V (out of 1.8V)
CMRR (50Hz)	>67dB
PSRR (In Band)	>71dB
Phase Margin	>68 °
Area (per channel)	0.035 mm^2

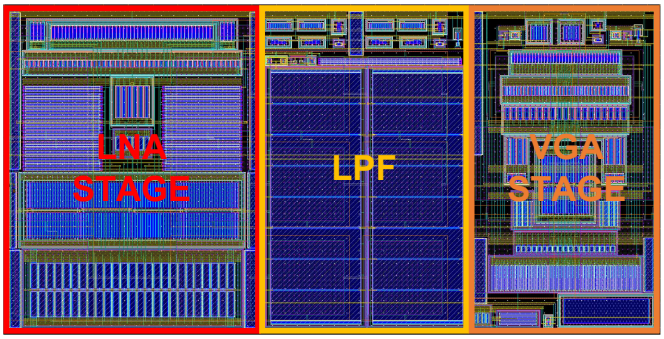

Fig. 8: layout of the reconfigurable front-end channel.

a few mV to 500mV, which is sufficient for certain implants).

The layout of a single front-end channel is shown in figure 8, it occupies 0.035 mm^2 chip area. Table III shows the post-layout simulation results of the front-end channel.

V. Conclusion and Future Work

In this paper, we propose a neural recording system to record mixed neural signals with 16 reconfigurable front-end channels including a memristive processing/memory unit. Thanks to the mixed recording characteristic, the system can not only handle the single-type neural signals recording as per a conventional recording system but can also store mixed neural signals into an off-chip memristor crossbar array. Besides, the proposed work will facilitate applying MIS for neural signal processing *in vivo* at much larger scale, which is our next step once the front-end chip is fabricated and tested with the memristor crossbar array.

VI. Acknowledgement

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References

[1] J. J. Jun *et al.*, "Fully integrated silicon probes for high-density recording of neural activity," *Nature*, vol. 551, no. 7679, pp. 232–236, 2017.

[2] N. A. Steinmetz *et al.*, "Neuropixels 2.0: A miniaturized high-density probe for stable, long-term brain recordings," *Science*, vol. 372, no. 6539, p. eabf4588, 2021.

[3] A. H. Shoeb and J. V. Guttag, "Application of machine learning to epileptic seizure detection," in *International Conference on Machine Learning*, 2010.

[4] S. M. Yao L, Brown P, "Improved detection of parkinsonian resting tremor with feature engineering and kalman filtering," *Clin. Neurophysiol*, vol. 131, no. 1, pp. 274–284, 2020.

[5] J. Stuijt, M. Sifalakis, A. Yousefzadeh, and F. Corradi, "brain: An event-driven and fully synthesizable architecture for spiking neural networks," *Frontiers in Neuroscience*, vol. 15, 05 2021.

[6] X. Yang *et al.*, "An ac-coupled 1st-order - readout ic for area-efficient neural signal acquisition," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 4, pp. 949–960, 2023.

[7] U. Shin *et al.*, "Neuraltree: A 256-channel 0.227-j/class versatile neural activity classification and closed-loop neuromodulation soc," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 11, pp. 3243–3257, 2022.

[8] S. Stathopoulos *et al.*, "Multibit memory operation of metal-oxide bi-layer memristors," *Scientific reports*, vol. 7, no. 1, pp. 1–7, 2017.

[9] C. Wang *et al.*, "Multi-state memristors and their applications: An overview," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 12, no. 4, pp. 723–734, 2022.

[10] C. Wang, L. Xie, X. Jiang, R. Ge, and C. Papavassiliou, "Design of a multi-state memristive memory," in *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2021, pp. 1–6.

[11] I. Gupta, S. Alexantrou, A. Khiat, R. Zeitler, S. Vassanelli, and T. Prodromakis, "Real-time encoding and compression of neuronal spikes by metal-oxide memristors," *Nature Communications*, vol. 7, 2016.

[12] Z. Liu *et al.*, "Multichannel parallel processing of neural signals in memristor arrays," *Science Advances*, vol. 6, no. 41, p. eabc4797, 2020. [Online]. Available: https://www.science.org/doi/abs/10.1126/sciadv.abc4797

[13] A. Serb *et al.*, "Memristive synapses connect brain and silicon spiking neurons," *Scientific Reports*, vol. 10, 02 2020.

[14] Y. He *et al.*, "An implantable neuromorphic sensing system featuring near-sensor computation and send-on-delta transmission for wireless neural sensing of peripheral nerves," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 3058–3070, 2022.

[15] I. Gupta, A. Serb, A. Khiat, R. Zeitler, S. Vassanelli, and T. Prodromakis, "Sub 100 nw volatile nano-metal-oxide memristor as synaptic-like encoder of neuronal spikes," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 2, pp. 351–359, 2018.

[16] P. Foster, J. Huang, A. Serb, S. Stathopoulos, C. Papavassiliou, and T. Prodromakis, "An fpga-based system for generalised electron devices testing," *Scientific Reports*, vol. 12, no. 1, p. 13912, 2022. [Online]. Available: https://doi.org/10.1038/s41598-022-18100-3

[17] R. Hogervorst, J. Tero, R. Eschauzier, and J. Huijsing, "A compact power-efficient 3 v cmos rail-to-rail input/output operational amplifier for vlsi cell libraries," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, 1994.

[18] E. Guglielmi *et al.*, "High-value tunable pseudo-resistors design," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2094–2105, 2020.

[19] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad, and A. M. Sodagar, "Analysis and design of tunable amplifiers for implantable neural recording applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 4, pp. 546–556, 2011.