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***Abstract*—With the shrinkage of process nodes for integrated circuits, analog circuits, like analog feedback control, have become increasingly expensive and more challenging to design. Here time-based control is a compelling alternative to traditional analog feedback control circuits due to its better scaling with the process node. Several publications about time-based PID-type controllers exist. There the PI-part is implemented in the time domain, but the D-part remains in the analog domain thereby limiting the process scaling benefits. This paper proposes a new PID structure that fully integrates the PID in the time domain. The proposed structure has improved ripple attenuation and maps directly to a typical PID. Simulations shows that the performance of the theoretical small signal controller translates well to the large signal time-based response.**

I. Introduction

In recent years, there has been an increasing interest in the emerging topic of time-based (TB) circuits and systems [1–3]. Unlike analog circuits, time-based circuits use time as the operating variable, not voltages and currents. They use controlled oscillators and delay lines to generate a phase difference between a reference and a feedback path which is compared in a phase detector (PD) to generate a PWM signal. Since time-based circuits do not need large resistors and capacitors, they are more suitable for integrated circuits as they scale better with process nodes. Integrated time-based circuits have already proved their functionality in many applications, such as Op-Amps [4–6] and time-based filter [7–10].

Another application for time-based systems are time-based control, that has been used for integrated Buck and Boost power converters where PI and PID controllers have been designed [11–18]. These controllers generate the proportional and integral gain in the time-based domain using current controlled delay lines (CCDL) for proportional gain and current controlled oscillators (CCO) as integrators. However, the derivative gain is generated outside of the time-based domain using a conventional RC highpass filter. Fig. 1 shows a typical time-based PID controller in a buck converter similar to the implementations in [11, 14–18].

This paper proposes a new time-based PID structure that utilizes the operating variable, time, in the form of a delay as an additional control parameter. By doing so, we can derive a time-based derivative action. Thus, integrating the entire

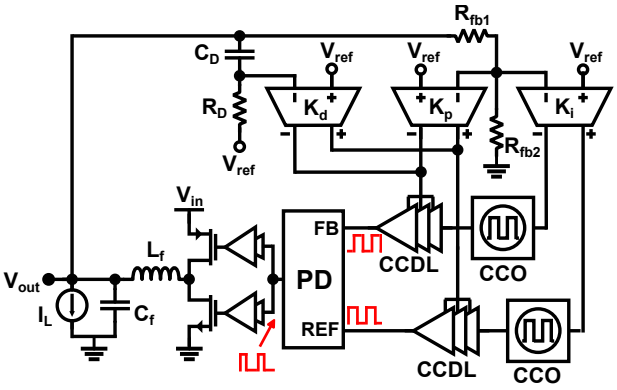


Fig. 1. Typical structure of a TB-PID controller with a buck converter.

PID controller into the time-based domain. We show that the derived controller has a simple mapping to a typical PID controller and that the derivative term can be made insensitive to the output ripple of the controlled system.

The rest of the paper is structured as follows. Section II presents the ideas behind the fully time-based PID controller and analyses the controller from a theoretical standpoint. Section III maps the proposed controller to the typical PID controller and covers the similarities and differences between the two. In section IV we look at the practical implementation of the proposed controller and the limitations it imposes. Finally, simulations of the time-based controller in closed-loop with a Buck converter are performed to verify its performance. The paper finishes with a conclusion.

II. Fully Time-Based PID

In time-based control, as it name suggest, the operating variable is time. This is seen in the use of variable delay lines as proportional gains, where the control gain adds more or less delay to the pulse train to get the desired phase shift. Hence introducing time delays to the control system is an inherent part of time-based control. Contrary to common belief, time delays in dynamical systems are not always detrimental to stability and performance. Several studies [19–23] have shown that time delays can be actively used in controllers to stabilize a system or approximate certain operations. One well-known example is the finite difference approximation in (1).

$$\frac{d}{dt}f(t) \approx \frac{f(t) - f(t-h)}{h} \tag{1}$$

Here, h is some known time delay applied to the function $f(t)$ that, together with the function value at the current time, is used to approximate the derivative. Since (1) relies purely on a time delay for its operation, it can be implemented in a time-based context. To show this, we consider a PD controller (2) that uses a finite difference as its derivative.

$$H(t) = f(t)K_p + \frac{f(t) - f(t-h)}{h}K_d \tag{2}$$

K_p is the proportional gain and K_d is the derivative gain. By collecting the terms that are related to the same time instance we find:

$$H(t) = f(t)\left(K_p + \frac{K_d}{h}\right) - f(t-h)\frac{K_d}{h} \tag{3}$$

Next, the control gains K_p and K_d are substituted with (4) and (5) and the controller is moved into the Laplace domain to get (6).

$$K_p = K_1 - K_2 \tag{4}$$

$$K_d = K_2 h \tag{5}$$

$$\mathcal{L}\{H(t)\} = H(s) = F(s)\left(K_1 - e^{-hs}K_2\right) \tag{6}$$

Equation 6 has two gains with $K_1 > K_2$. K_1 is an instantaneous gain that provides a large initial change to transients. Likewise, K_2 act as a compensation gain that counteracts the large gain of K_1 after the set time h. To see this and to recover the original gains, the limits of (6) are derived for steady state in (7) and infinite frequencies in (8).

$$\lim_{s\to 0} H(s) = F(s)\left(K_1 - K_2\right) = F(s)K_p \tag{7}$$

$$\lim_{s\to \infty} H(s) = F(s)K_1 = F(s)\left(K_p + \frac{K_d}{h}\right) \tag{8}$$

$$\tag{9}$$

As expected, we find that only K_p is active in steady state and that both K_p and K_d is active during transients. Finally, the integral action is added to the controller to form the controller in (10).

$$C_{PIR}(s) = K_1 - K_2 e^{-hs} + \frac{K_i}{s} \tag{10}$$

The structure in (10) is convenient for a time-based implementation compared to (2) because the controller gains are partitioned by their corresponding time delay. This will become evident in section IV.

This type of PID controller, where one of the control signals is delayed, is also referred to as Proportional-Integral-Retarded (PIR) controller [20–22], where the retarded refers to the fact that the controller forms a retarded delay type system. We will use the PIR notion for the rest of this paper to differentiate between our proposed controller and the typical PID controller

III. PID Mapping

It is of interest to know how the proposed controller in (10) maps to a typical PID controller since it enables a design through conventional design methods. The analysis in section II found that the proportional and integral gain has a simple mapping from the PIR controller to the PID controller. However, since an approximation of the derivative in the form of a finite difference is used in the PIR controller, the mapping to the derivative term in the PID controller needs to be investigated. Equation (11) shows the derivative term from (2) and its laplace transform.

$$H_D(s) = \mathcal{L}\left\{\frac{f(t) - f(t-h)}{h}K_d\right\} = F(s)\frac{K_d}{h}\left(1 - e^{-hs}\right) \tag{11}$$

To eliminate the time delay and get (11) to a form more close to $K_d s$, the time delay is approximated with a first order Padé approximation (12).

$$e^{-hs} \approx \frac{1 - 0.5hs}{1 + 0.5hs} \tag{12}$$

The Padé approximation creates an all pass filter with a 180 degree phase shift. The placement of this phase shift aligns with the phase shift due to the time delay. By replacing the delay in (11) with (12) the transfer function in (13) is obtained.

$$H_D(s) = F(s)\frac{K_d s}{1 + 0.5hs} \tag{13}$$

The transfer function in (13) is identical to the lead-compensation term, which is often preferred in PID controllers. The lead compensation is usually more practical since it does not need the true derivative and is less noise sensitive due to its finite gain at high frequencies. Hence the proposed PIR controller has a mapping to the practical PID controller shown in (14).

$$C_{PID}(s) = K_p + \frac{K_i}{s} + \frac{K_d s}{\tau s + 1} \tag{14}$$

A complete mapping between all the control gains for the proposed PIR controller in (10) and the PID controller in (14) is shown in Table I.

TABLE I
MAPPING BETWEEN TYPICAL PID GAINS AND THE PROPOSED PIR.

PID Gains	TB-PIR Gains
K_p	$K_1 - K_2$
K_i	K_i
K_d	$K_2 h$
τ	$h/2$

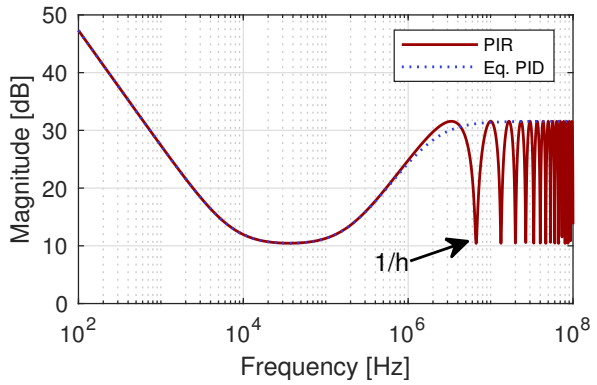


Fig. 2. Comparison of the frequency response for the PID controller and the PIR controller using the mapping in Table I. The used controller values are identical to the values in Table III with the exception of K_i which is 10 times smaller.

Fig. 2 shows the frequency response for the PIR controller and the mapped equivalent PID controller. At low frequencies, the PIR and PID behaves identically. However, at high frequencies, when the PID reach a plateau, the PIR controller exhibits a comb filter response due to the time delay h with notches at every integer multiple of h^{-1}. These notches have the benefit of reducing noise sensitivity at high frequencies. Furthermore, suppose the delay is tuned to be the switching period ($h = f_{sw}^{-1}$). In that case, the derivative term will attenuate ripple going into the controller, thereby reducing the problem of the derivative action amplifying the switching harmonics.

IV. Practical Implementation

So far, section II and III have looked at the PIR controller's theoretical aspects. This section will cover how the PIR controller is implemented in the time-based control framework. Fig. 3 shows the implementation of the PIR controller in the time domain. The implementation has many similarities with the PID implementation in Fig. 1 used in the prior arts. Like with the PID implementation, the reference and feedback voltage enters an OTA for each control gain. The OTA outputs a differential current that controls the frequency of the CCOs in the case of the integrator and the delay of the CCDLs for proportional gains. The control gains $K_{1,2}$ is distributed across the OTA and the CCDL, resulting in the relation $K_{1,2} = 2K_{OTA}K_{CCDL}f_{sw}$. The same is the case for K_i, but instead of $K_{CCDL}f_{sw}$, K_{CCO} is used. The factor of two in both cases is due to the gain being split evenly between the reference and feedback path in the controller. Unlike the PID controller, the PIR controller has no K_D path, but an additional pair of CCDLs with a corresponding OTA to provide a path for K_1. A SDL is placed between the CCDLs for K_1 and K_2 to provide the delay h needed for the controller.

Each of the CCDLs has its own intrinsic delay (φ) due to biasing that will be passed on to blocks down the signal chain. This will impact the controller performance as it will increase the desired delay h to $h+\varphi_1$. Moreover, the integrator (CCOs) will have its signal delayed by all the delay elements. Equation

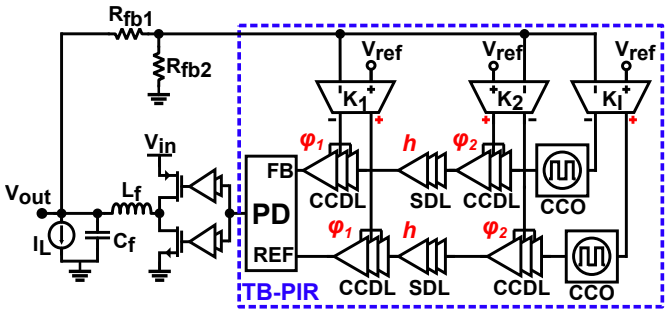


Fig. 3. Circuit diagram of the proposed TB-PIR controller combined with the buck converter used for simulation.

(15) shows the updated controller transfer function accounting for the added delays due to the implementation.

$$C_{TB-PIR} = \frac{K_i}{s}e^{-(h+\varphi_1+\varphi_2)s} - K_2 e^{-(h+\varphi_1)s} + K_1 \quad (15)$$

To counteract the implementation delays, h can be reduced to partly or completely remove the effect of φ_1 on K_2. While this will also reduce φ_1's contribution to the unwanted delay on the integrator, the integrator will still be impacted by the delay $h + \varphi_2$. However, because integration is an operation that dominates at low frequencies, the additional delay will have a limited impact since it's phase-shift is only significant at high frequencies.

V. Simulation Results

A. Simulation Model

The proposed implementation of the time-based controller in section IV is created using Verilog-A in Cadence Virtuoso together with a buck converter to verify the performance. Fig. 3 shows the structure of the circuit. The time-based controller outputs its control signal as a PWM signal that is used to drive the gate driver of the buck converter. Table II shows the specifications and component values for the buck converter.

TABLE II
Components and Specifications for the Buck Converter.

Specifications	Value	Components	Values
V_{in}	1.8 V	L_f	220 nF
V_{out}	1.0 V	R_{L_f}	120 mΩ
I_L	100 mA	C_f	4.7 µF
f_{sw}	20 MHz		

The component values leads to an underdamped response with a damping of $\zeta = 0.28$ and a cutoff frequency of $f_c = 157$ kHz. The PIR controller is designed to ensure approximately 60° degree of phase margin while minimizing the disturbance for a load step. Lastly, the feedback network R_{fb1} and R_{fb2} is designed to provide an attenuation of V_{in}^{-1}. Besides the PIR, an equivalent PID controller is made for comparison using the parameters for the PIR and the mapping in Table I. Table III shows all the controller gains for both

TABLE III
CONTROLLER GAINS FOR THE PIR CONTROLLER AND THE EQUIVALENT PID CONTROLLER.

PID	Value	Unit	PIR	Value	Unit
K_p	3.32		K_1	20.60	
K_i	1.46	M	K_i	1.46	M
K_d	2.59	µ	K_2	17.28	
τ	74.85	ns	h	149.70	ns
			$\hat{h}$	63.90	ns

controllers. The delay through each of the CCDLs are estimated based on the value of K_1 and K_2 to be $\varphi_1 = 85.8\,\text{ns}$ and $\varphi_2 = 72.0\,\text{ns}$. Since $\varphi_1 < h$, the effect of φ_1 can be completely compensated by using the delay $\hat{h} = h - \varphi_1$ in the SDL. φ_2 cannot be compensated but as it only impacts the integrator, the resulting performance degradation is negligible. Finally, the delay h is tuned in such a way that the comb filter aligns with f_{sw} and its harmonics.

B. Results

Fig. 4 shows the bode plot for the simulated large signal closed-loop buck converter along with the small signal response for the PIR and the equivalent PID using (15) and (14) respectively. Lastly, the frequency response of the buck converter without any control is also shown. We find no noticeable difference between the simulated response and the small signal PIR, and the first notch of the comb filter at $h^{-1} = 6.7\,\text{MHz}$ is seen in both cases. The equivalent PID controller follows a similar response up until the notch which, as expected, is not present.

Fig. 5 shows the output voltage and the duty cycle when the load I_L is step from 0 A to 100 mA at time 0. Both the simulation and the small signal PIR and PID shows nearly identical response in both the output voltage and the duty cycle i.e. the control signal. Looking at the duty cycle, a steep initial transient is observed, showing the derivative action that multiplies the error by K_1.

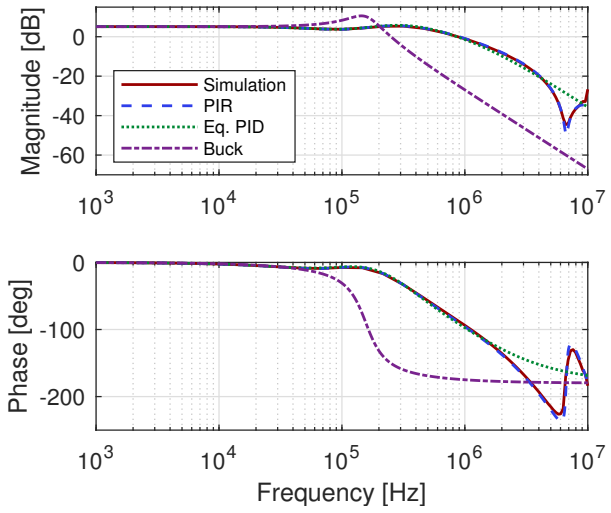
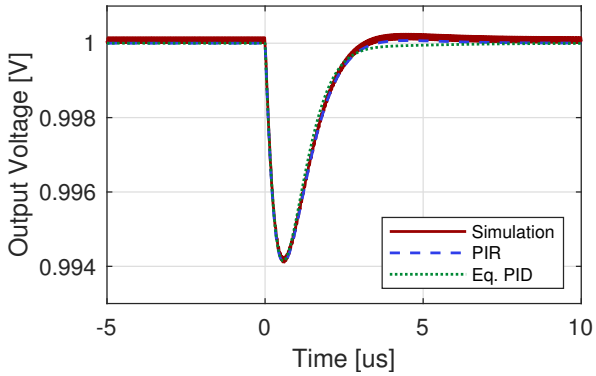
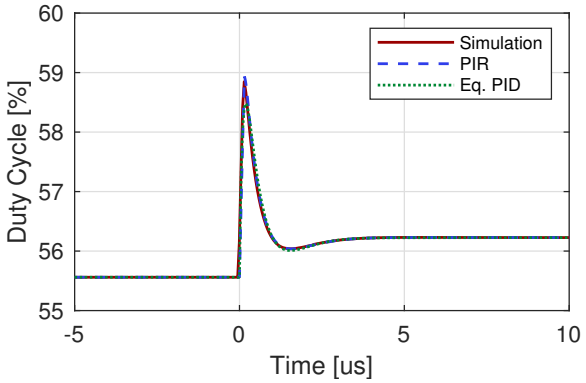


Fig. 4. Simulated large signal response and small signal response from V_{ref} to V_{out} for the circuit in Fig. 3. The response 'Buck' is the dc/dc converter without any control.



(a) Output Voltage



(b) Duty Cycle

Fig. 5. Response for a load step when the load I_L is step from 0 A to 100 mA at time 0. (a) shows the output voltage V_{out} and (b) show the duty cycle from the output of the PD.

VI. CONCLUSION

This paper has proposed a new PID structure for time-based control that integrates the derivative into the time-based domain. By integrating the derivative, a passive RC highpass filter used in the prior art can be omitted, leading to smaller footprints that scales better with the process node. The derivative was designed using a finite difference inspired approach that utilizes the operating variable, time, in the time-based domain to construct an approximate derivative. We showed that the proposed controller directly maps to a typical PID controller, allowing existing control design methods to be reused. Furthermore, the proposed controller exhibited a comb filter behavior at high frequencies that, through appropriate tuning, can be used for output ripple attenuation in the controller. Simulations of the time-based controller with a buck converter followed the behavior predicted by the small signal models. To finalize, the proposed controller: allows for smaller designs with better process node scaling, maps simply to a typical PID, and provides ripple attenuation that enables better derivative performance.

REFERENCES

[1] J.-G. Kang, K. Kim, and C. Yoo, "Time-domain analog signal processing techniques," *Journal of Semiconductor Engineering*, vol. 1, no. 2, pp. 64–73, 2020.

[2] P. R. Kinget, "Scaling analog circuits into deep nanoscale cmos: Obstacles and ways to overcome them," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–8, IEEE, 2015.

[3] Q. A. Khan, S.-J. Kim, and P. K. Hanumolu, "Time-based pwm controller for fully integrated high speed switching dc-dc converters—an alternative to conventional analog and digital controllers," in *2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID)*, pp. 226–231, IEEE, 2018.

[4] K. Kim and C. Yoo, "Time-domain operational amplifier with voltage-controlled oscillator and its application to active-rc analog filter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 3, pp. 415–419, 2019.

[5] B. Vigraham, J. Kuppambatti, and P. R. Kinget, "Switched-mode operational amplifiers and their application to continuous-time filters in nanoscale cmos," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2758–2772, 2014.

[6] Q. A. Khan, S. Saxena, and A. Santra, "Area and current efficient capacitor-less low drop-out regulator using time-based error amplifier," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, IEEE, 2018.

[7] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog filter design using ring oscillator integrators," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, 2012.

[8] H. Osman and E. S.-S. Life, "A pvt-resilient, highly-linear fifth-order ring-oscillator-based filter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4295–4308, 2020.

[9] B. Salz, M. Talegaonkar, G. Shu, A. Elmallah, R. Nandwana, B. Sahoo, and P. K. Hanumolu, "A 0.7 v time-based inductor for fully integrated low bandwidth filter applications," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, IEEE, 2017.

[10] L. B. Leene and T. G. Constandinou, "Time domain processing techniques using ring oscillator-based filter structures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 12, pp. 3003–3012, 2017.

[11] P. Melillo, A. Dago, A. Gasparini, S. Levantino, and M. Ghioni, "A novel feedforward technique for improved line transient in time-based-controlled boost converters," in *2022 17th Conference on Ph. D Research in Microelectronics and Electronics (PRIME)*, pp. 257–260, IEEE, 2022.

[12] C. Lim, D. Mandal, B. Bakkaloglu, and S. Kiaei, "Switching battery charger with cascaded two loop control using time-based techniques," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1991–1995, IEEE, 2021.

[13] J.-G. Kang, J. Park, M.-G. Jeong, and C. Yoo, "A time-domain-controlled current-mode buck converter with wide output voltage range," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 865–873, 2018.

[14] S. J. Kim, Q. Khan, M. Talegaonkar, A. Elshazly, A. Rao, N. Griesert, G. Winter, W. McIntyre, and P. K. Hanumolu, "High frequency buck converter design using time-based control techniques," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 990–1001, 2015.

[15] M. Leoncini, A. Bertolini, A. Gasparini, S. Levantino, and M. Ghioni, "An 800-ma time-based boost converter in 0.18 μm bcd with right-half-plane zero elimination and 96% power efficiency," in *ESSCIRC 2021-IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, pp. 223–226, IEEE, 2021.

[16] T. Rosa, M. Leoncini, and S. L. M. Ghioni, "A novel start-up technique for time-based boost converters with seamless pfm/pwm transition," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, IEEE, 2020.

[17] S. J. Kim, W.-S. Choi, R. Pilawa-Podgurski, and P. K. Hanumolu, "A 10-mhz 2–800-ma 0.5–1.5-v 90% peak efficiency time-based buck converter with seamless transition between pwm/pfm modes," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 814–824, 2017.

[18] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. Pilawa-Podgurski, and P. K. Hanumolu, "A 4-phase 30–70 mhz switching frequency buck converter using a time-based compensator," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2814–2824, 2015.

[19] R. Sipahi, S.-I. Niculescu, C. T. Abdallah, W. Michiels, and K. Gu, "Stability and stabilization of systems with time delay," *IEEE Control Systems Magazine*, vol. 31, no. 1, pp. 38–65, 2011.

[20] K. López, R. Garrido, and S. Mondié, "Cascade proportional integral retarded control of servodrives," *Proceedings of the Institution of Mechanical Engineers, Part I: Journal of Systems and Control Engineering*, vol. 232, no. 6, pp. 662–671, 2018.

[21] K. López, R. Garrido, and S. Mondié, "Position control of servodrives using a cascade proportional integral retarded controller," in *2017 4th International Conference on Control, Decision and Information Technologies (CoDIT)*, pp. 0120–0125, IEEE, 2017.

[22] A. Ramirez, S. Mondié, R. Garrido, and R. Sipahi, "Design of proportional-integral-retarded (pir) controllers for second-order lti systems," *IEEE Transactions on Automatic Control*, vol. 61, no. 6, pp. 1688–1693, 2015.

[23] A. Galip Ulsoy, "Time-delayed control of siso systems for improved stability margins," *Journal of Dynamic Systems, Measurement, and Control*, vol. 137, no. 4, 2015.