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Analysis and Design of Start-up Circuits for a 48 V-12 V Switched-Capacitor Converter in a 180 nm SOI Process

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***Abstract*—In this work an analysis, design and layout of two start-up methods for high-voltage switched-capacitor converters is presented. During the converter start-up phase, the capacitors are charged from their initial voltage to their steady-state voltages. If a start-up approach is not considered, this creates undesired large currents in the power switches and chip I/Os, which can damage the chip. A $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor converter with an integrated power stage and external capacitors is designed and taped out in a $180\,\mathrm{nm}$ SOI CMOS process to demonstrate two different approaches of mitigating the start-up problem. The first approach solves the uneven capacitor charging during input ramp-up by creating a charging path from the input to the capacitors and carefully sizing the capacitors. The second approach charges the capacitors with a dedicated active pre-charging circuit and thereby ensures limited peak currents during start-up of the designed switched-capacitor converter. This first start-up method reduces the start-up peak current from $40\,\mathrm{A}$ to $6.5\,\mathrm{A}$ and the second method lowers the peak current to $3.5\,\mathrm{A}$. The designed pre-charge circuit consumes $105\,\mu\mathrm{A}$ quiescent current and has an area of $743\,\mu\mathrm{m} \times 911\,\mu\mathrm{m}$.**

I. Introduction

Switched-capacitor power converters are becoming more interesting in high-voltage and high-power applications such as in automotive and in data centers due to the lack of magnetic components [1]–[5]. This allows for a higher power density and lower weight since the inductors are usually bulky in traditional power converters. The recent advances in high-voltage semiconductor technology allows for integrating the switches and gate-drivers of the converter, allowing for a lower production cost and smaller size. One draw-back of switched-capacitor converters that is rarely considered is the issue of starting up the converter safely and consistently. When the voltage input of the converter ramps up the large capacitors are charged through undesired parasitic charging paths. This results in large peak currents going into the chip whenever these unmatched voltages are connected through low resistance integrated switches. These large peak currents can damage the bonding wires in the packaging to the integrated circuit (IC). Another issue is that by integrating the power stage resolves in a lack of measurement points to monitor these voltages, therefore precise control of these voltages during start-up is essential for a robust power converter.

Only a few research papers mention the start-up issue of switched-capacitor power converters. In the work of [6] an integrated LED driver is proposed with an input range of $80\,\mathrm{V}$-$90\,\mathrm{V}$ with a single IC. The LED driver is a hybrid resonant switched-capacitor converter also facing some start-up challenges. The start-up solution proposed in [6] is interesting but specific for the topology presented since it is using the gate-drivers to charge the capacitor nodes. In [7] a soft start-up is achieved in a buck converter. This is achieved with integrated power-switches and gate-drivers with additional control signals for only turning on a small part of the switch. This means that the large switch resistance will decrease the large peak current until the output capacitor is charged to the desired level. This solution is interesting because it utilizes the large switches and otherwise only rely on small digital circuitry. The complexity of the solution presented in [7] does however increase since more switches has to be controlled in different voltage domains. This requires an additional level-shifting for each start-up signal and could, dependent on the implementation, take up significant area on-chip.

This paper investigates the challenges of start-up in high-voltage switched-capacitor power converters with integrated switches. To showcase the analysis and explanation of proposed start-up solutions this work is based around a $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor converter implemented as a ladder topology, which has been designed in a $180\,\mathrm{nm}$ SOI process and sent to fabrication. The power converter is designed for a peak efficiency of $92.5\,\%$ at an output power of $12\,\mathrm{W}$. In this topology the challenges of start-up is eminent since large capacitors are connected in parallel in every switching-phase.

This paper is structured as follows: Section II gives an expanded analysis on the challenges of start-up in a high-voltage switched-capacitor converter and shows two possible start-up solutions: an passive and active implementation. Section III shows simulation results of the two start-up solutions. Section IV discusses these simulation results and compared these to previous research. The implications and applications of the two solutions are also discussed. Section V mentions the future work. The integrated circuit has been taped-out in April 2021 and is expected to return December 2021. Section VI concludes the work presented in the paper.

II. Analysis of start-up in Ladder switched-capacitor converter

In Fig. 1 the $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor ladder converter can be seen. Here the switches M_1, M_3, M_5 and M_7 are turned on during phase 1 and M_2, M_4, M_6 and M_8 are turned

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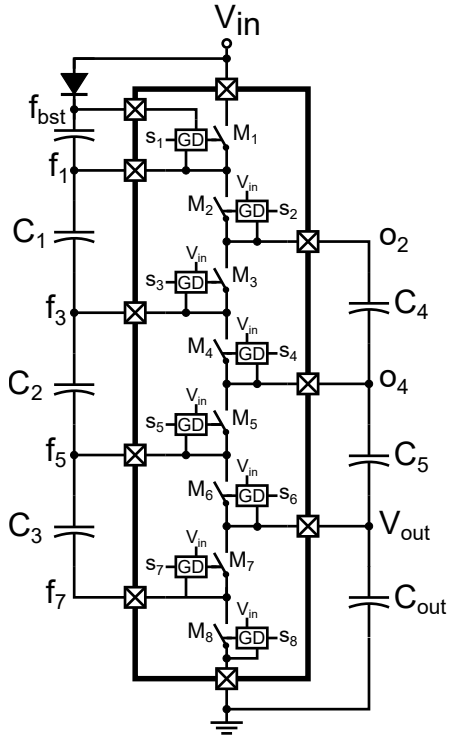

Fig. 1: 4:1 switched-capacitor converter implemented with a ladder topology with the gate-drivers (GD) references to the power converter input.

on during phase 2. The switches are turned on by gate-drivers which are all supplied from the converter input. The connection of the gate-drivers to the power converter input voltage means that the switches can be turned on as the input voltage is ramping up. It does however also mean that there is a leakage current path from the input to all the capacitors through the gate-drivers and the parasitic capacitances of the large switches in the integrated power stage. This together with the parasitic capacitance of the switches themselves means, that during the input voltage ramp-up the capacitors are charged to voltages dependent on the capacitor size and their specific parasitic leakage current.

This results in undesired voltages during the input voltage ramp-up. Since the capacitor voltage differences can easily be several volts and the integrated switches around $100\,\mathrm{m\Omega}$ a large peak current can easily be observed in the first switching periods during start-up. The peak current can be estimated by observing that the connection is an RLC-circuit. [7] The peak current can be expressed as:

$$i_{peak} = \frac{V_s}{L \cdot w_d} \mathrm{e}^{\frac{-R\pi}{4Lw_d}} \tag{1}$$

where $w_d = \sqrt{\frac{1}{LC} - \alpha^2}$ and $\alpha = \frac{R}{2L}$. Here V_s is the capacitor voltage mismatch, R is the total series resistance in the loop dominated by the integrated switches, C is the total capacitance from the output and flying capacitors and L is the total inductance from the bonding wires. This peak current can lead to damage in the bonding wires during start-up. This damaged can be reduced by choosing wider and multiple bonding wires in parallel for each bonding pad but the peak current still resolves in a fragile start-up sequence.

To overcome this challenge the capacitor voltages must be charged such that they match those of the steady-state capacitor voltages. In the case of the 4-1 ladder converter topology that means that all capacitors must have a $1/4V_{in}$ voltages across them before any switching occurs. This should be achieved in a robust fashion without any significant addition to the power loss of the power converter, since that degrades the power efficiency. Note that classical inductor-based power converters also suffers from large inrush currents during start-up. This is usually solved by various inrush limiter circuits such as in [8]. However, this is not a viable solution in the case of a switched-capacitor converter, since the large peak currents originates from the capacitor voltage mismatch and being connecting in parallel through low resistance paths and not from being connected to the power converter input.

A. Passive external start-up circuit

The capacitor voltage mismatch generated by the charge leakage path through the switches can be controlled by connecting a capacitor from o_2 to the power converter input. This can be seen in Fig. 2. A start-up control bit (s_{en}) controls the M_1 switch and a charge path is created through C_1, C_2 and C_3 as they are connected in series with the input. This makes the drain-source voltage of M_7 negative turning on the parasitic diode of M_7. Thereby an equivalent circuit of series capacitance $C_1 - C_3$ is in parallel with series capacitance $C_{start} - C_5$. To ensure that during the input voltage ramp-up the voltages across all capacitors is the same the capacitors should be sized by

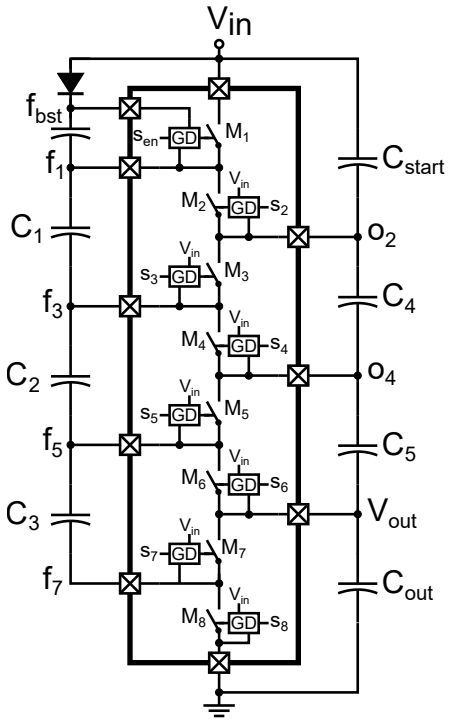

Fig. 2: Switched-capacitor converter implemented with a ladder topology and with the start-up capacitor C_{start} added. The start-up bit s_{en} controls the M_1 switch during start-up.

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_{start} = 0.5 \cdot C_{out} \quad (2)$$

This ensures that the voltage across each capacitor $1/4$ of the input voltage. The capacitors' charge times are dependent on the total time constant of the system. This time constant is dependent on bonding wire resistance, capacitor equivalent series resistance and capacitor sizes. The passive start-up circuit is dependent on that M_1 can be turned on at an early stage of the start-up procedure. Since the gate signals are controlled on chip by a $5\,\mathrm{V}$ digital supply voltage the input voltage, from which the digital supply voltage is generated, must be above $5\,\mathrm{V}$ before the start-up control bit can be enabled.

This start-up procedure is beneficial since the C_{start} capacitor is an external addition and only specific control of the M_1 switch is required. The limitation of the method is the specific capacitor sizing. The optimal sizing of the capacitors follows the charge flow analysis described in [9]. By resizing to ensure a safe start-up this optimal sizing is not fulfilled meaning that the voltage ripple on all capacitors are not equal. This can be neglected by increasing the size of all capacitors, but still resolves in a sub-optimal design, which increases the total area of the power converter. Another limitation of the start-up procedure is that the start-up is dependent on the relative capacitor sizes. Thereby will any variation in the capacitor sizes due to production variation also alter the effectiveness of the start-up method. A benefit of this start-up method is that the addition of C_{start} does not affect the power converter operation or consume any static current. It does however increase the total power converter area since the extra capacitor, C_{start}, is added.

B. Active internal start-up circuit

To save area and utilize optimal capacitor sizing an internal circuit responsible for charging the output capacitors (C_4, C_5 and C_{out}) to the desired steady-state voltages can be seen in Fig. 3. The schematic of the active pre-charge circuit (APC) can be seen in Fig. 4. Here the diode-coupled M_{diode} is biased by the depletion-mode transistor M_{cs} and R_{ref} working as a current source. The transistor M_{diode} is biased such that V_{ref} can be expressed as:

$$V_{ref} = V_x + V_{th,Mdiode} \quad (3)$$

where $V_{th,Mdiode}$ is the threshold voltage of M_{diode} and V_x is the reference voltage, which the active pre-charge circuit should charge the V_{charge} node to. The M_{pass} acts as a pass device as long as:

$$V_{eff,Mpass} = V_{ref} - V_{charge} - V_{th,Mdiode} > 0 \quad (4)$$

Where $V_{eff,Mpass}$ is the effective voltage of the pass transistor. This means that the voltage generated at the output of the APC, V_{charge}, converges towards:

$$V_{charge} = V_{ref} - V_{th,Mdiode} = V_x + V_{th,Mpass} - V_{th,Mdiode} \quad (5)$$

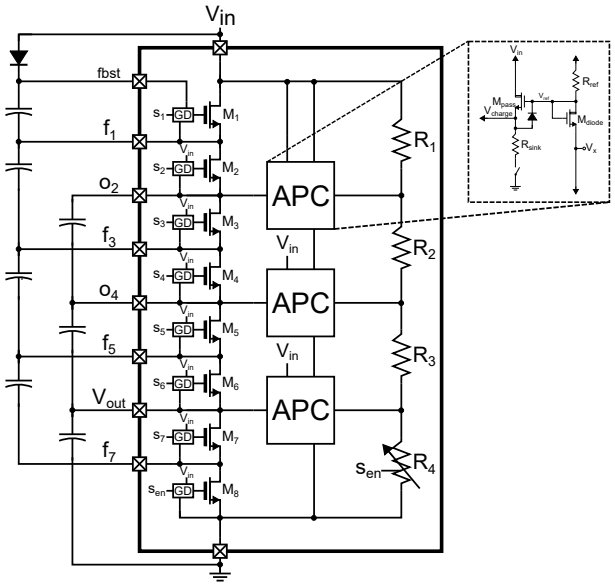

Fig. 3: The 4-to-1 integrated ladder converter with the active pre-charge circuit (APC) blocks.

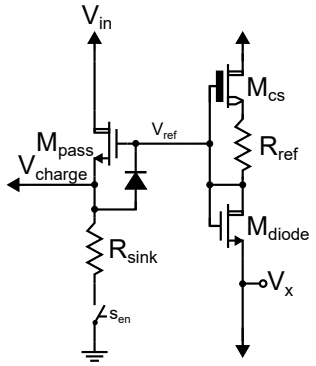

Fig. 4: Active pre-charge circuit block for charging the output capacitors to the desired steady-state voltage.

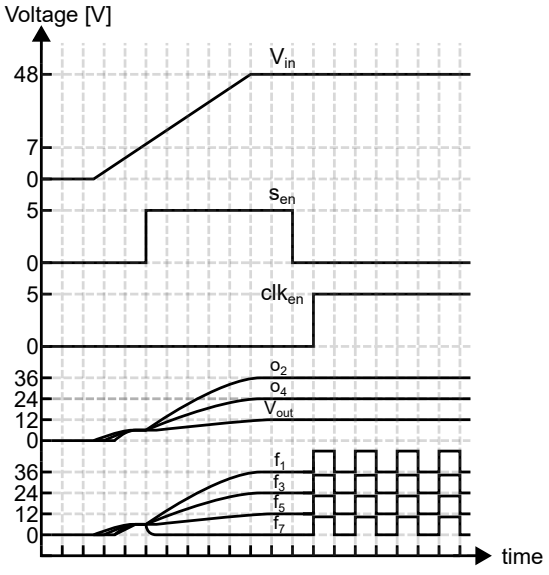

Fig. 5: Start-up procedure and switched-capacitor power converter voltages using the active pre-charge circuit to ensure safe start-up.

by matching M_{pass} and M_{diode} identical threshold voltages can be achieved and the output of the APC becomes:

$$V_{charge} = V_x \tag{6}$$

The resistor R_{sink} is responsible for current sinking, since the V_{charge} can also be above V_{ref} before the start-up circuit is enabled. The reference for the APC blocks are generated by a resistor string ($R_1 - R_4$). Since this is connected directly from the power converter input to ground the total resistance should be designed to be large enough such as the quiescent current does not degenerate the converter efficiency significantly. The resistor ladder generates the voltages $3/4V_{in}$, $1/2V_{in}$ and $1/4V_{in}$. The resistor R_4 is a variable resistor controlled by the start-up enable bit s_{en}. When $s_{en} = 1$ the resistors are all equal, while when the converter has reached the steady-state voltages and start-up is disabled R_4 is reduced thereby decreasing the reference voltages for the APC blocks. This means that V_{ref} for all the APC blocks is decreased and the requirement in (4) is never true, turning off the M_{pass} transistor. The current sinking path through R_{sink} is also turned off by a switch controlled by the s_{en} bit. In Fig. 5 the start-up procedure with the active pre-charge circuit is shown. The input voltage is ramped up and when it reaches above 7 V the start-up enable signal s_{en} is enabled. This turns on power transistor M_8, connecting the flying node f_7 to ground. The APC blocks now starts charging the output nodes to the desired steady-state voltages. The flying nodes f_1, f_3 and f_5 are charged through the body diodes of M_2, M_4 and M_6 respectively. This charging current from the APC should be low enough so that the switches are not damaged, since the body diodes have limited charging capabilities. This current is limited by the maximum output current from the pass devices in the APC blocks. This means that when the power converter clock is enabled by clk_{en} the capacitor voltages are all equal to the desired $1/4V_{in}$ and no large peak current is experienced.

III. Simulation Results

To verify the two proposed start-up methods the high-voltage switched-capacitor power converter has been designed in a 180 nm SOI process and the performance simulated. The start-up procedure shown in Fig. 5 has been used for both the passive start-up and the active pre-charge start-up method.

A. Baseline without start-up circuit

A simulation without any of the two start-up methods has also been done to show the bonding wire peak current baseline. In this case the start-up bit s_{en} is kept low and the clock is enabled, when the input voltage has reached the desired 48 V. The switched-capacitor voltages during the input voltage ramp-up with the start-up circuit disabled can be seen in Fig. 6. Here it can be seen that as the input voltage increases so does the capacitor nodes. They do however not reach the desired values for steady-state. In Fig. 7 the bonding wire currents can be seen when the the clock is enabled. Here it is clear that the switched-capacitor nodes have not reached the desired voltages and that this leads to peak currents close to 40 A. It can be seen that the current going into the chip from the f_7 node must go through M_7 since it can be seen to go out of the V_{out} node. These 40 A would most likely burn both the bonding wire and damage the M_7 switch. Especially after repeated start-up sequences. It can be seen that the peak current decreases with time, since the switched-capacitor nodes settles towards their desired steady-state voltages. In the high-voltage switched-capacitor converter there are 6 bonding wires connected in parallel from the pads from f_7 on the chip to the packaging. The same is true for the V_{out}-pad. These each have a length of around 3.2 mm and a diameter of 33 μm. With the current being equally distributed this means that the bonding wire's each see about 6.67 A. According to [10] a 3 mm gold wire with 33 μm diameter have a fusing current of around 0.665 A. This fusing current

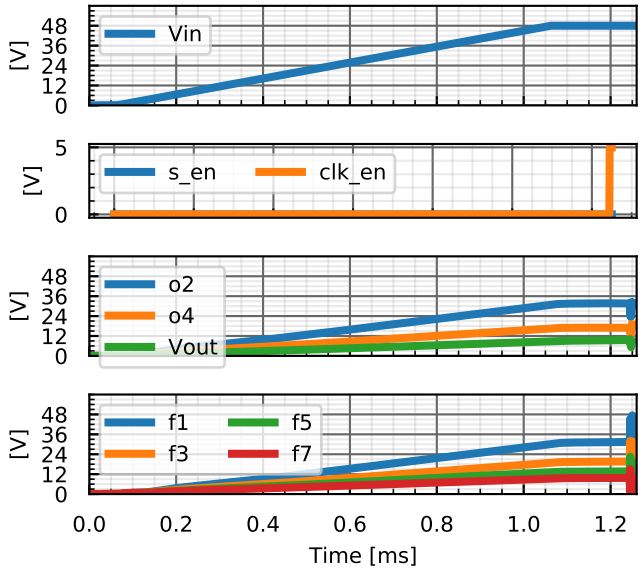

Fig. 6: Switched-capacitor voltages with no start-up method enabled.

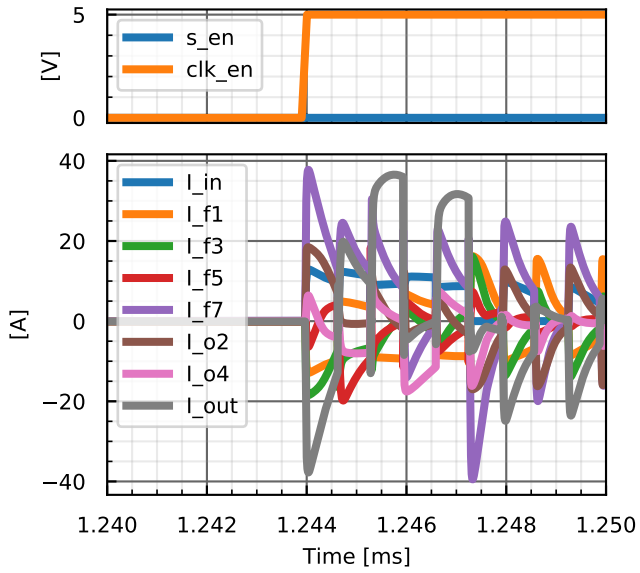

Fig. 7: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with no start-up method enabled.

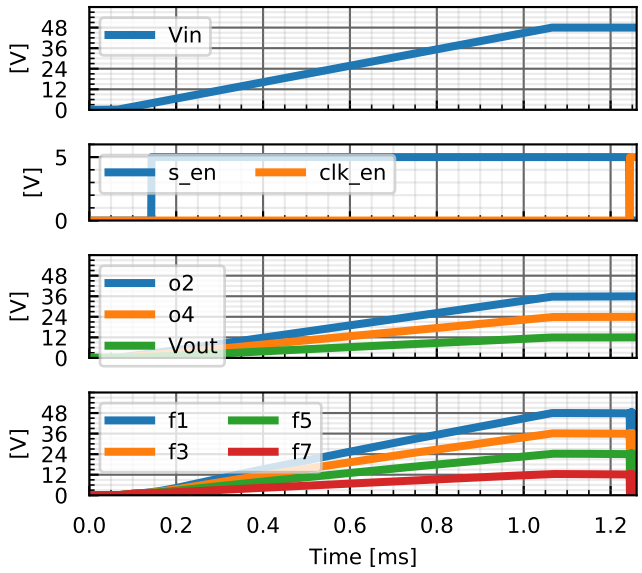

Fig. 8: Switched-capacitor voltages with the passive start-up method.

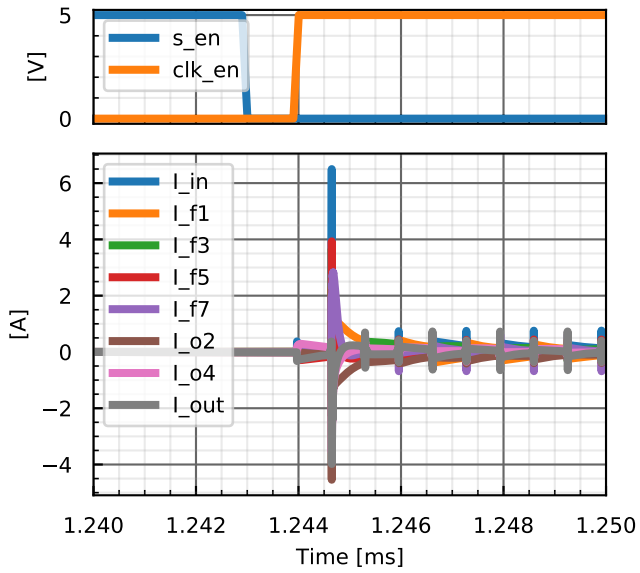

Fig. 9: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with the passive start-up method.

is the bonding wire's RMS fusion current. Estimating the peak current as a triangular wave the approximate peak current fusion current is around:

$$I_{peak} = \sqrt{3} \cdot 0.665\,\text{A} = 1.15\,\text{A} \tag{7}$$

Since the bonding wire peak current is almost six times this limit, the bonding wire would be expected to get damaged during repeated start-up procedures.

B. Passive start-up method simulation results

In Fig. 8 the switched-capacitor converter voltages nodes can be seen, where a capacitor C_{start} is connected from o_2 to V_{in} as is shown in Fig. 2. Here the capacitors C_{start}, C_1, C_2, C_3, C_4 and C_5 are $5.4\,\mu$F and C_{out} is $10.8\,\mu$F. In Fig. 8 M_1 is controlled by s_{en} during start-up and M_1 therefore connects the f_1 node to V_{in}. In Fig. 8 it can be seen that all the voltage nodes reach their desired steady-state voltages. In Fig. 9 the switched-capacitor converter bonding wire currents can be seen when the clock is enabled. Now, since the capacitors have approximately the same voltages when connected through the low resistance switches, the maximum peak current is $6.5\,\text{A}$ through the bonding wire connected to the input of the power converter. It can also be seen that after a single switching period the peak current is down to what is expected for steady-state operation. There are 3 bonding wires of length $2.3\,\text{mm}$ connected to the input bonding pad. According to [10] the fusion RMS current for this bonding wire is around $0.95\,\text{A}$. The approximate peak fusion current is then $1.65\,\text{A}$. This is lower than the expected peak current of $\frac{1}{3} \cdot 6.5\,\text{A} = 2.17\,\text{A}$ per bonding wire and could mean that the bonding wire could get damaged after repeated start-up sequences.

C. Active pre-charge circuit start-up method simulation results

In Fig. 10 the switched-capacitor node voltages can be seen during the input voltage ramp-up. Note that here the M_8 switch is turned on by the s_{en} signal, which means that the f_7 node is connected to ground. It can be seen from Fig. 10 that all the switched-capacitor voltage nodes reach the desired steady-state. In Fig. 12 the bonding wire currents can be seen when the clock is enabled. In this case, the maximum peak current through a bonding wire is $3.5\,\text{A}$. This is through the output node bonding wire and the f_7 node bonding wire. These have 6 bonding wires each, which means that the largest bonding wire current is $0.58\,\text{A}$. With a bonding wire length of $3.2\,\text{mm}$ the peak fusion current is around $1.15\,\text{A}$. This means that the bonding wires should be safe even for repeated starting sequences. The active pre-charge circuit consumes a static $105\,\mu\text{A}$, when the converter has reached steady-state. This means that the active pre-charge circuit does not affect the power converter efficiency in any significant way compared to the power converter output power of $12\,\text{W}$.

IV. Discussion

A summary of the simulation results of the start-up methods together with the designed switched-capacitor power converter can be seen in Table I. Here it can be seen that the two methods reduces the bonding wire inrush current from $40\,\text{A}$ to $6.5\,\text{A}$ and $3.5\,\text{A}$ for the passive start-up and the active pre-charge method respectively. Since not much prior work has been published on

TABLE I: Summary of the simulation results for the different start-up sequences.

Start-up method	No start-up	Passive start-up	Active start-up
Maximum peak current [A]	40	6.5	3.5
Peak current bonding wire	V_{out} and f_7	V_{in} and o_2	V_{out} and f_7
Peak current per bonding wire [A]	6.67	2.17	0.58
Peak bonding wire fusion current [A]	1.15	1.65	1.15
$I_{quiescent}$ [μA]	0	0	105
Extra capacitor added	No	Yes	No

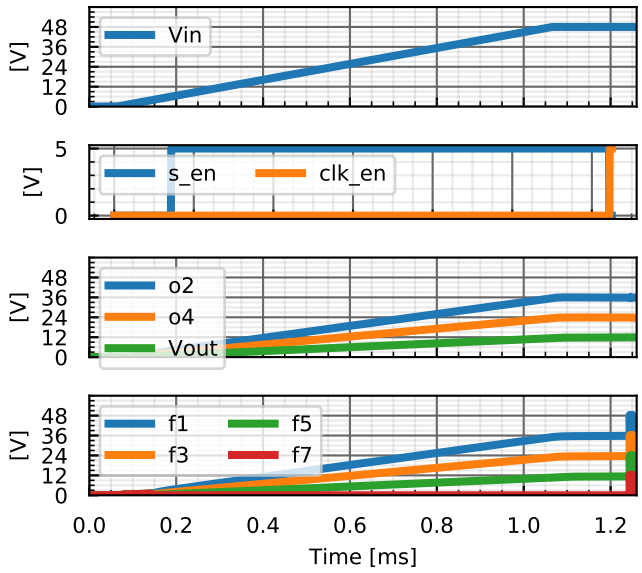

Fig. 10: Switched-capacitor voltages with the active pre-charge start-up method.

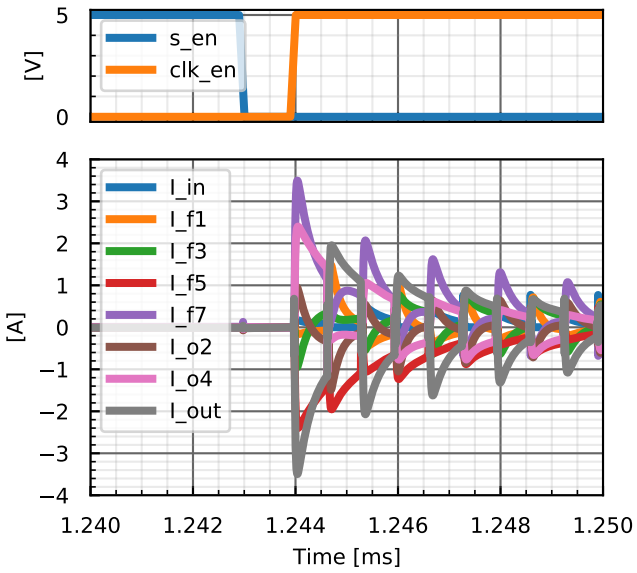

Fig. 12: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with the active pre-charge start-up method.

the challenges of start-up in switched-capacitor converters with an integrated power stage it has not been possible to compare these results with the state-of-the-art. The performance of the active pre-charge start-up method us simulated across global variations and from temperatures at 27 °C, 80 °C and 100 °C. The largest peak current comes from the 27 °C case, which is 3.5 A. The resistor string responsible for the reference voltages for the APCs has been carefully matched, such that local mismatch variations does not alter the APC output voltages.

V. Future Work

The switched-capacitor converter with the integrated power stage and the active pre-charge start-up circuit has been sent to fabrication and is expected back December 2021. The performance of both the power converter and the start-up sequences described in this paper is to be validated with measurement results. In the future a start-up method based on the work in [7] could also be interesting, since it saves the area of the APC blocks and could lower the quiescent current consumption of the start-up circuit.

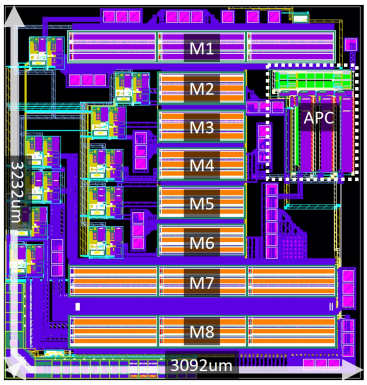

Fig. 11: Layout of the designed and taped out 48 V-12 V switched-capacitor converter with the integrated power stage and active pre-charge circuit (APC).

VI. Conclusion

Two start-up methods have been designed and presented for a 12 W, 48 V-12 V switched-capacitor power converter with an integrated power stage implemented in a 180 nm SOI process. First an analysis of the challenges in start-up for a switched-capacitor power converter has been presented. Next the two proposed solutions have been shown and the trade-offs of each method presented. The first method controls the top switch of the integrated power stage to charge all capacitors during input ramp-up together with an extra external capacitor and careful sizing of the capacitors to ensure that all capacitors are charged to the same voltages. The second method uses a fully integrated active pre-charge circuit to charge the external capacitors to the desired steady-state voltages before enabling the power converter. Both implementations have been verified in simulation and compared to a baseline of 40 A inrush current from not using a dedicated start-up circuit. The passive method does not consume any additional static current, but does increase the converter size with an added capacitor, additionally it uses sub-optimal capacitor sizing for the converter, this limits the peak inrush current to 6.5 A. The active pre-charge circuit consumes a static 105 µA and has an area of 743 µm×911 µm, this limits the peak inrush current to 3.5 A. Finally, a discussion of the results is presented and future work of the start-up methods is presented.

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