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High-voltage Pulse-triggered SR Latch Level-Shifter Design Considerations

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Abstract—This paper compares pulse-triggered level shifters with a traditional level-triggered topology for high-voltage applications with supply voltages in the 50 V to 100 V range. It is found that the pulse-triggered SR (Set/Reset) latch level-shifter has a superior power consumption of 1800 $\mu\text{W}/\text{MHz}$ translating a signal from 0-3.3 V to 87.5-100 V. The operation of this level-shifter is verified with measurements on a fabricated chip. The shortcomings of the implemented level-shifter in terms of power dissipation, transition delay, area, and startup behavior are then considered and an improved circuit is suggested which has been designed in three variants being able to translate the low-voltage 0-3.3 V signal to 45-50 V, 85-90 V, and 95-100 V respectively. The improved 95-100 V level shifter achieves a considerably lower power consumption of 438 $\mu\text{W}/\text{MHz}$ along with a significantly lower transition delay. The 45-50 V version achieves 47.5 $\mu\text{W}/\text{MHz}$ and a transition delay of only 2.03 ns resulting in an impressive FOM of $2.03 \text{ ns}/(0.35 \mu\text{m } 50 \text{ V}) = 0.12 \text{ ns}/\mu\text{m V}$.

I. INTRODUCTION

Level shifters are used in applications where there is a need to interface between different voltage domains. Two types of level shifters can be distinguished by whether the voltage domains share a common ground potential or not. Full-swing level shifters translate signals between voltage domains sharing a ground potential and are typically used to interface between a low voltage digital domain and analog domain circuitry or input/output pins, typically having a higher supply voltage.

On the other hand, floating level shifters are characterized by the two voltage domains not sharing a common ground potential. These level shifters can be used in gate drivers for high voltage (HV) drain-extended MOS (DMOS) transistors with thin gate-oxide where $V_{gs,max}$ is significantly lower than $V_{ds,max}$. Gate drivers based on floating level shifters are often used in power output stages in applications such as DC-DC converters [1], biomedical transducer drivers [2], and Class-D audio amplifiers [3]. The floating level shifters often translate signals up to high voltage levels of tens to hundreds of Volts. Sourcing charge from a high-voltage supply to ground will result in a high power consumption, rendering reduction of the current drawn from the high voltage supply paramount to the design of efficient floating level shifters. Especially, when considering high-voltage battery-powered applications such as handheld ultrasound scanners [4] where power consumption should be kept minimal.

This work considers different level shifter topologies for use in a transducer interface operating at 5 MHz where several power nDMOS and pDMOS transistors referred to different fixed supply rails, ranging from 50 V to 100 V, need low-power gate drivers. In addition to these fixed-supply gate-drivers the possibility of operating the level shifters in a power domain ramping at up to 2 V/ns from the lowest to highest supply rail should also be considered to enable the use of floating high-side nDMOS gate drivers where the gate driver is referenced to the source potential of the nDMOS being driven. The performance of a basic level-triggered level-shifter is compared to a pulse-triggered topology in terms of power dissipation and transition delay. The flexibility of the topologies, in terms of what range of HV domain signal amplitude is feasible to use, i.e. with which V_{gs} the DMOS transistors can be driven, is also considered. The designs considered are using internal components only.

A pulse-triggered level shifter has been fabricated following the design considerations and measurement results of this level shifter are presented. The performance and area limitations of the fabricated level-shifter are identified and an improved circuit is suggested that employs a more robust way of controlling the magnitude of the current pulses used in the pulsed level-shifter topology.

II. DESIGN OF A HIGH-VOLTAGE FLOATING LEVEL-SHIFTER

The basic level-triggered HV level-shifter in Fig. 1 [5] is first considered as a candidate topology for a gate driver to a pDMOS transistor with the source connected to a 100 V supply. Thick gate-oxide pDMOS transistors are used with a driving V_{gs} of 12.5 V. Referring to Fig. 1 the voltage potentials considered are: $V_{DDH} = 100 \text{ V}$, $V_{SSH} = 87.5 \text{ V}$, $V_{DDL} = 3.3 \text{ V}$. The HV domain signal amplitude is named $V_H = V_{DDH} - V_{SSH}$ for future reference. It is evident that this design requires a large amount of deep N-wells which comes with a high area-penalty in the process considered here as each deep N-well biased at a high voltage potential has to be enclosed by a large guardring biased at the substrate potential.

To size the transistors in the level shifter in Fig. 1, the DC operation of the circuit is investigated. The case where $V_{out} = V_{SSH}$ and $V_c = V_{DDH}$ (the input voltage to the inverter) is considered. Upon a low-to-high transition of V_{in} , M1 will

pull the source of M3 to ground resulting in M3 pulling V_b to ground as well. Now, the pDMOS transistor M5 needs to be strong enough to change the state of the M7/M8 latch. This requirement results in the constraint that M5 needs to be stronger than M7 when $V_c = V_{DDH} - V_{th8}$, i.e. in the instant where M8 will start to conduct and, via positive feedback, change the state of the latch. With the given voltage levels M5 is in the saturation region and M7 is in the linear region. Equating I_{D5} and I_{D7} :

$$I_{D5} = \frac{K'_{p5}}{2} \left(\frac{W}{L} \right)_5 (V_H - V_{th8} - V_{th5})^2 \quad (1)$$

$$I_{D7} = K'_{p7} \left(\frac{W}{L} \right)_7 (V_H - V_{th7}) V_{th8} \quad (2)$$

Here the square-law equations are used neglecting the $V_{DS}^2/2$ term in (2), channel-length modulation is ignored, and the transconductance parameter $K'_p = \mu_p C_{ox}$ was used. Due to symmetry the transistors M2/M4/M6/M8 are sized equal to their M1/M3/M5/M7 counterparts which results in $V_{th8} = V_{th7}$. With this in mind, and defining the device size as $S = W/L$, the following minimum size ratio is obtained:

$$\frac{S_5}{S_7} = \frac{2K'_{p7}}{K'_{p5}} \frac{(V_H - V_{th7}) V_{th7}}{(V_H - V_{th7} - V_{th5})^2} \quad (3)$$

Using the device parameters from the HV CMOS process used in this work, (3) gives the following device size ratios:

$$\left(\frac{S_5}{S_7} \right) \Big|_{V_H=12.5\text{ V}} > 0.5 \quad (4)$$

$$\left(\frac{S_5}{S_7} \right) \Big|_{V_H=5\text{ V}} > 1 \quad (5)$$

Here (4) refers to the devices used in Fig. 1, and (5) was calculated using device parameters for a similar design where $V_H = 5\text{ V}$, i.e. where the amplitude of the HV domain signal is reduced to 5 V enabling the use of low-voltage (LV) transistors in the latch. It is evident from (4)-(5) that reasonable device sizes can be used for the voltage levels considered in the application at hand. If V_H is reduced further the S_5/S_7 ratio might become prohibitively large, calling for very large M5/M6 devices as was noted in [6]. Using these results the level-triggered level-shifter is sized as annotated in Fig. 1. Using minimum size devices for both M5/M6 and M7/M8 yields $S_5/S_7 = 1$ which adheres to the constraint from (4). Simulation results of this level shifter are presented in Table I. With the power consumption listed, the level-shifter will dissipate more than 16 mW at 5 MHz clock frequency which is found to be too large.

In [6] a thorough analysis of a similar topology is carried out and in addition to the large area it was found that both the power consumption and transition delay were high compared to other topologies. The level shifter in [6] having the lowest transition delay and power dissipation needs a separate startup pulse referred to V_{SSH} to ensure a well-defined initial condition. This signal can be generated by a slower level-shifter during startup and distributed to all fast

TABLE I
SIMULATED PERFORMANCE OF THE LEVEL-TRIGGERED LEVEL-SHIFTER TOPOLOGY OVER PROCESS VARIATIONS. THE RESULTS ARE OBTAINED WITH A 100 PF LOAD CAPACITOR.

	Min	Typical	Max
Power [$\mu\text{W}/\text{MHz}$]	2980	3210	3790
$T_{L \rightarrow H}$ [ns]	5.08	8.28	12.1
$T_{H \rightarrow L}$ [ns]	5.69	9.64	14.6

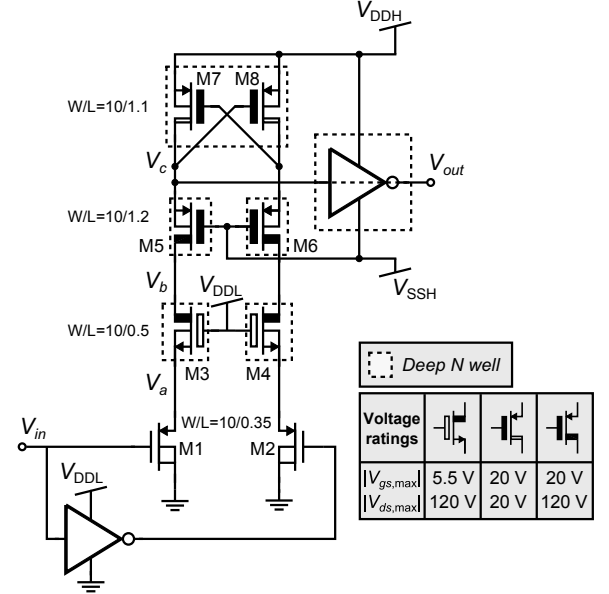


Fig. 1. Schematic of a basic level-triggered HV level-shifter.

level shifters referred to the same V_{SSH} . As the application considered in this work has several HV voltage-domains and because V_{SSH} might be variable, e.g. in high-side nDMOS gate drivers where V_{SSH} would be connected to the source of the floating nDMOS, a separate startup signal would need to be generated for each level shifter which is not found feasible. Next, a pulse-triggered SR (Set/Reset) latch level-shifter is considered instead.

A. The pulse-triggered SR latch level-shifter

The design chosen for the manufactured level shifter is shown in Fig. 2. The SET and RESET pulses for the level shifter are generated by the circuit in Fig. 3. Several variations of this topology, the pulse-triggered SR latch level-shifter, has been published [3], [7], [8].

The implemented level-shifter is characterized by a low component count due to the aforementioned deep N-well area cost. The driving V_{gs} of the floating SR latch is $V_H = 12.5\text{ V}$ and this necessitates thick gate-oxide on all transistors in the HV domain. In the process used the thick-oxide nDMOS devices can only share deep N-wells with other nDMOS transistors having the same drain voltage. Similarly, thick-oxide pDMOS devices can only be used with other pDMOS devices having the same source voltage. Despite these drawbacks

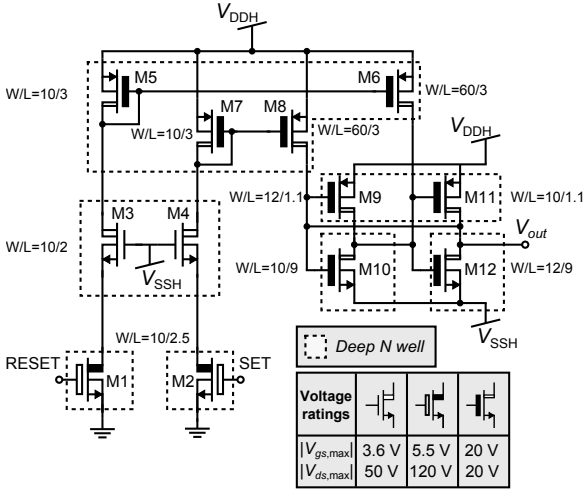


Fig. 2. Schematic of the implemented 100 V pulse-triggered SR latch level-shifter. All device dimensions are given in μm .

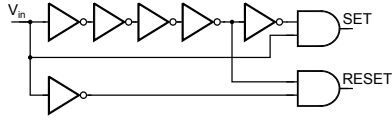


Fig. 3. Schematic of the SET/RESET pulse generator. Layout area: $39 \mu\text{m} \times 13 \mu\text{m}$.

the thick gate-oxide DMOS transistors were chosen due to other system level considerations. The main purpose of the fabricated level-shifter is to prove that this topology is suited for the application at hand.

The operation of the level-shifter topology is as follows (considering a low-to-high transition of V_{out}):

- A pulse with a pulse-width $t_{\text{pulse}} < 1/(2f_s)$ and an amplitude of V_{DDL} referred to ground, where f_s is the frequency of the LV input signal, is applied to the gate of M2. In the fabricated level-shifter $t_{\text{pulse}} = 10 \text{ ns}$ in the typical process corner.
- M2 will pull the source of M4 toward ground which in turn will pull the source of M7 down to a lower voltage potential.
- The current mirror consisting of M7 and M8 will transfer a six times larger current pulse to the latch.
- The current provided by M8 is significantly larger than what M12 in the latch can sink which results in V_{out} being pulled to V_{DDH} effectively changing the state of the SR latch.

B. Device size considerations

Referring to the schematic in Fig. 2 the following considerations were made when sizing the transistors:

- The input transistors M1/M2 should be sized to provide a sufficient current pulse to change the state of the latch fast. Choosing a width of $10 \mu\text{m}$ (the minimum allowed in the process) and a length of $2.5 \mu\text{m}$ (larger than the

TABLE II
SIMULATED PERFORMANCE OF THE PULSE-TRIGGERED SR LATCH LEVEL-SHIFTER TOPOLOGY OVER PROCESS VARIATIONS. THE RESULTS ARE OBTAINED WITH A 100 pF LOAD CAPACITOR.

	Min	Typical	Max
Power [$\mu\text{W}/\text{MHz}$]	1600	1800	2010
$T_{L \rightarrow H}$ [ns]	9.65	15.7	26.0
$T_{H \rightarrow L}$ [ns]	7.66	12.1	19.0

minimum allowed in the process), the latter being chosen on behalf of device lifetime simulations.

- The cascodes M3/M4 should be large enough to discharge the PMOS current mirror nodes (gates of M5/M6 and M7/M8, respectively) fast. The minimum device size of $10 \mu\text{m} \times 3 \mu\text{m}$ (taking device lifetime into account) was found to be sufficient.
- M5/M7 should have a higher $I_{d,sat}$ than M1/M2 to properly protect the gate-oxide of M5-M8 from breakdown. Equating the drain currents for the two opposing transistors for the device sizes in Fig. 2 and defining the maximum allowable V_{sg} of M5/M7 to 12.5 V:

$$I_{d1,sat} = \frac{1}{2} K'_{n1} \frac{10}{2.5} (3.3 \text{ V} - V_{th1})^2 = 1080 \mu\text{A} \quad (6)$$

$$I_{d5,sat} = \frac{1}{2} K'_{p5} \frac{10}{3} (12.5 \text{ V} - V_{th5})^2 = 2450 \mu\text{A} \quad (7)$$

From this it is clear that the gate-oxide of M5-M8 will be operated below breakdown conditions even with a continuous high input signal as $I_{d5,sat} > I_{d1,sat}$ at the specified maximum V_{sg5} .

- The SR latch comprise the transistors M9-M12 which are sized according to two considerations (note that the minimum width of M9-M12 is $10 \mu\text{m}$, limited by the process design rules):
 - The switching threshold of the two inverters are set significantly closer to V_{DDH} than V_{SSH} which result in small W/L ratio of the NMOS transistors such that the latch requires as little current from M6/M8 to change state as possible.
 - The latch is sized asymmetrical to force it to a well-defined initial condition upon system startup.

C. Simulation Results

The performance of the level shifter in Fig. 2 is simulated across process corners and the results are listed in Table II. Note that the transition delay is evaluated from the input of the pulse generator to the voltage across the 100 pF load capacitor. Comparing these results with those listed for the level-triggered topology in Table I it is evident that the implemented pulse-triggered topology only dissipates around half the power albeit it is slower than the level-triggered topology.

In addition to the common performance parameters, the startup behavior of the SR latch is also investigated. A symmetrical SR latch is bistable and its initial condition is therefore unknown. The SR latch designed in Fig. 2 was designed asymmetrical to force the level-shifter output, V_{out} , to

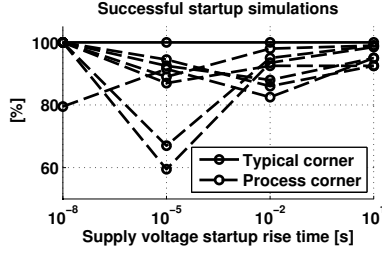


Fig. 4. Monte Carlo simulation of the SR latch initial condition across process corners for various V_{DDH} supply rail rise times.

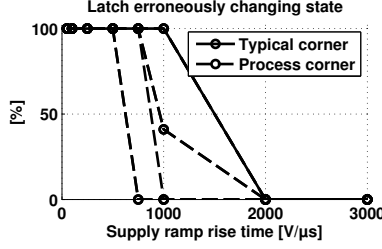


Fig. 5. Monte Carlo simulation of the SR latch state retention for various HV domain ramp rise times (when used in high-side nDMOS gate-driver applications).

V_{SSH} upon power-up. To test this the circuit is first considered in steady state with $V_{DDH} = V_{SSH} = 87.5$ V and $V_{DDL} = 3.3$ V, i.e. with $V_H = 0$ V supply voltage across the SR latch. A linear ramp of the V_{DDH} supply rail from 87.5 V to 100 V with a transition time of T_{rise} is then applied to the system. This test was performed for T_{rise} equal to 10 ns, 10 μ s, 10 ms, and 10 s each with 200 random Monte Carlo mismatch iterations across 8 process corners on the RC extracted layout (a total of 6400 startup events). The results are visualized in Fig. 4. This simulation reveals that it is a challenge to ensure a well-defined initial condition of the SR latch by sizing it asymmetrical.

By sizing the latch asymmetrical it will also have a tendency to favor the state where $V_{out} = V_{SSH}$ (if it is sized to have this as the initial condition) when subject to various error conditions. This turns out to be a problem when the HV power domain is ramping as will be the case when using the level shifter in a high-side nDMOS gate driver (where it will float with the nDMOS source voltage). Parasitic capacitance on the drain nodes of M1/M2 will cause a common-mode error current to be generated in the Set and Reset branches, including the drains of M5/M7. This common mode current will be transferred to the asymmetrical latch via M6/M8. If the latch had been SIZED SYMMETRICAL it would, ideally, have been immune to this common mode current but having a asymmetrical latch will cause unintended changes of the latch state if the ramp on V_{SSH} and V_{DDH} is fast. This is investigated in Fig. 5 where, again, 200 random Monte Carlo mismatch iterations across 8 process corners on the RC extracted layout is simulated for varying HV domain ramp rise times. It is evident that the HV domain ramp speed has to be limited to 0.5 V/ns to avoid unintended latch state changes.

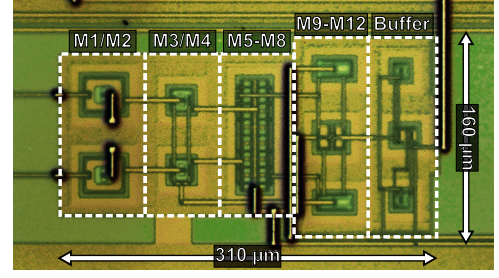


Fig. 6. Micrograph of the implemented 100 V pulse-triggered SR latch level shifter.

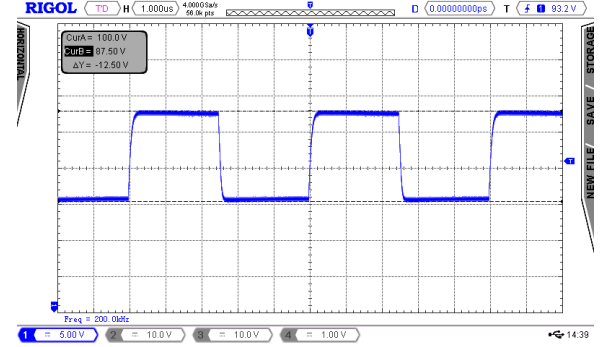


Fig. 7. Measured output voltage of the level shifter with a 200 kHz square wave input. The output switches between 87.5 V and 100 V as intended.

As correct initial condition cannot be guaranteed across process corners, as was seen in Fig. 4, it is necessary to ensure that no unwanted startup event will occur by providing the level shifter with an initial "Reset" pulse provided by on-chip control logic as was also found necessary in [7].

III. MEASUREMENT RESULTS

The level shifter design in Fig. 2 was fabricated in a 0.35 μ m HV CMOS process. From the micrograph of the fabricated level-shifter in Fig. 6 the large area penalty of the many deep N wells is visible: the transistors are spaced far from each other resulting in a large area. Also visible in the micrograph is an output buffer that connects the level shifter to a pad. The buffer is sized to drive the pad parasitic capacitance and a measurement probe at 200 kHz as sizing it for operation at 5 MHz would call for a prohibitively large output buffer (bearing in mind that the level shifter will be used to drive internal nodes only under normal operation). The measured level-shifter output at 200 kHz is shown in Fig. 7. It is evident that the level shifter works as intended.

The output signal with 5 MHz input is also measured and shown in Fig. 8. The level shifter is still working as intended although the output signal is distorted by the small output buffer. The current consumption of the level shifter can not be evaluated as it is supplied from the same voltage domain as the buffer driving the large (and to some extent unknown) capacitance of the output pad which would dominate the power consumption as was also the case in [7].

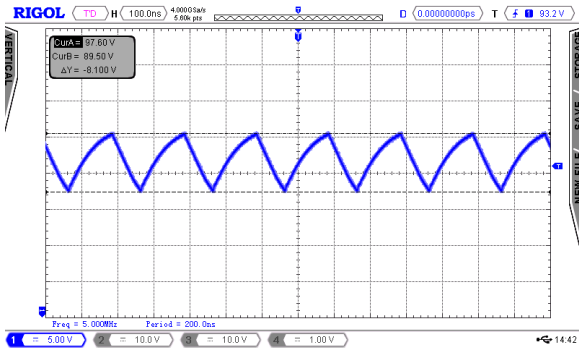


Fig. 8. Measured output voltage with a 5 MHz square wave input. The output voltage swing is limited by the capacitive load comprising the package pad and the oscilloscope probe. Despite the limited buffer driving strength, the level shifter is still operating as intended.

TABLE III
COMPARISON OF SIMULATED PERFORMANCE OF THE FABRICATED AND IMPROVED LEVEL SHIFTERS.

	Area [μm^2]	Power [$\mu\text{W}/\text{MHz}$]	$T_{L \rightarrow H}$ [ns]
Fabricated 100 V	35500	1800	15.7
Improved 100 V	16700	438	7.60
Improved 90 V	13200	400	6.49
Improved 50 V	4600	47.5	2.03

IV. PULSED SR LATCH LEVEL SHIFTER IMPROVEMENTS

While the fabricated level shifter had a considerably lower power consumption than the basic level-triggered level-shifter from Fig. 1 there is still room for improvement. To overcome some of the problems with the design an improved design is suggested in Fig. 9. The voltage in the level-shifter is limited to $V_{DDH} < 50$ V but designs with $V_{DDH} < 90$ V, and $V_{DDH} < 100$ V has also been made (with increasing area for increasing maximum operating voltage). The layout of the 100 V version is shown in Fig. 10 with dimensions annotated for comparison with Fig. 6. The main performance parameters in the typical process corner are tabulated in Table III. Again, the delay is evaluated from the input of the pulse generator to the output voltage across a 100 pF load.

The main differences in the improved design are:

- V_H is reduced from 12.5 V to 5 V. This allows for the floating current mirror and SR latch to be collected in a single deep N well resulting in a considerable area reduction. Notice that only a single deep N well is present in Fig. 9. In addition to the fewer N wells, the 5 V gate-oxide transistors can have a considerably smaller width compared with the thick gate-oxide transistors used in the fabricated design (with 10 μm minimum width).
- The current pulse magnitude is controlled by an "improved Wilson current mirror" M1a/M1b/M1c/M1d in Fig. 9. This allows for a smaller current pulse as it can be controlled from a bias generator with reduced PVT (process/voltage/temperature) dependence. Without the current control one should design for the worst case

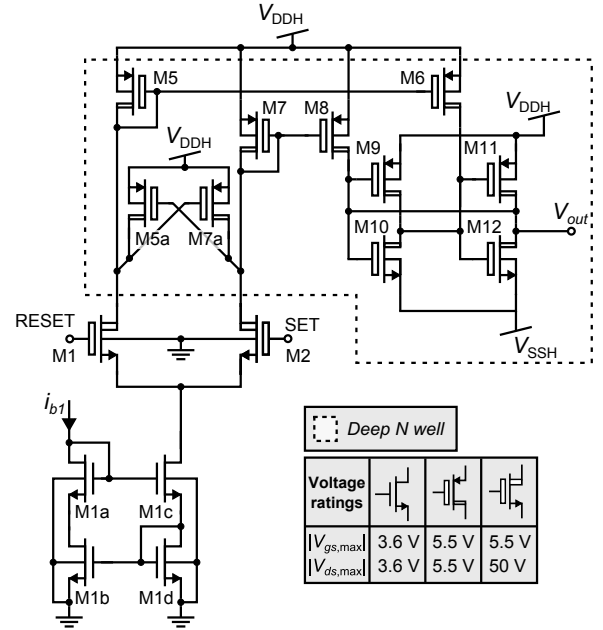


Fig. 9. Schematic of the improved pulse-triggered SR latch level shifter. This version can translate a 0-3.3 V signal to 45 – 50 V.

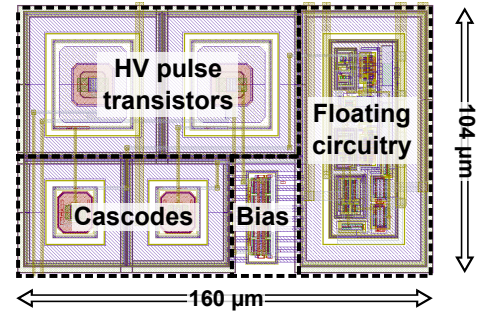


Fig. 10. Layout of the improved pulse triggered SR latch level shifter including the pulse current mirror. The 0-3.3 V to 95-100 V version is shown for reasonable comparison with the layout in Fig. 6.

process corner, usually resulting in over-design in the typical corner.

The improved Wilson current mirror was chosen as it automatically clamps the local reference current i_{b1} (Fig. 9) when no Reset/Set pulse is present. Once a pulse is encountered the mirror will start out with a large current (to discharge all parasitic capacitances), as the drain of M1c is at the ground potential when no pulse is present, before regulating the current to a magnitude set by the reference current (via the negative feedback that the Wilson mirror utilizes). This combination of a large starting current (still lower than the peak current in the fabricated design) followed by a tightly controlled tail current allows for low transition delay and low power consumption.

- Common mode clamping transistors M5a/M7a were added to reduce the common mode current transferred to

the latch when the HV domain is ramping, as proposed in [3]. This was done to improve the ramp immunity (when using the level shifter in a high-side nDMOS gate driver) compared to what was found in Fig. 5.

It is generally more desirable to distribute a reference current than a voltage to the level shifter for controlling the current pulse magnitude. Having a simple current mirror instead of M1a-M1d controlled by a bias voltage would be susceptible to possible ground potential differences between the power domain, where it is desirable to have the level shifters to have them as close as possible to the DMOS transistors being driven, and the analog domain where the bias generator would be located. In the regime of the improved level shifter a single reference current would be distributed to the power domain were a local PMOS current mirror would distribute the i_{b1} reference currents to the level shifters. As the i_{b1} is clamped when the level shifter is not changing state, the power penalty is minimal.

The results in Table III shows that the improved design lowers both area, power dissipation and transition delay considerably compared with the fabricated design and the level-triggered topology. The combination of common-mode clamping transistors and the Wilson current mirror makes for a more robust design, and the lower V_H greatly improves the area. It is clear from Table III that using lower voltage potentials allows for better level shifter performance, as cascode transistors are necessary when handling high voltages. The improved 50 V level shifter has a FOM of $2.03 \text{ ns}/(0.35 \mu\text{m } 50 \text{ V}) = 0.12 \text{ ns}/\mu\text{m V}$ (referring to the simulation results in Table III). This is superior to the 9 FOM's compared in [6], ranging from 0.29 to $28.6 \text{ ns}/\mu\text{m V}$.

The three improved level shifters has been implemented in a transducer driver system which is currently being fabricated.

V. CONCLUSION

Design considerations for designing HV level shifters were presented and the basic level-triggered topology was compared with a pulse-triggered SR latch level-shifter with an asymmetrical latch. The latter was found to have a power dissipation of $1800 \mu\text{W}/\text{MHz}$, around half of that of the level-triggered topology. The operation of the designed pulse-triggered level-shifter was verified on a fabricated chip. The asymmetrical latch is found to limit the robustness of the level shifter, while not being able to guarantee correct initial condition upon startup. An improved pulse-triggered level-shifter design was proposed which improves both area, power dissipation, and transition delay figures. It incorporates common-mode clamp transistors and a Wilson current mirror. The improved design achieves a power consumption of $47.5 \mu\text{W}/\text{MHz}$ with $V_{SSH} = 45 \text{ V}$ and $V_{DDH} = 50 \text{ V}$ with a 100 fF load thus achieving an impressive FOM of $0.12 \text{ ns}/\mu\text{m V}$.

REFERENCES

[1] M. C. W. Høyerby, M. A. E. Andersen, and P. Andreani, "A $0.35 \mu\text{m}$ 50V CMOS Sliding-Mode Control IC for Buck Converters," *ESSCIRC 2007*, 2007.

[2] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 48, no. 11, pp. 2734–2745, 2013.

[3] H. Ma, R. van der Zee, and B. Nauta, "Design and Analysis of a High-Efficiency High-Voltage Class-D Power Output Stage," *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 7, pp. 1514–1524, July 2014.

[4] B. T. Rosen and M. J. Ault, "Portable ultrasound: the next generation arrives," *Critical Ultrasound Journal*, vol. 2, no. 1, pp. 1–4, 2010.

[5] B.-D. Choi, "Enhancement of current driving capability in data driver ics for plasma display panels," *IEEE TRANSACTIONS ON CONSUMER ELECTRONICS*, vol. 55, no. 3, pp. 992–997, 2009.

[6] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond delay floating high voltage level shifters in a $0.35 \mu\text{m}$ hv-cmos technology," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 46, no. 2, pp. 485–497, 2011.

[7] T. Lehmann, "Design of fast low-power floating high-voltage level-shifters," *Electronics Letters*, vol. 50, no. 3, p. 1, 2014.

[8] D. Liu, S. J. Hollis, and B. H. Stark, "A new circuit topology for floating high voltage level shifters," in *Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph.D. Research in*, June 2014, pp. 1–4.