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Capacitor-Free, Low Drop-Out Linear Regulator in a 180 nm CMOS for Hearing Aids

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Abstract—This paper presents a capacitor-free low dropout (LDO) linear regulator based on a new dual loop topology. The regulator utilizes the feedback loops to satisfy the challenges for hearing aid devices, which include fast transient performance and small voltage spikes under rapid load-current changes. The proposed design works without the need of an off-chip discrete capacitor connected at the output and operates with 0-100 pF capacitive load. The design has been implemented in a 0.18 μm CMOS process. The proposed regulator has a low component count and is suitable for system-on-chip integration. It regulates the output voltage at 0.9 V from 1.0 V - 1.4 V supply. A current step load from 250-500 μA with an edge time (rise and fall time) of 1 ns results at ΔV_{out} of 64 mV with a settling time of 3 μs when $C_L = 0$. The power supply rejection ratio (PSRR) at 1 kHz is 63 dB.

I. INTRODUCTION

Linear voltage regulators are important components in today's integrated circuits. For on chip power management, where multiple supply voltages are used, low drop-out (LDO) voltage regulator play an important role. Improving power management will help to extend the battery life and could increase the use of portable devices. As the industry is pushing towards complete system-on-chip (SoC) design solutions, including improving power management, LDO voltage regulators play an important role. Linear regulators have some advantages over switch mode power supplies as they provide lower output noise, less electromagnetic emission, high PSRR and are easy to integrate on-chip within a small area while maintaining an accurate output voltage.

In portable devices such as hearing aids there is a strict requirement on area consumption. The number of discrete components must be minimized, as the electronics must fit in the ear canal. Implementing a capacitor free LDO regulator will help to reduce the overall size by eliminating the large output capacitor and increase the reliability of the system. On the other hand, for a voltage regulator without a on-chip capacitor (usually referred as capacitor-free or capacitor-less) the designer has to design a stable circuit without a large capacitor that sets the dominate pole. In this application the estimated capacitance of load circuitry is between 0-100 pF. The absence of an output capacitor gives rise to issues in the transient response, ΔV_{out} (undershoot and overshoot) that will be larger and there will be an increase of the recovery time (settling time). Moreover a large output capacitor ensures stability as it will set the dominant pole and acts as a supply

for the frequency components of the current load, I_L, outside the bandwidth of the regulator.

Removing the external capacitor requires to overcome the transient response and stability issues mentioned. There have been a number of capacitor-free topologies suggested in earlier articles. This previous research mainly focus on improving the transient performance [1] - [2]. One approach is to use active feedback and slew-rate enhancement circuit [3]. Another approach is a LDO structure with a three-stage amplifier and damping-factor-control frequency compensation [1] or utilizing voltage spike detection [4]. All those approaches and others result in a rather complex design, large area and normally high quiescent current.
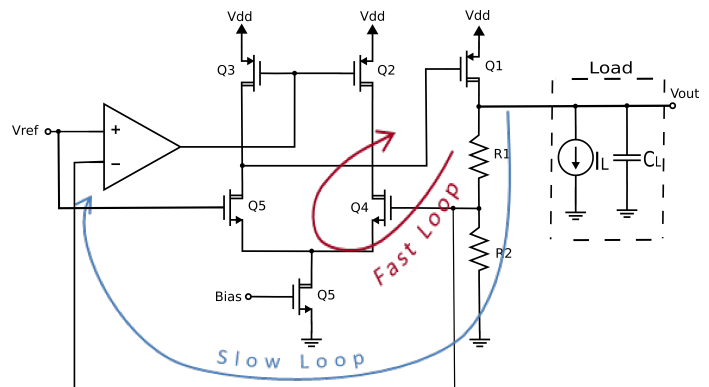

Figure 1. Functional diagram of the proposed LDO linear voltage regulator

Some voltage regulator use NMOS as pass device. Those designs can be smaller in size due to the higher charge carrier mobility in NMOS devices, thus enabling the same drain current with a smaller area. A PMOS pass element reduce the minimum required voltage drop across it. The advantage of using PMOS as pass transistor is that the supply voltage does not need to be significantly higher than the output voltage. Smaller voltage headroom results in less power dissipation, essential for devices like hearing aids.

In this paper, Section II presents the circuit description and introduces the two regulation loops and its design details. Section III discusses the simulation results. Discussion of performance comparison with former work are presented in Section IV. Finally, the conclusions of this paper are given.
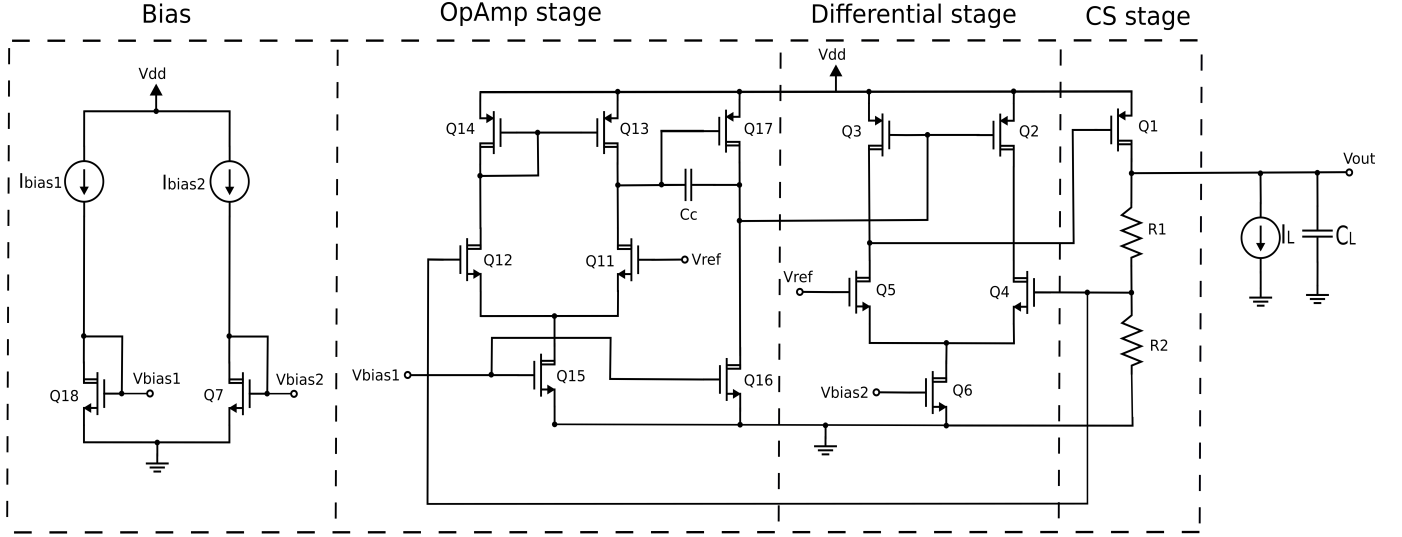
Figure 2. Full schematic of the proposed LDO linear regulator

II. CIRCUIT DESCRIPTION

The new design proposed in this work is based on a principle similar to [5], employing two control loops and an PMOS pass transistor configured as a common source (CS) amplifier. Refer to Fig. 1 for the circuit diagram of the proposed regulator. The design specifications target the following parameters. The regulator is supplied by nominal voltage of 1.2 V and outputs a voltage of 900 mV. The load current, I_L, is 250-500 μA which is stepped with a 1 ns rise and fall time. ΔV_{out} is 64 mV during current step load and the circuit consumes 10.3 μA quiescent current. The capacitance C_L represents the load of up to 100 pF.

The fast loop consists of a differential amplifier stage, driving the common source (CS) amplifier, which include the pass transistor (Q1) and 2 resistors. The PMOS transistors in the differential stage (Q2 and Q3) are controlled by the slow loop containing the operational amplifier. The proposed design does not contain any large passive devices and has a low count of transistors. The simplicity allows for easy and area efficient implementation, while demonstrating good performance. Moreover, reaching stability is simpler compared to other designs due to the low number of poles and zeros. The following sections describe the two control loops in detail. The circuit was biased from two different current sources for debugging proposes. The full circuit diagram can be found in Fig. 2.

A. Principle of Operation of the Fast Loop

The fast loop directly regulates the gate of the pass transistor. Its purpose is to suppress the spikes in the output voltage, V_{out}, which is due to a step in the load. The overall performance of the regulator is impacted by the amplitude of the voltage spikes and the recovery time. By assuming the fast loop constitutes an underdamped system, the gain bandwidth product (GBWP) of the open loop gain will be inversely proportional to the settling time T_s. Therefore we will design the fast loop to have large GBWP. There is a trade-off between the circuit quiescent current in the fast loop stage, to the GBWP of the loop. As can be seen in Fig. 1, this loop starts at the gate of Q4 and ends at the drain of Q1.

The open loop transfer function, $A_{OL}(s)$, is described in (1). In order to analyze the loop, the equation was divided into two parts, CS stage ($H_1(s)$) described in (2) and differential stage ($H_2(s)$) described in (5). From the analysis of the transfer function it can be realized that the parasitic capacitance and resistance of the pass transistor (Q1) dominate the poles ω_{p1} (3) and ω_{pa} (6). The gate-source capacitance is C_{gs1} and C_{gd1} is the gate-drain capacitance of Q1. The output resistance is represented by r_{ds1} and g_{m1} is the transconductance of Q1. The analysis was done with a load capacitance C_L to understand its impact on the system, therefore in the zero load case $C_t = C_{gd1}$. In this work the maximum value of the load capacitance was 100 pF as expected in hearing aids.

$$A_{OL}(s) = H_1(s)H_2(s) \tag{1}$$

$$H_1(s) = -g_{m1}R_t \frac{1}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \tag{2}$$

$$\omega_{p1} = \frac{1}{C_t R_t + R_t(C_{gs1} + g_{m1}R_s C_{gd1})} \tag{3}$$

$$\omega_{p2} = \frac{1}{R_t(R_s g_{m1}C_{gd1} + C_{gs1})} + \frac{1}{C_t R_t} \tag{4}$$

$$Where: R_t = r_{ds1}\|(R_1 + R_2); C_t = C_L + C_{gd1}$$

The differential stage and common source stage set the gain of the fast loop. By maximizing g_{m1} we can achieve higher gain for the CS stage. The poles and zeros were selected in the design of the fast loop to achieve high GBWP. The

high W/L ratio of Q1 will introduce a large gate capacitance which on one hand, will dominate the frequency response of the fast loop. On the other hand, a large pass transistor will also cause high parasitic capacitances which will impact the regulator performance. This big capacitance will also push the non-dominate poles down in frequency and potentially closer together, and therefore at some point compromise the system stability.

$$H_2(s) = -g_{m5}R_{diff}\frac{(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_{pa}})(1+\frac{s}{\omega_{pb}})} \quad (5)$$

$$\omega_{pa} \approx \frac{1}{R_{diff}C_{gd1}} \quad (6)$$

$$\omega_{pb} \approx \frac{g_{m5}}{C_g} \quad (7)$$

$$\omega_z \approx \frac{2g_{m5}}{C_g} \quad (8)$$

$$Where: C_g = C_{gs3} + C_{gs2}; R_{diff} = r_{ds3}\|r_{ds5}$$

The resistors R_1 and R_2 bias Q1. Moreover they are used to set the gate voltage of Q4 and keep the transistor in saturation. The quiescent current in the differential stage should be minimized. By choosing W/L as mentioned for Q1 the output capacitor of this stage will mainly be the pass transistor gate capacitance, C_{g1}, which will be larger than the capacitances at the other nodes. The differential stage gain that is set mainly by the output resistance of transistors Q3 and Q5. Another aspect is the power supply rejection ratio which can be increased by using larger length for transistors Q2-Q5. The loop gain of the fast loop is defined by

$$L(s) \approx A_{OL}(s)\frac{R_2}{R_1+R_2} \quad (9)$$

When current step loads are applied, ringing can occur on the output of the regulator due to low phase margin of the loop response. Therefore it is desirable to keep the phase margin of $L(s)$ above 75 degrees at maximum expected load capacitance.

B. Principle of Operation of the Slow Loop

The role of the slow loop is to control the gate voltage of transistors Q2 and Q3 and thereby stabilize the DC level at V_{out}. A two stage operational amplifier (OpAmp) with Miller capacitor has been utilized for this function. The slow loop is designed to consume a low quiescent current and therefore will have low power consumption. Transistors Q11 to Q18 and the miller compensation capacitor constitute the OpAmp as can be seen in Fig. 2. The slow loop starts at the gate of Q12, then through the OpAmp, proceed from the gate to the drain of Q3 and then from the gate to the drain of Q1. In order not to degrade the frequency response of the fast loop, this OpAmp has a unity gain frequency approximately two decades below that of the fast loop, Therefore the dominate pole of the OpAmp was placed at a low frequency, at 100 Hz
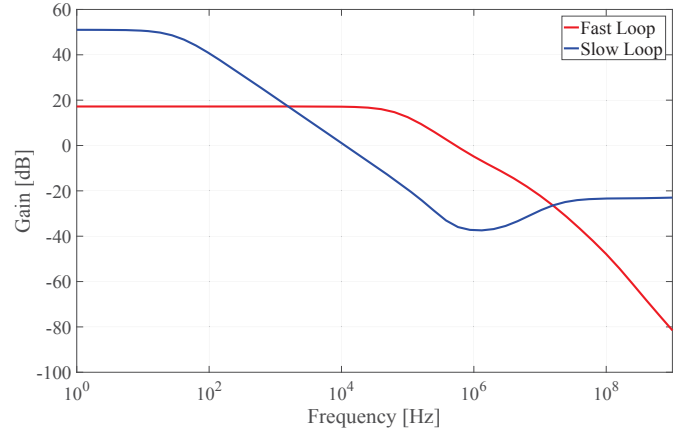

Figure 3. Simulated open loop frequency response of the slow and fast loops, without extracted parasitics. $C_L = 0$ and $I_L = 0$

as can be seen at Fig. 3. Moreover, the loop has to be stable to maintain the stable operation of the whole system.

When the steps in I_L occur the OpAmp must be able to drive the gate of Q2 and Q3 without slewing the transient. Therefore, the common source stage of the OpAmp must provide a sufficiently large drain current, I_{D16}. The required I_{D16} can be reduced by choosing a lower W/L for transistors Q2 and Q3 to reduce the parasitic capacitance related to the gate. When designing the OpAmp for the slow loop choosing trade-off are needed between the GBWP of the differential stage, V_{gs}, the transistor dimensions of Q2 and Q3 and the necessary I_{D16} to reduce slewing.

Table I
DEVICE DIMENSIONS AND DRAIN CURRENT

Device	Width [μm]	Length [μm]	I_Q [μA]	g_m [μA/V]
Q1	4000	0.18	1.0	6532
Q2,Q3	4	1	4.128	43.98
Q4,Q5	30	1	4.128	112.92
Q6	4	2	8.256	89.78
Q7	1	2	2.0	22.24
Q11,Q12	64	1	0.0157	0.445
Q13,Q14	2	8	0.0157	0.316
Q15	2	1	0.0315	0.855
Q16	64	1	1.021	27.8
Q17	32	1	1.021	23.46
Q18	64	1	1.021	27.04

The design compromises of the slow and fast loop discussed above lead to the device dimensions, quiescent currents and transconductance presented in Table I. The total quiescent current is 10.3 μA. A value of 4 pF was chosen for C_C.

III. SIMULATION RESULTS

The proposed capacitor-free LDO linear voltage regulator has been implemented in a 180 nm CMOS process. The presented results are based on the post layout simulation. The bias current in the CS stage was 1.0 μA, current of 8.256 μA was distributed at the differential stage and 1.05 μA to the
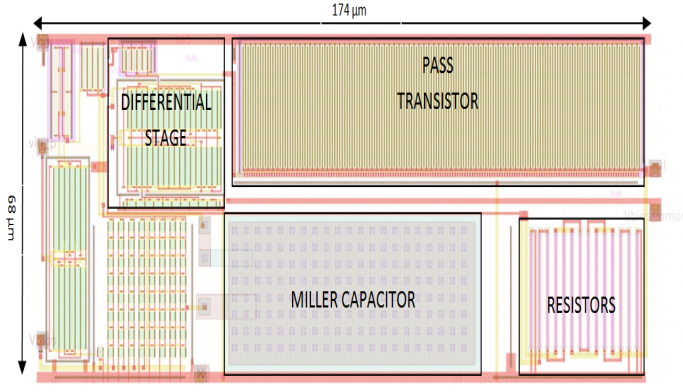
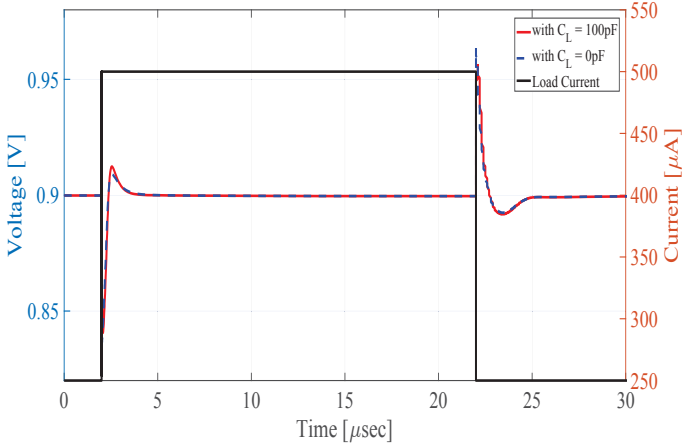Figure 4. Screenshot of the layout of the proposed LDO linear regulator

Figure 5. Post layout transient response simulation of the complete circuit

Figure 6. Power Supply Rejection Ratio

Figure 7. Transient response simulation of the complete circuit with different supply voltages

OpAmp, giving a total quiescent current consumption of 10.3 µA.

The layout is presented in Fig. 4 and has been designed with measures 174 µm x 68 µm. Common centroid matching and dummy devices have been used. The pass transistor Q1, differential stage, resistors and the compensating capacitor can be seen in the layout figure.

Post-layout simulation has been performed. Fig. 3 shows the open loop frequency response of the slow and fast loops at $C_L = 0$ and zero load current. The slow loop unity gain frequency is approximately two decades below that of the fast loop as we required. The PSRR is shown in Fig. 6, its dc values with and without the load capacitor is 63 dB at 1 kHz, under the typical case.

The transient response of the capacitor-free LDO voltage regulator for a current step of 0 - 250 µA with a rise and fall time of 1 ns is shown in Fig. 5. The simulation was preformed with and without C_L. ΔV_{out} without a load capacitance is 64 mV, while for $C_L = 100$ pF the spikes reach 56 mV. It should be noted that a smaller current step or lager edge time will decrease the spikes. Fig. 7 presents the transient analysis with different voltage supplies. The design was sent for fabrication, we expect to present result at the conference.
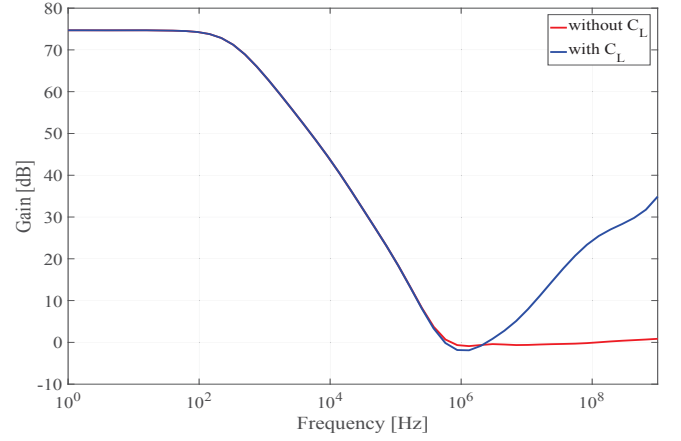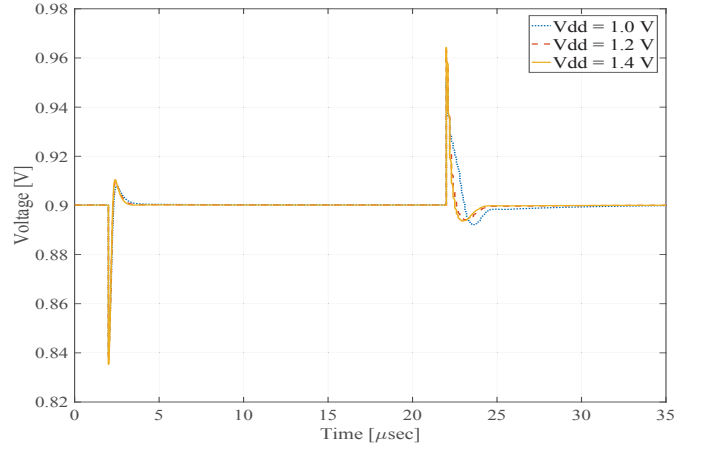
IV. PERFORMANCE COMPARISON

The presented theory and results of the proposed LDO linear voltage regulator show that external capacitor can be replaced by the design proposed. This design is suitable to supply low current to internal circuitry like needed in hearing aids. The design is simple to implement, with small area, which makes it ideal for a system-on chip. Simulations show good performance when compared with known capacitor-free topologies. For the purpose of comparison with other regulators we define a figure of merit (FOM) from [2]. This is used for standardized comparison in capacitor-free regulators as in the table. For this parameter, the smaller the FOM, the better the transient response of the regulator.

$$FOM = K \frac{\Delta V_{OUT,pp} I_Q}{\Delta I_{out}} \qquad (10)$$

Where, $\Delta V_{OUT,pp}$ is the sum of the undershoot and over-shoot and K is the edge time ratio which is defined by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{smallest } \Delta t \text{ among the designs for comparison}}$$

Table II
COMPARISON OF EXISTING WORK

	Units	[1]	[6]	[3]	[4]	[2]	[7]	[8]	[9]	This Work*
Year		2003	2007	2009	2010	2010	2013	2015	2016	2016
Technology	[μm]	0.6	0.35	0.35	0.35	0.09	0.11	0.18	0.5	0.18
V_{in}	[V]	1.5 - 4.5	3.0 - 4.2	1.8 - 4.5	0.95 - 1.4	0.75 - 1.2	1.8 - 3.8	1.4 - 1.8	2.3 - 5.5	1.0 - 1.4
V_{out}	[V]	1.3	2.8	1.6	0.7 - 1.2	0.5 - 1	1.2	1.2	1.2 - 5.4	0.9
I_{out}(max)	[mA]	100	50	100	100	100	200	100	150	0.5
$I_{quiescent}$	[μA]	38	65	20	43	8	41.5	141	40	10.3
$V_{dropout}$	[mV]	200	200	200	200	200	200	200	100	100
Undershoot	[mV]	120	90	78	70	73	385	110	96	64
Overshoot	[mV]	90	90	97	70	114	200	85	120	64
$\Delta V_{OUT,pp}$	[mV]	210	180	175	140	187	585	195	216	128
ΔI_{out}	[mA]	90	50	90	99	97	199.5	99.99	150	0.25
Settling time	[μs]	2	15	9	3	5	0.65	30	3	3
Compensation cap	[pF]	12	21	7	6	7	3.2	9	29	4
$Cout$	[pF]	10000	100	100	100	50	40	100	470	100
PSRR @ 1 kHz	[dB]	-60	-57	N/A	N/A	N/A	N/A	N/A	-57	-63
Edge time ΔT	[μs]	0.5	1	1	1	0.1	0.5	1	1	0.001
Edge time ratio K		500	1000	1000	1000	100	500	1000	1000	1
FOM	[mV]	44.33	234.0	38.89	60.81	1.54	60.85	274.9	57.6	5.27
Active Area	[mm^2]	0.307	0.12	0.145	0.16	0.019	0.11	0.07	0.279	0.012

* Post layout simulation results of this work is compared to the measurement results of the other designs

The unit of the FOM is volt as noted in Table II. The K factor depends on the designs considered for comparison, because the edge time of our work is the smallest, it K factor is equal to 1.

The performance comparison between the proposed design and some selected published LDOs is shown in Table II. The FOM of the proposed design when comparing to similar designs is the second lowest. Our design has the smallest chip area, with the second lowest quiescent current of 10.3 μA while the load capacitance can be as large as 100 pF. Not only does the proposed regulator consume low power, but it provides a low dropout voltage and fast settling time.

Table III present the results for the typical and worst case corners. Although the spikes and settling time has increased from the typical case the results are still quite similar.

Table III
SUMMARY OF $\Delta V_{OUT,pp}$, SETTLING TIME AND FOM UNDER TYPICAL
AND WORST CASE WITH C_L=0

Case	Typical	Worst
$\Delta V_{OUT,pp}$	128 mV	140 mV
Settling time	3 μs	4.5 μs
FOM	5.27 mV	5.768 mV

V. CONCLUSION

We have demonstrated a new capacitor-free low-dropout linear regulator for hearing aids in 180-nm CMOS technology. The structure, post layout simulation and performance comparing have been provided. The proposed regulator has proven a good transient performance. The internal compensating capacitor is as small as 4 pF and the chip total area is 0.012 mm^2. The LDO voltage regulator can operate with supply voltage between 1.0 - 1.4 V while having a quiescent current of 10.3 μA and small ΔV_{out} due to the two regulation loops. The achieved specification of the proposed LDO makes it suitable for hearing aids and similar SoC applications.

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