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A 10 MHz Bandwidth Continuous-Time Delta-Sigma Modulator for Portable Ultrasound Scanners

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Abstract—**A fourth-order 1-bit continuous-time delta-sigma modulator designed in a 65 nm process for portable ultrasound scanners is presented in this paper. The loop filter consists of RC-integrators, with programmable capacitor arrays and resistors, and the quantizer is implemented with a high-speed clocked comparator and a pull-down clocked latch. The feedback signal is generated with voltage DACs based on transmission gates. Using this implementation, a small and low-power solution required for portable ultrasound scanner applications is achieved. The modulator has a bandwidth of 10 MHz with an oversampling ratio of 16 leading to an operating frequency of 320 MHz. The design occupies an area of 0.0175 mm^2 and achieves a SNR of 45 dB consuming 489 µA at a supply voltage of 1.2 V; the resulting FoM is 197 fJ/conversion. The results are based on simulations with extracted parasitics including process and mismatch variations.**

I. INTRODUCTION

Ultrasound scanning is a widely used technique in medical applications due to its operating simplicity, non-invasive nature, live imaging capabilities and extended diagnosis range. However, the commonly used static ultrasound scanners are expensive, large and have no power consumption limitations since they are plugged into the AC mains. Due to its virtually unlimited supply power, the electronics of a static scanner are generic discrete components which are typically over-designed and consume a high amount of power for a handheld device.

In the last decade portable ultrasound scanners has emerged in the market and research on their implementation has increased since they suppose a price, size and power consumption reduction. There are several challenges in the design of a portable ultrasound scanner. Firstly, due to the reduced size, the maximum power dissipation on an ultrasound scanner is 2 W. Secondly, since the device is USB or battery supplied, the maximum power consumption of the electronics is limited, which obsoletes the usage of generic discrete components. An application specific integrated circuit (ASIC) solution is required to custom design the electronics and minimize the power consumption. Implementing the electronics using ASICs leads to the best signal-to-noise ratio for a specific power budget, which directly translates into the best picture quality achievable for that power budget.

An ultrasound scanner comprises several channels, and each of them consist of a transducer, a transmitting circuit (Tx) and a receiving circuit (Rx). The Tx excites the transducer with high-voltage signals in order to generate ultrasound waves. The Rx amplifies, delays and digitizes the signal induced in the transducer by the reflected waves. The most power consuming part of each channel is the Rx, and a large part of this power consumption comes from the analog-to-digital

SNR [dB]	BW [MHz]	OSR	V_{SS}/V_{DD} [V]	V_{cm} [V]	$V_{d,in}$ [V]
42	10	16	0 / 1.2	0.6	+/-0.6

converter (ADC). Consequently, the ADC design is a very critical part in order to achieve an overall power consumption reduction. The topology and specifications of the ADC depend on system level considerations.

In this paper the design and implementation of an integrated fully-differential continuous-time $\Delta\Sigma$ modulator (CTDSM) for a 64-channel portable ultrasound scanner based on capacitive micromachined ultrasonic transducers (CMUTs) is presented. Each channel contains one CTDSM with relaxed requirements due to the in-handle pre-beamforming of the scanner. The circuit is designed and implemented in a 65 nm process.

II. CTDSM TOPOLOGY AND SPECIFICATIONS

In [1] the 64-channel system based on CMUTs was studied and the most adequate topology and specifications were derived. A fourth-order 1-bit CTDSM with optimal zero placing topology was chosen. A summary of signal-to-noise ratio (SNR), bandwidth (BW), oversampling ratio (OSR), supply voltages (V_{SS}/V_{DD}), common mode level (V_{cm}) and maximum differential input voltage ($V_{d,in}$) is shown in Table I. The relaxed SNR requirements for the ADC is possible due to the in-handle pre-beamforming of the 64-channels.

Due to the low SNR of the specifications, the thermal noise was found to be negligible compared to the inherent quantization noise, which is rare in CTDSM design. Typically, the modulator is designed with a signal to quantization noise ratio (SQNR) 10-12 dB higher than the desired SNR in order to give margin for the thermal noise introduced by the circuitry and the non idealities. This limits the options, and sets some constrains on the design. In this paper, the thermal noise can be neglected which, as it is can be seen later, affects significantly the design choices and implementation of the CTDSM.

The block level structure of the CTDSM designed is shown in Fig. 1. The signal is modulated with four RC-integrators based on an operational transconductance amplifier (OTA). The integrators are grouped in pairs in order to create two resonators which optimally place two zeros in the transfer function to improve the SNR. The quantizer is implemented with a high-speed clocked comparator and a pull-down clocked latch. The feedback signal is generated with voltage digital-to-analog converters (DACs).
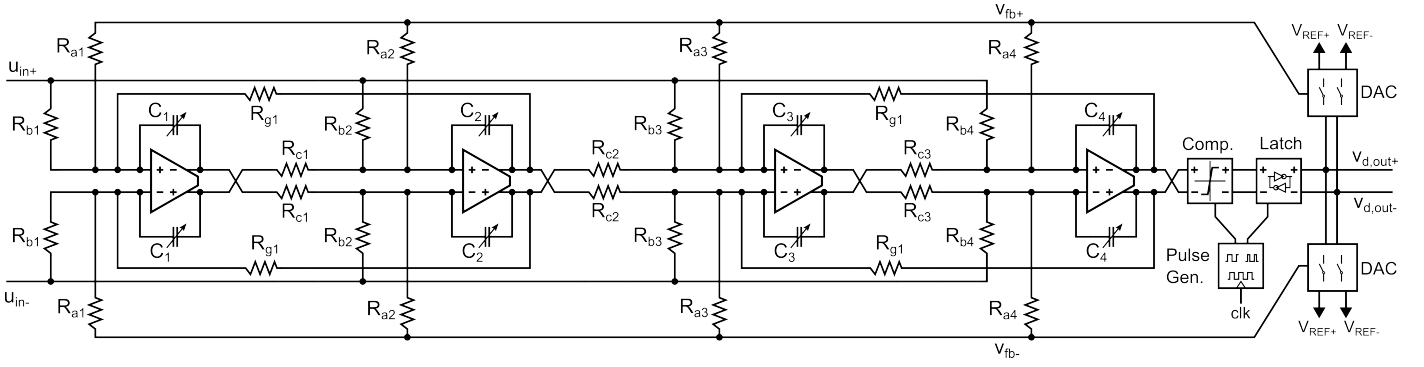
Fig. 1. Structure of the fourth-order 1-bit continuous-time $\Delta\Sigma$ modulator with two resonators for optimal zero placing.

III. Block design

In this section, the design of each block of the CTDSM is shown. In each subsection, the specifications, topology and design choices of the block are discussed. The main target of the circuitry is to lower the power consumption and area, hence all the blocks are designed to fit that target. Note that in all schematics the bulks of the PMOS and NMOS transistors are connected to the positive supply (V_{DD}) and negative supply (V_{SS}) respectively if it is not indicated otherwise.

A. Operational Transconductance Amplifier

The specifications for the OTA are a gain of (A_v) 40 dB, a gain-bandwidth of (GBW) 1.32 GHz, phase margin of (PM) 35° and a slew rate of (SR) 120 V/µs. The load of the OTA is the integrating capacitor of 100 fF. The most limiting factor is the GBW and it needs to be achieved with the minimum current possible. The symmetrical OTA topology shown in Fig. 2 has a very high current-to-GBW ratio, and since it is perfectly symmetrical it has good matching, low offset and high output swing. Cascoded transistors M_{8a}/M_{8b} and M_{9a}/M_{9b} had to be added to boost the gain. The main disadvantage of symmetrical OTAs is the high levels of thermal noise, however, as it was stated before, due to the low SNR required, the thermal noise is not a limiting factor. The bias current in the inner branch is generated by M_6 and is mirrored five times larger with the current mirror formed by M_{2a}/M_{2b} and M_{3a}/M_{3b}. The common-mode feedback (CMFB) consists of M_{4a}/M_{4b} and M_5, which detect the output level and adjust the current in the outer branches to compensate it. The OTA was simulated in
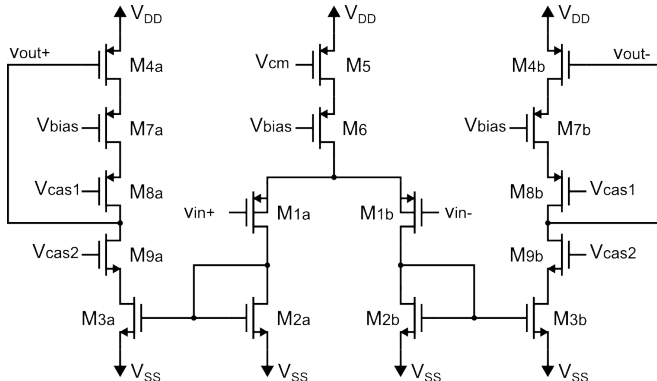
TABLE II. SYMMETRICAL OTA PERFORMANCE

	A_v [dB]	GBW [GHz]	PM [°]	SR [V/µs]
Nom.	46.3	1.41	40.6	267
Min.	45.9	1.35	39.5	256
Max.	46.6	1.44	41.6	277

the corners including mismatch and the performance obtained is shown in Table II. The nominal value (in the typical corner) and the maximum and minimum value across all the corners and mismatch simulations are noted. All the specifications are satisfied even in the worst case of each parameter.

B. Programmable capacitor array

Due to process corners and other variations, the value of the resistors and capacitors can range up to +/-20%, therefore the coefficients of the modulator, which depend inversely on the RC product can highly vary. In order to compensate for these variations, the integrating capacitors are implemented as programmable capacitor array so that the capacitance value can be adjusted. The schematic of the array can be seen in Fig. 3. The bits b_n control whether the corresponding capacitor C_n is connected to the input/output of the OTA or if it is disconnected and shorted to ground. In this design three control bits (n = 1,2,3) are used, leading to eight possible capacitor values combining C_0, C_1, C_2 and C_3. The extra control bit, rst, works as a reset signal of the CTDSM by shorting the input/output of the OTAs.

C. High-speed clocked comparator

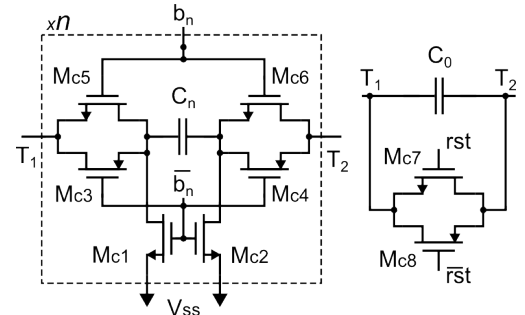Sampling frequency of the modulator is 320 MHz therefore a very fast comparator is needed. Furthermore, in order to

Fig. 2. Symmetrical OTA schematic with cascodes and CMFB.

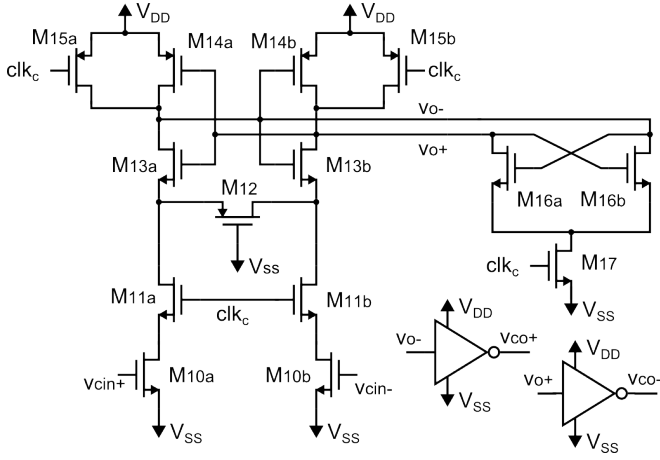Fig. 3. Capacitor array schematic. In this design n = 3.

Fig. 4. Comparator schematic.

Fig. 5. Latch schematic.

get consistent comparisons with the same starting state, the comparator needs to be reset every cycle. The topology used is the one suggested in [2], and it is shown in Fig. 4. The comparator has two different phases. Firstly, when the clock clk_c is low, the comparator is disabled and both outputs v_{o+} and v_{o-} are pulled up to V_{DD}. Secondly, when clk_c is high, the starting state of the comparator is unstable since both v_{o+} and v_{o-} are high. A small differential signal in the input pair of the comparator, M_{10a}/M_{10b} will pull down either v_{o+} or v_{o-} through the two positive feedback paths formed by M_{13a}/M_{13b} and M_{16a}/M_{16b}. M_{14a}/M_{14b} are sized significantly bigger than the rest of the transistors so that once the circuit is flipped to one side, the input signal can not change the state allowing only one comparison per reset cycle. Two inverters are added at the outputs of the comparator so that the v_{o+} and v_{o-} are equally loaded. Consequently, the consistency and symmetry of the output signals of the comparator is increased.

D. Pull-down clocked latch

Even though the comparator is symmetric and equally loaded, the input amplitude of its differential input signal determines the comparison time. The comparator takes more time to compare small differential signals, and is quicker at deciding for larger differential signals. This would create inconsistencies in the feedback signals of the modulator, which would decrease its SNR, hence a pull-down clocked latch is needed. The latch provides a time consistent output independently of the comparator behavior. Firstly, clk_c enables the comparator and after a decision time, clk_l enables the latch passing the comparator decision to the outputs of the CTDSM $v_{d,out+}$ and $v_{d,out-}$. The outputs are consistently generated on the rising edge of clk_l, hence any effects of the differential input of the comparator are effectively neutralized.

The schematic of the pull-down clocked latch can be seen in Fig. 5. It consists of a latch formed by M_{20a}/M_{20b} and M_{21a}/M_{21b} and two pull down branches composed of M_{18a}/M_{18b} and M_{19a}/M_{19b}. When the clock clk_l is low, both branches are disconnected, and the latch maintains its state. When clk_l is high, one of the branches pulls down one of the nodes of the latch forcing a state. The pulling strength of both branches is consistent every cycle since v_{co+} and v_{co-} are always either V_{DD} or V_{SS} when the latch is enabled.
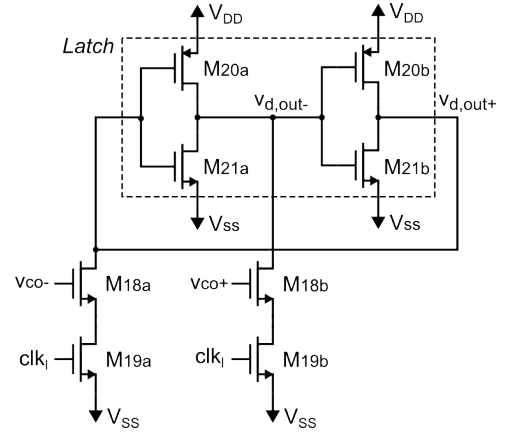
E. Pulse generator

In order to control both the comparator and the latch the enabling pulses clk_c and clk_l need to be generated. There are three states per cycle, the comparison time (t_c), the latch time (t_l) and the reset time (t_r). In t_c, only the comparator is enabled. During t_l, both the comparator and latch are enabled. Finally, in t_r, both comparator and latch are disabled. It is important to notice that the comparator can stay enabled during the latch time since M_{14a}/M_{14b} are designed to be very strong, hence the comparator inputs can not flip its output. This allows for a way simpler and more robust control scheme where it is not critical to turn off the comparator before the output is latched. The pulse generator is implemented with a simple inverter delay line, an AND gate and some control transmission gates generating clk_c and clk_l. This simple design is low in current consumption and resistant to process and mismatch variations since, even though t_c, t_l and t_r can vary, these states can not overlap due to its inherent structure.

The loop delay of this CDTSM is largely dominated by t_c, which comes determined by the delay of the inverters and the AND gate. The layout of this block affects the unit delay of an inverter, therefore all the timing simulations need to be done with extracted parasitics. Following the specifications found in [1], the loop delay can not be higher than 300 ps. Simulations with extracted parastics including corners and mismatch variations show that the total loop delay vary from 210 ps to 298 ps with a nominal value of 252 ps.

F. Voltage feedback DAC

The two DACs of the system are chosen to be implemented as simple voltage DACs for simplicity, easiness of matching and area reduction. They consist of a PMOS and NMOS connected as a transmission gate that connect the feedback nodes v_{fb+} / v_{fb-} to either V_{REF+} (1.1 V) or V_{REF-} (0.1 V) depending on the gate signals $v_{d,out+}$ and $v_{d,out-}$ (see Fig. 1). These transmission gates need to be fast, therefore small transistors should be used. Furthermore, in order to obtain consistent, symmetric feedback pulses, both DACs should have a good matching, hence several minimum size unit transistors are used in each MOSFET device.

IV. CTDSM PERFORMANCE AND DISCUSSION

After the assembly of all the blocks, the layout of the full CTDSM, with a total area of $0.0175\,\text{mm}^2$ is shown in Fig. 6. The area distribution is as follows: OTAs, including its bias circuit, occupy $3100\,\mu\text{m}^2$ (17.7%), the capacitor arrays $7600\,\mu\text{m}^2$ (43.4%), the resistors $6300\,\mu\text{m}^2$ (36%), and the comparator, latch, pulse generator and DACs combined occupy $500\,\mu\text{m}^2$ (2.9%). It can be seen that the majority of the area is occupied by the loop filter (OTAs, capacitor array and resistors), and the area of the quantizer (comparator, latch and pulse generator) and DACs are significantly smaller.

The performance of the full CTDSM with extracted parasitics is shown in Fig. 7. Small integrating capacitors were chosen to lower power consumption, which lead to large noisy resistors, and minimum current was used in the OTAs, which leads to the worst case for thermal noise. However, as it can be seen in Fig. 7, the circuit is still inherently dominated by quantization noise which is very uncommon in CTDSM design. Due to the low impact of the thermal noise, all the tradeoffs of the design have been biased towards low current consumption instead of noise performance.

The nominal SNR and current consumption simulated with extracted parasitics are $45\,\text{dB}$ and $489\,\mu\text{A}$ respectively, and even across the corners, the design falls within specifications. From the total current, $443\,\mu\text{A}$ are spent on the OTAs (90.6%), $22\,\mu\text{A}$ are spent on the quantizer (4.5%) and $24\,\mu\text{A}$ are spent in the DACs (4.9%). The current consumption is clearly dominated by the loop filter, mainly in the OTAs. The supply voltage is $1.2\,\text{V}$, hence the power consumption of the CTDSM results in $0.587\,\text{mW}$. The CTDSM has been sent to fabrication in a $65\,\text{nm}$ process and it has been recently received. Preliminary measurements on the integrated circuit suggest promising results. Further complete measurements will be done in order to test the performance of the CTDSM and the results will be shown at the conference.

For the purpose of comparing the design with other converters, the commonly used figure of merit (FoM) of energy per conversion is used (1). Using the results of the simulated performance with parasitic extraction, the calculated FoM of the design is 197 fJ/conversion. A performance comparison between this design and other CTDSM with similar specifications is shown in Table III. As it can be seen, this design achieves a comparatively low FoM using a very small die area and
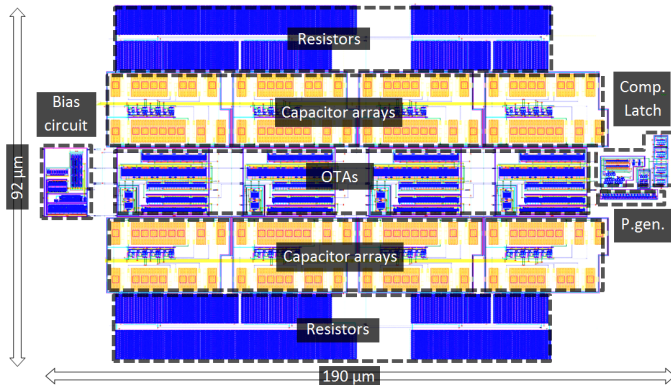
TABLE III.   CTDSM COMPARISON

	This work	[3]	[4]	[5]	[6]	[7]
SNR [dB]	45	54.5	44	64.5	67.9	70
BW [MHz]	10	5	20	20	10	10
Fs [MHz]	320	200	522	640	320	300
Area [mm²]	0.0175	-	-	0.072	0.39	0.051
Power [mW]	0.587	3.4	11.6	11	4.8	2.57
FoM [fJ/c.]	197	360	1900	225	230	50

low power consumption which enables channel scalability, a necessary factor for portable ultrasound scanners.

$$FoM = \frac{P}{2 \cdot BW \cdot 2^{\frac{SNR-1.76dB}{6.02dB}}} \qquad (1)$$

In order to put in perspective the power consumption of the CTDSM in the total power budget of the portable ultrasound scanner the full system is considered. A 64-channel portable ultrasound scanner, containing 64 ADCs, has an approximate power budget of $2\,\text{W}$. Using 64 of the designed CTDSM, only a power consumption of $37.6\,\text{mW}$, which correspond to a 1.9% of the total budget would be needed.

V. CONCLUSIONS

In this paper a fourth-order 1-bit continuous-time $\Delta\Sigma$ modulator designed in a $65\,\text{nm}$ process for portable ultrasound scanners is presented. The modulator has a BW of $10\,\text{MHz}$, an OSR of 16 and optimal zero placing. The aim of the design is to minimize the power consumption and area of the design because of the power budget and size of a portable ultrasound scanner. Due to the low SNR specifications, the design is inherently dominated by quantization noise, which is very uncommon for CTDSM. OTA based RC-integrators are used, and the quantizer is composed of a high-speed clocked comparator and a pull-down clocked latch which are both controlled by a clock generator. Voltage DACs are utilized for the feedback paths. The design is robust to process and mismatch variations and it occupies a die area of $0.0175\,\text{mm}^2$. The simulated SNR and power consumption with extracted parasitics obtained are $45\,\text{dB}$ and $489\,\mu\text{A}$ for a $1.2\,\text{V}$ supply; the resulting FoM is 197 fJ/conversion. The modulator has been sent to fabrication and measurements will be performed on the packaged die to assess its performance.
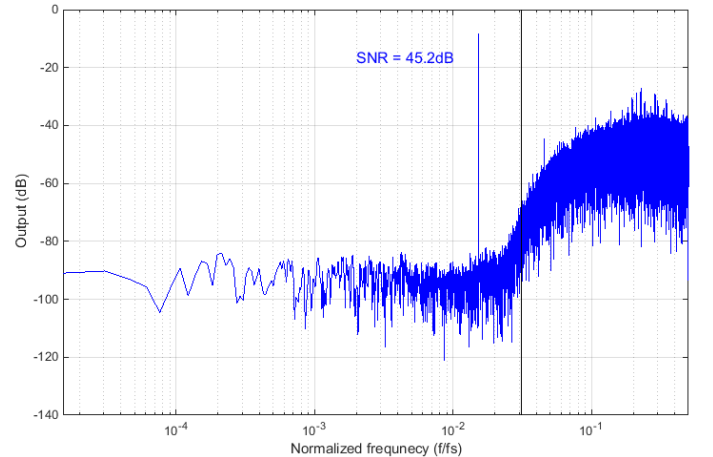
Fig. 6.   Layout of the CTDSM designed.

Fig. 7.   Simulated FFT of the output of the CTDSM with extracted parasitics.

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