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# Novel Clocking Scheme with Improved Voltage Gain for a Two-Phase Charge Pump Topology

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Abstract—This paper presents a novel clocking scheme for the Favrat charge pump topology. The proposed clock scheme achieves an 8 % higher maximum power output and a 12 % higher maximum output voltage than the prior-art clock scheme. The novel clock scheme is part of the development of a very high voltage charge pump for MEMS applications. In this work a 46stage charge pump based on the Favrat charge pump topology has been fabricated in a 180-nm SOI process with a > 200 V breakdown voltage. With an input voltage of 5 V the fabricated charge pump reach an output voltage of 185 V when driven by the proposed clock scheme can only reach an output voltage of 165 V with a 2 nA load.

#### I. INTRODUCTION

Micro Electro-Mechanical Systems (MEMS) can be found in applications used by most people every day, applications such as sensors, projectors, and radio-frequency communication. Especially the use of MEMS based sensors is wide-spread as these sensors are extensively used in mobile electronics and cars.

One topic of research in the field of MEMS is micromanipulation where MEMS motors, actuators, and grippers are used to handle microparticles and fluids. Examples of microparticles are cells and bacteria. MEMS based motors are commonly driven by an actuator as they are easy to implement in a MEMS module. A popular way of achieving actuation is using comb-drives where electrostatic force is used to actuate a MEMS structure [1]. The comb-drives usually require a high driving voltage to generate the required force. The driving voltage for comb drives are usually in the range of 10s to 100s of volts dependent on the application [1], [2], [3].

Comb-drives behave as a capacitive load and usually have a very small leakage current. Because the comb-drives behave as a capacitive load they do not require a large static driving current. The capacitive behaviour of the comb-drives makes it necessary to use a bi-directional driver if it is desired that the voltage on the drive, and thereby the force exerted by the drive, is lowered.

Reducing the cost of MEMS based microgrippers and other mechanical structures will aid with commercialization and enable a more widespread use of micro-manipulation MEMS modules.

MEMS sensors are often developed with all the necessary assisting electronics such as drivers and read-out circuits, microgripper modules however, are typically developed with only a read-out circuit [1], [2], [3] as it is non-trivial to implement a low to High-Voltage (HV) converter in a small Application Specific Integrated Circuit (ASIC). If the high voltage required to drive the MEMS comb-drives could be generated by a circuit in a small ASIC it would help with reducing the price and implementation complexity of MEMS microgripper modules.

Multiple approaches for low to high voltage conversion exists. For example inductor based boost converters, piezoelectric transformers, and charge pumps. But out of all those, only the charge pump approach is suitable for full implementation in an ASIC. It is possible to implement the other converters in an ASIC but for good performance it would require advanced process technologies to achieve good quality factor inductors or have Piezo material implemented into the ASIC.

Generating a high voltage in an ASIC is limited by the breakdown voltage of the process technology. Multiple approaches to design around the N- and P-well breakdown voltages in CMOS processes exist. One approach is to use devices that can be implemented on top of the field oxide as the field oxide has a high breakdown voltage [4], another approach is to use multiple ASICs [5]. It is also possible to use processes that are designed for HV applications such as Silicon On Insulator (SOI) processes which has been the approach in [6], [7], [8].

In this work a 46-stage charge pump consisting of cascaded Favrat charge pump [9] topologies was fabricated in a 180nm SOI process. The intended application for the developed charge pump is to drive a MEMS comb-drive with a voltage of up to 180 V. The leakage in the comb-drive is conservatively estimated to be 2 nA.

The Favrat charge pump topology was chosen due to its linear scaling, low voltage stress on transistors, and a voltage gain per stage that is better compared to the Dickson charge pump [10]. The Favrat topology is similar to the Pelliconi charge pump topology [11] but it has fewer challenges with keeping the parasitic bi-polars in an off-state.

The remainder of this paper is organized as follows. Section II gives a short presentation of the implemented charge pump. The proposed clock scheme is presented together with an analysis of the reverse currents in the Favrat charge pump



Fig. 1. Two cascaded Favrat charge pump stages.

topology in section III. Section IV presents measurement results of the fabricated charge pump driven by different clock schemes and compare the results with simulations, finally the conclusion is presented in section V.

#### **II. CHARGE PUMP IMPLEMENTATION**

The 46-stage charge pump of this work consist of cascaded Favrat charge pump stages; a depiction of two cascaded stages are shown in Fig. 1. The charge pump capacitors  $C_1$ - $C_4$  and  $C_{bias}$  are in this work implemented as 300 fF HV metal-insulator-metal capacitors. Due to the small capacitance the voltage gain per stage is very sensitive to parasitic capacitances.

The transistors in the implemented charge pump are all implemented with minimum width and minimum length (W/L = 220 nm / 500 nm) as larger transistors reduce the charge pump voltage gain. The voltage gain is reduced by increased transistors sizes due to increased parasitic capacitance and the increased reverse currents during clock transitions.

On the fabricated ASIC the output of the charge pump is filtered by the low-pass filter shown in Fig. 2 to reduce the ripple at the output voltage for the MEMS module. The capacitors  $C_5$ ,  $C_6$ , and  $C_7$  are respectively 1.7 pF, 6.9 pF, and 14.8 pF. The simulated -3 dB cutoff frequency when settled, with parasitic extraction capacitances included, is 0.052 Hz.

The described charge pump was implemented in two versions, one without and one with an integrated clock generator. A die photo of the fabricated charge pumps is shown in Fig. 3 with the charge pumps and low-pass filters high-lighted. The area of each charge pump is 0.260 mm<sup>2</sup>, the area of each filter



Fig. 2. Topology of output filter.

is 0.145 mm<sup>2</sup>, and the clock generator had an area of 0.004 mm<sup>2</sup>.

#### III. PROPOSED CLOCK SCHEME

In prior-art [12], [9], [13] the Favrat charge pump is driven by two non-overlapping clocks which leads to significant reverse currents. We propose to use a crossing clock scheme as this reduce the reverse currents and thereby achieve a higher voltage gain and output power capability.

The most significant reverse current paths in the Favrat topology are highlighted as the paths  $I_1$ - $I_4$  in Fig. 1. These reverse currents are the most significant for both the non-overlapping and crossing clock schemes. The relative magni-



Fig. 3. Die photograph of the fabricated charge pump and output filter.

tude of the reverse currents in Fig. 1 with the different clock schemes are depicted in Fig. 4.

For the non-overlapping clock scheme the causes for the reverse currents with reference to Fig. 1 and Fig. 4a are:

- Phase A:
  - The charge pump has settled and charge is no longer being transferred
  - $V_2 = V_3 = V_{bulk,1}$
  - $M_4$ ,  $M_6$ , and  $M_7$  are saturated and ON as  $V_1 < V_2$ and  $V_4 > V_3$
- Phase B:
  - $\varphi_2$  transitioning towards 0 lowers  $V_2$  leading to  $V_2 < V_3$  and  $V_2 < V_{bulk,1}$
  - $M_4$ ,  $M_6$ , and  $M_7$  are still saturated and ON
  - The current  $I_3$  is running from  $C_3$  to  $C_2$
  - The current  $I_2$  is running from  $C_{bulk,1}$  to  $C_2$
- Phase C:
  - As  $\varphi_2$  approaches 0,  $M_3$  and  $M_5$  are becoming saturated as their gate voltage  $V_2$  is lowered and currents  $I_1$  and  $I_4$  become non-zero
  - $M_7$  is entering its cut-off region, hence  $I_3 \rightarrow 0$
- Phase D:
  - $\varphi_1$  is transitioning to  $V_{dd}$
  - $\varphi_2$  is 0,  $M_7$  is OFF, and the current  $I_3$  is 0
  - The increasing  $\varphi_1$  is turning off  $M_6$ , and  $M_4$ , hence  $I_2 \rightarrow 0$
  - As  $\varphi_1 \rightarrow V_{dd}$ ,  $V_1$  becomes larger than  $V_4$  and  $V_{bulk,1}$  leading to forward currents in the charge pump
- Phase E:
  - Charge is being transferred from  $C_1$  to  $C_4$  and to  $C_{bulk,1}$
  - After enough time the charge pump will reach equilibrium leading to  $V_1 = V_4 = V_{bulk,1}$

All in all the reverse currents occurring during the phases described above results in a reduced voltage gain of the charge pump.

For the crossing clock scheme the causes for the reverse currents are more or less the same, the duration and magnitude of the reverse currents, however, are significantly different though and with a smaller sum. See Fig. 4b. With crossing clocks,  $\varphi_1$  transition towards  $V_{dd}$  earlier, compared to the non-overlapping clock scheme, hence  $M_4$  and  $M_6$  enter their cut-off region earlier; this reduces the duration of  $I_2$  and  $I_3$ ; the magnitude of  $I_2$  is also smaller as  $M_6$  does not reach full saturation. For the crossing clock scheme  $I_3$  has a higher magnitude as the increasing  $\varphi_1$  increases  $V_3$  while the decreasing  $\varphi_2$  decreases  $V_2$  leading to a larger potential difference between  $V_3$  and  $V_2$  thereby causing a larger current  $I_3$ .

The reverse current  $I_1$  is also reduced as there is less time where  $M_5$  is saturated and  $V_1 < V_{bulk,1}$ .

The reverse current  $I_4$  is increased in magnitude as the increasing  $\varphi_1$  saturate  $M_8$  while the decreasing  $\varphi_2$  saturate  $M_3$  leading to better conduction from  $C_4$  to  $C_1$ . The duration of the reverse current  $I_4$  is reduced as the voltage on  $V_1$  is close to be larger than  $V_4$  by the time  $M_3$  and  $M_8$  are saturated.

Visually comparing the area under the curves for the reverse currents,  $I_1$ - $I_4$ , in the plot of Fig. 4 indicate that the crossing clock scheme should achieve less net reverse currents and hence be able to achieve a higher voltage gain and output power capability; as there would be a reduced amount of charge transfer losses.

If an overlapping clock scheme were to be used, reverse currents similar to those in Fig. 4a would occur but the causes for reverse currents would be slightly different. We will not go through this in detail but from measurements it can be observed that the output voltage with the overlapping clock scheme is similar to the output voltage of the non-overlapping clock scheme.

# IV. RESULTS

#### A. Measurement setup

For measurements, the fabricated charge pump was driven by a two-channel function generator (Keysight 33622A) with a 50  $\Omega$  load near the pins of the packaged ASIC; the rise and fall time of the clock signals are 5 ns; unless otherwise specified the clock signals used for the measurements has a 5 V swing and a frequency of 2 MHz. The output of the charge pump was loaded with 2 nA by a source-meter (Keithley 2450); the source-meter was also used to measure the output voltage of the charge pump. An oscilloscope (Rigol DS4024) was used to verify the waveforms of the clock signals fed to the charge pump. A picture of the measurement setup is shown in Fig. 5 and measurements of the two clock signals at 2 MHz and different amounts of overlap (also presented in terms of duty cycles) are presented in Fig. 6.

The fabricated charge pump was bonded in a ceramic package with very low leakage. The measured leakage in the



Fig. 4. Principal plot of reverse currents in the Favrat charge pump when driven by non-overlapping and crossing clocks.



Fig. 5. Picture of measurement setup.

package is less than 20 pA at a potential difference of 200 V between pins.



(a) Non-overlapping clock with  $t_{overlap}$ =0.0 ns (49 % duty-cycle for a 2 MHz clock)



(b) Crossing clock with  $t_{overlap}$ =2.5 ns (50 % duty-cycle for a 2 MHz clock)



(c) Overlapping clock with  $t_{overlap}$ =5.0 ns (51 % duty-cycle for a 2 MHz clock)

Fig. 6. Measured waveforms of clock signals @ 2 MHz fed to the fabricated charge pump. The rail-to-rail voltage is 5 V and the rise/fall time is 5 ns.

# B. Output Voltage vs Clocking Scheme

For measurements 3 dies with the charge pump were bonded and used for measurement of the charge pump output voltage at different clock schemes; for the rest of the measurements the a single bonded charge pump was used.

In Fig. 7 the charge pump output voltage is plotted as a function of duty cycle; The 49 % duty cycle correspond to non-overlapping clock signals, 50 % to crossing clocks, and 51 % to overlapping clocks; this is also depicted in Fig. 6.

As it can be observed from Fig. 7 the output voltage is very



Fig. 7. Measured charge pump output voltage versus clock duty cycle for the three bonded charge pumps.

dependent on the clock scheme, where the crossing clocks (@ 50 % duty cycle) achieve an output voltage of 185 V versus the 165 V and 161 V at respectively 49 % and 51 % duty cycle. This was the same for all three charge pumps.

# C. Output Voltage vs Clock Frequency

The output voltage at different duty cycles was also measured at different clock frequencies; the measurement results are shown in Fig. 8 and Fig. 9.

The plot in Fig. 8 show a difference based on the clock frequency, however, this is due to 49 % duty cycle of a 1 MHz clock result in a wider gap between the two non-overlapping clock signals than if it was a 2 MHz clock signal. For a 1 MHz clock, 1 % of the duty cycle equals 10 ns, for a 2 MHz clock, 1 % of the duty cycle equals 5 ns. The measurements in Fig. 8 are also presented in Fig. 9 but with output voltage as a function of the amount of overlap. From the plot in Fig. 9 it can be observed that the performance of the proposed clock scheme does not depend on the clock frequency only the overlap.

## D. Impact of Pumping Voltage

The benefit of using the crossing clock scheme is affected by the supply voltage as it can be observed in Fig. 10 where the charge pump voltage gain at different supply voltages is plotted, however, the crossing clock scheme still achieve a higher output voltage than the overlapping and non-overlapping clock schemes.

# E. Output Power vs Clocking Scheme

The crossing clock scheme is not only able to deliver a higher output voltage but also a higher output power. Observing the output power curve in Fig 11 it can be observed that a charge pump driven with crossing clocks has a peak output power that is around 8-12 % higher than the peak power output of the other clock schemes.



Fig. 8. Measured charge pump output voltage versus clock duty cycle for different frequencies.



Fig. 9. Measured charge pump output voltage versus clock overlap for different frequencies.

#### F. Comparison with Simulation

In Table I the measured and simulated (with all extracted parasitic capacitances included) output voltages for the three clock schemes are listed together. A significant difference in output voltage between simulation and measurements is observable, but, percentagewise the performance of the crossing clock scheme compared to the overlapping and nonoverlapping clock schemes is similar.

In the measurements the crossing clock scheme yield an output voltage that is 14.5 % higher than when the charge pump is driven by overlapping clocks, in simulation the number is 14.0 %. For the crossing clocks versus non-overlapping clocks the percentages are 12.0 % for measurements and 9.5 % for simulations.

The significant difference in output voltage between measurements and simulations are most likely caused by non-



Fig. 10. Measured charge pump voltage gain versus clock duty cycle at different clock voltage swings.



Fig. 11. Measured charge pump output power versus output voltage for the three clock schemes.

perfect modelling of parasitic capacitances as the fabricated charge pump is very sensitive to parasitics due to the use of minimum sized components.

### G. Measurement Summary

A summary of the charge pump specifications with the different clock schemes is listed in Table II together with the specifications for a charge pump version with a fully integrated crossing clock generator. The specifications are listed for a clock voltage of 5 V, a clock frequency of 2 MHz, and a load of 2 nA for the peak output voltage.

#### V. CONCLUSION

In this paper a novel clock scheme was proposed for the Favrat charge pump topology. The proposed clock scheme of using crossing clocks achieve a 12 % higher output voltage and

TABLE I Measured and Simulated Output Voltages

	Measured	Simulated
Clock scheme	output voltage [V]	output voltage [V]
Overlapping	161.5	175.6
Crossing	184.9	200.2
Non-overlapping	165.1	182.8

 TABLE II

 Charge Pump Specifications for Different Clock Schemes

	Peak	Peak
Clock scheme	output voltage [V]	Peak output power [µW]
Overlapping	161.5	202.2
Crossing	184.9	226.9
Non-overlapping	165.1	209.3
Integrated clock gen.	182.5	243.0

a 8 % higher peak output power than the prior-art approach of using non-overlapping clocks to drive the charge pump. The performance of the proposed clock scheme was verified through measurements on a 46-stage charge pump that was fabricated in a 180-nm SOI process. The performance of the charge pump driven by overlapping clocks was also measured and the overlapping clock scheme led to a worse performance than both the crossing and non-overlapping clock schemes.

#### REFERENCES

- M. Boudaoud, Y. Haddab, and Y. L. Gorrec, "Modelling of a MEMSbased microgripper : application to dexterous micromanipulation," *IEEE International Conference on Intelligent Robots and Systems*, pp. 5634 -5639, 2010.
- [2] B. Kim, J. S. Park, C. Moon, G. M. Jeong, and H. S. Ahn, "A precision robot system with modular actuators and MEMS micro gripper for micro system assembly," *Journal of Mechanical Science and Technology*, vol. 22, no. 1, pp. 70-76, 2008.
- [3] Femtotools, "FT-G102 Force Sensing Microgripper," accessed at http://www.femtotools.com/fileadmin/datasheets/FT-G102\_Datasheet.pdf on 26th of April 2019.
- [4] M. D. Ker, and S. L. Chen, "On-Chip High-Voltage Charge Pump Circuit in Standard CMOS Processes With Polysilicon Diodes," *IEEE Asian Solid-state Circuits Conference*, pp. 157-160, 2005.
- [5] I. Yousr, 2015, "High-Voltage Generation and Drive in Low-Voltage CMOS Technology," *PhD Dissertation*, available: https://escholarship.org/uc/item/7g1014zm.
- [6] Y. Okamoto et al., "On-Chip High-Voltage Charge Pump With MEMS Post-Processed Standard 5-V CMOS on SOI for Electroosmotic Flow Micropumps," *IEEE Electron Device Letters*, vol. 39, no. 6., pp. 851-854, 2018.
- [7] M. B. Saif, C. Hofmann, and Y. Xu, "Comparison of Charge Pump and Boost Circuits for High Voltage and Low Power Voltage Conversions," 58th International Symposium ELMAR, 2016.
- [8] M. R. Hoque, T. Ahmad, T. McNutt, A. Mantooth, and M. M. Mojarradi, "Design Technique of an On-Chip, High-Voltage Charge Pump in SOI," *IEEE International Symposium on Circuits and Systems*, 2005.
- [9] P. Favrat, P. Deval, and M. J. Declercq, "A New High Efficiency CMOS Voltage Doubler," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 410-416, 1997.
- [10] M. L. S. Mi et al., "Review of Charge Pump Topologeis for Micro Energy Harvesting Systems," *American Journal of Applied Sciences*, vol. 13, no. 5, pp. 628-645, 2016.
- [11] R. Pelliconi et al., "Power efficient charge pump in deep submicron standard CMOS technology," *European Solid-state Circuits Conference*, vol. 38, no. 6, pp. 1068-1071, 2001.

- [12] A. H. Alameh, and F. Nabki, "A 0.13-um CMOS Dynamically Reconfigurable Charge Pump for Electrostatic MEMS Actuation," *IEEE Transactions on VLSI Systems*, vol. 25, no. 4, pp. 1261-1270, 2016.
  [13] A. H. Hassan et al., "A VCO-Based MPPT Circuit for Low-Voltage Energy Harvesters," *IEEE Computer Society Annual Symposium on VLSI*, 2017.