

Reliability and Cell-to-Cell Variability of TAS-MRAM arrays under cycling conditions

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Abstract—The impact of 500k write cycles on 1kbits TAS-MRAM arrays has been evaluated by extracting a set of characteristic parameters describing the technology in terms of cell-to-cell variability and switching reliability. The relationship between switching voltages and cell resistances has been investigated in order to define the most reliable working conditions.

I. INTRODUCTION

Magnetic Random Access Memories (MRAM) are one of the most promising candidates to replace traditional Flash in future non-volatile memories generations [1], [2]. Among the MRAM paradigms that are under investigation, the Thermally Assisted Switching represents a good candidate for a replacement of the standard flash memories in embedded environments [3]–[5]. The information storage mechanism is based on the current-induced magnetization switch of a magnetic material [6], [7]: dependently on the imposed field direction with respect to that of a reference layer, a defined resistance of the material can be achieved. Such a technology is already at an intermediate maturity level, that calls for the evaluation of its potentialities at an integrated array level. Many experimental works [8], [9] still show the good performances of single cells structures, whereas only few analyze the behavior of entire arrays [10], [11]: a full array characterization is mandatory to evaluate the cell-to-cell variability and to extract statistical parameters fully representing the memory array.

In this work the reliability and the cell-to-cell variability during 500k endurance cycles have been evaluated by extracting a set of characteristic parameters from measurements performed on 1kbits arrays. After a preliminary optimization of the writing parameters on fresh devices, the effectiveness of the selected parameters has been verified during cycling by evaluating their impact on cell-to-cell variability and on the reliability lowering due to the cell breakdown.

II. MEMORY ARCHITECTURE AND EXPERIMENTAL SETUP

The 1kbits memory device integrated into a CMOS process is made of a 32x32 array. The cell and the test array architecture are depicted in Fig. 1, where:

- MTJ is the Magnetic Tunnel Junction device, composed of two ferromagnetic layers separated by an insulating layer;
- SP_1 , SP_2 and SP_3 are sense pads used during read. SP_1 is on the top of the MTJ, SP_2 is connected right below

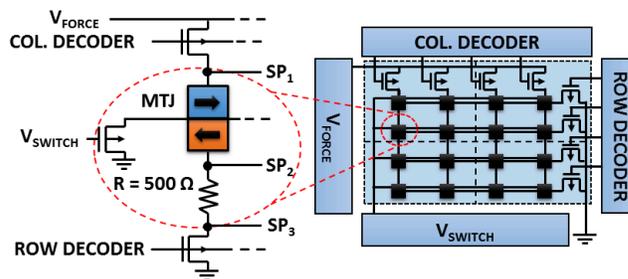


Fig. 1. Structure of a TAS-MRAM cell and its integration into the array tested in this work.

the MTJ and SP_3 is between a poly 500 Ω resistance and a select transistor.

In order to change the state of a memory cell, two different writing operations are available: Write '0' (W0) and Write '1' (W1). Both operations require two voltages: V_{FORCE} is required to locally heat the magnetic material, whereas V_{SWITCH} allows changing the magnetic field polarization after heating. All write operations have been performed with $T_{FORCE} = 500ns$, $T_{SWITCH} = 600ns$ and $T_{rise/fall} = 500ns$ for both voltages in order to avoid overshoot issues. All read operations have been performed with $V_{SWITCH} = 0V$, $V_{FORCE} = 0.3V$, $T_{FORCE} = 10\mu s$ and $T_{rise/fall} = 1\mu s$.

III. PARAMETER OPTIMIZATION IN FRESH DEVICES

To evaluate the impact of heating and switching voltages on write operations, a preliminary hysteresis analysis of both parameters has been performed on fresh devices. $|V_{SWITCH}|$ has been increased from 0.2V to 5V with $|\Delta V_{SWITCH}| = 0.2V$ and $V_{FORCE} = 1.4V$. The same procedure has been applied to evaluate V_{FORCE} hysteresis by increasing V_{FORCE} from 0.2V to 1.8V with $\Delta V_{FORCE} = 0.2V$ and $|V_{SWITCH}| = 5V$. A read operation has been performed after every step in both hysteresis analysis. Fig. 2 (a) shows the average resistances measured during switching voltage hysteresis and the switching parameters extracted for further analysis of W0 and W1 operations with $V_{FORCE} = 1.4V$:

- $\overline{R_{W0}}$ and $\overline{R_{W1}}$ are the average values of resistance R_{W0} and R_{W1} , respectively measured at $V_{SWITCH} = 5V$ and $V_{SWITCH} = -5V$.

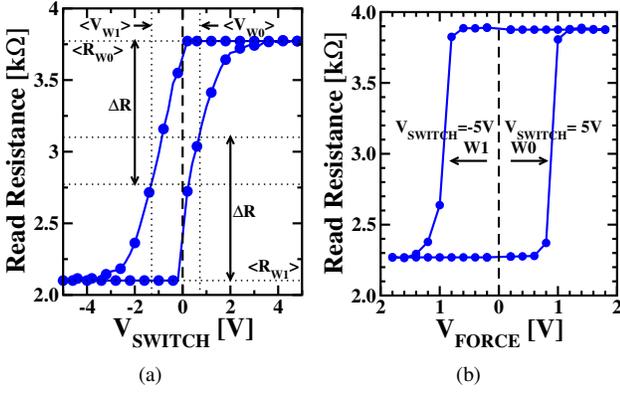


Fig. 2. Switching (a) and heating (b) voltage hysteresis measured on fresh devices.

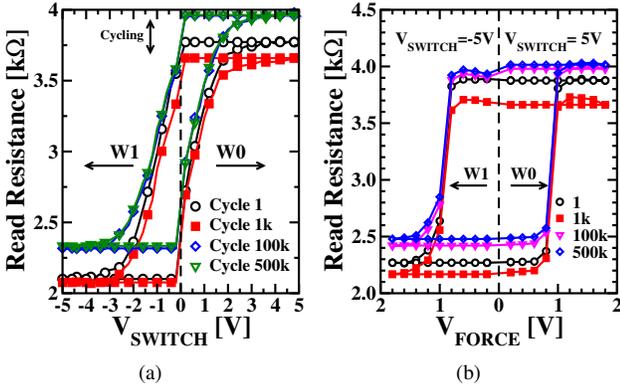


Fig. 3. V_{SWITCH} hysteresis measured during W0 and W1 operations at different cycles with $V_{FORCE} = 1.4V$ (a). V_{FORCE} hysteresis measured during W0 and W1 operations at different cycles with $|V_{SWITCH}| = 5V$ (b).

- $\overline{V_{W0}}$ and $\overline{V_{W1}}$ are the average switching voltages V_{W0} and V_{W1} , respectively, that allow obtaining a variation $\Delta R = 1k\Omega$ of the average measured resistance values.

Fig. 2 (b) shows the average resistances of the array cells measured during heating voltage hysteresis in W0 and W1 operations with $|V_{SWITCH}| = 5V$. It can be observed that $V_{FORCE} \geq 1V$ is required in order to successfully switch the magnetic field, whereas using $V_{FORCE} > 1.6V$ shows no advantages in terms of average resistance for both W0 and W1 operations. $V_{FORCE} = 1.4V$ and $|V_{SWITCH}| = 5V$ are shown to be the optimal write conditions, ensuring the highest resistance difference in W1 and W0 states.

IV. PARAMETER ANALYSIS UNDER CYCLING

To evaluate the cells performance and reliability during cycling and the effect of the cell degradation, 500k W0 and W1 operations have been performed with $V_{FORCE} = 1.4V$ and $|V_{SWITCH}| = 5V$.

Fig. 3 shows the switching voltage (a) and the heating voltage (b) hysteresis evolution during cycling: an equal R_{W0} and R_{W1} variation can be observed, thus keeping the resistance difference constant during cycling.

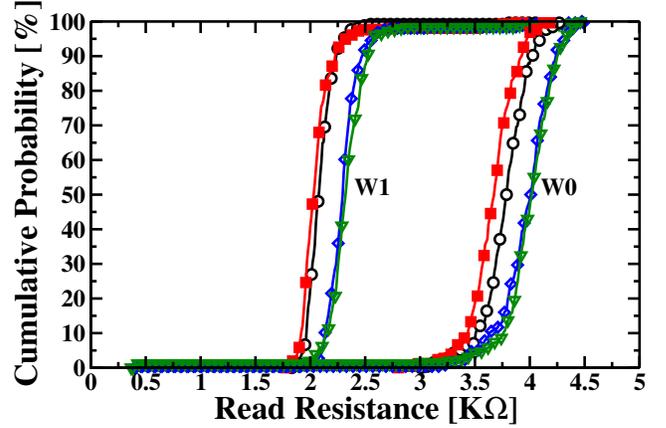


Fig. 4. R_{W0} and R_{W1} cumulative probability functions measured during 500k cycling with $V_{FORCE} = 1.4V$, $|V_{SWITCH}| = 5V$.

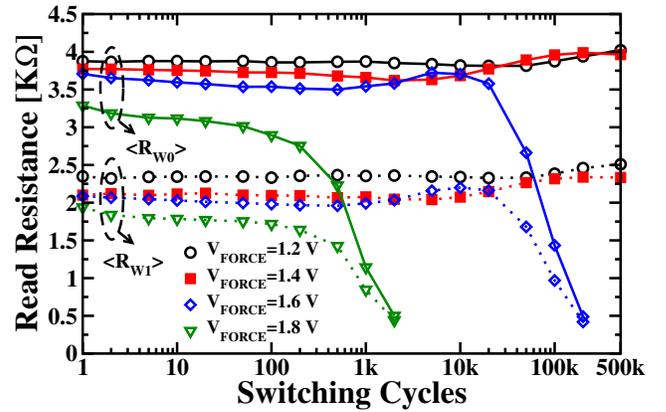


Fig. 5. $\overline{R_{W0}}$ (full lines) and $\overline{R_{W1}}$ (dotted lines) measured during 500k cycling with different V_{FORCE} conditions.

Fig. 4 shows the cumulative distributions of the read resistances measured after W0 and W1 operations at different cycles. Left tails on the distributions appear during cycles due to the cell degradation for a limited percentage of cells (below 3% after 500k cycles).

In order to evaluate the impact of V_{FORCE} during cycling, 500k cycles have been performed with different V_{FORCE} values and $|V_{SWITCH}| = 5V$, measuring R_{W0} and R_{W1} at different cycles. $\overline{R_{W0}}$ and $\overline{R_{W1}}$ measured during cycling are reported in Fig. 5, showing a sudden cell degradation after 100k cycles with $V_{FORCE} = 1.6V$ and after 1k cycles with $V_{FORCE} = 1.8V$, whereas the average resistances do not show any relevant change during the endurance tests with $V_{FORCE} = 1.2V$ and $1.4V$.

The dispersion coefficients (i.e. standard deviation over mean value) for R_{W1} and R_{W0} , evaluated during cycling with different V_{FORCE} conditions, are reported in Fig. 6: a rapid increase of their values can be observed before the breakdown with $V_{FORCE} = 1.6V$ and $V_{FORCE} = 1.8V$ at cycles 50k and 500, respectively. The use of $V_{FORCE} = 1.4V$ induces the lowest cell-to-cell variability of R_{W0} and R_{W1} during cycling.

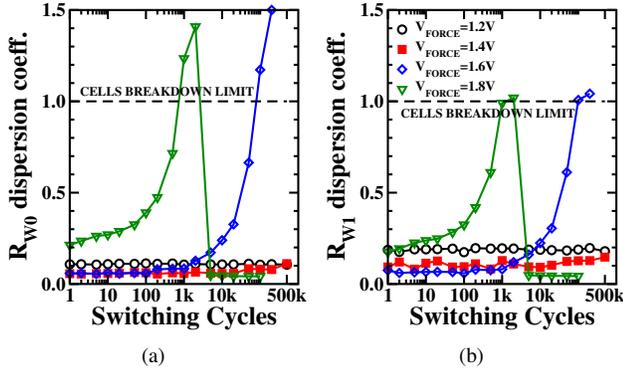


Fig. 6. R_{W0} (a) and R_{W1} (b) dispersion coefficients measured during 500k cycling with different V_{FORCE} conditions.

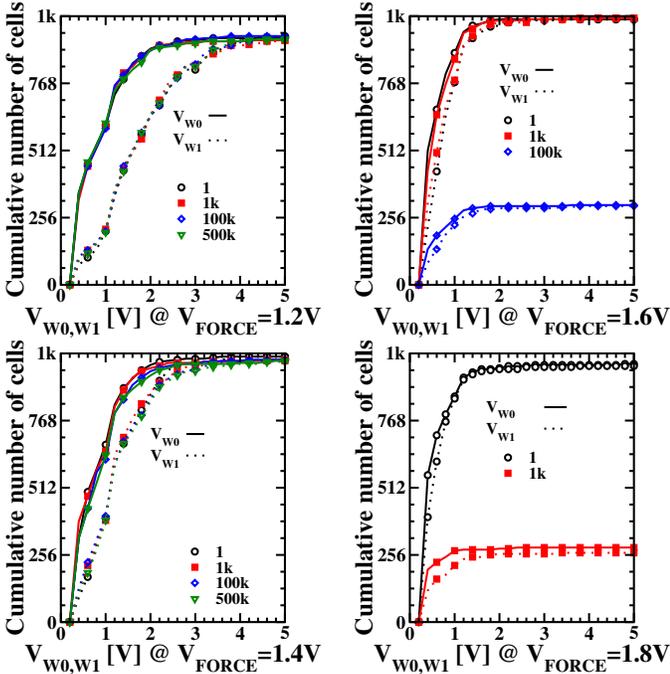


Fig. 7. Cumulative number of switching cells reaching the assumed variation $\Delta R = 1k\Omega$ with different V_{FORCE} during cycling.

The cumulative distributions of the V_{W0} and V_{W1} parameters measured during cycling with different V_{FORCE} conditions are reported in Fig. 7. The cumulative number of cells do not reach 1k because a limited number of cells do not reach, in switching, the assumed $\Delta R = 1k\Omega$. The minimum cell-to-cell variability during the endurance test is obtained by using $V_{FORCE} = 1.4V$. Moreover, $V_{FORCE} = 1.4V$ shows the highest cumulative number of switched cells: this means that a higher cells percentage reached the requested resistance variation $\Delta R = 1k\Omega$. According to the obtained results, the use of $V_{FORCE} = 1.4V$ has to be preferred since it guarantees the best reliability in cycling, denoted as the percentage of cells correctly switching. Using higher heating voltages results in a reduced yield (lower percentages of cells reaching the

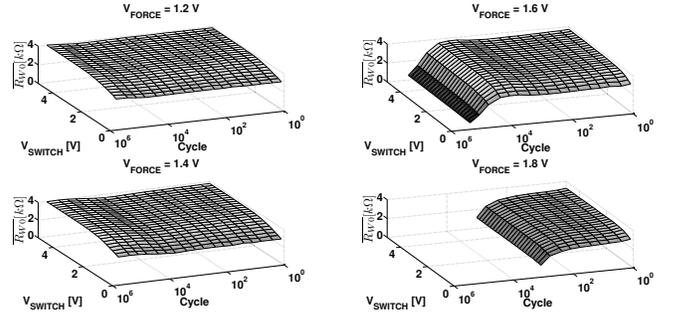


Fig. 8. 3D plot of $\overline{R_{W0}}$ as a function of V_{SWITCH} and cycle number for different V_{FORCE} conditions.

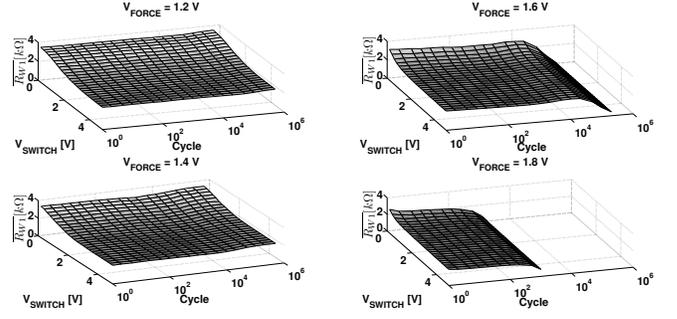


Fig. 9. 3D plot of $\overline{R_{W1}}$ as a function of V_{SWITCH} and cycle number for different V_{FORCE} conditions.

requested ΔR) and in a faster breakdown. According to the reported analysis, R_{W0} and R_{W1} are shown to depend on V_{FORCE} , V_{SWITCH} and cycling: the relationship between these parameters has been analyzed through 3D plots for different V_{FORCE} conditions for both W0 (Fig. 8) and W1 (Fig. 9). $\overline{R_{W0}}$ and $\overline{R_{W1}}$ depend on $|V_{SWITCH}|$ for any cycling and V_{FORCE} conditions: $|V_{SWITCH}| = 5V$ allows obtaining the highest $\overline{R_{W0}}$ values and lowest $\overline{R_{W1}}$ values. Using too high heating voltages (i.e. $V_{FORCE} \geq 1.6V$) results in a shorter lifetime, independently from V_{SWITCH} .

The most important parameter used to evaluate the switching capabilities on MRAM is the tunnel magnetoresistance (TMR) [12], calculated as:

$$TMR = \frac{R_{W0} - R_{W1}}{R_{W1}} \quad (1)$$

TMR cumulative distributions measured during endurance test at different cycles are reported in Fig. 10 for each V_{FORCE} condition. Since TMR depends on the difference between R_{W0} and R_{W1} and the resistance shift due to cell degradation is the same on both resistive states, no relevant variations can be observed on TMR until the cell breakdown is reached. $V_{FORCE} = 1.4$ allows obtaining the highest TMR in each cycling condition.

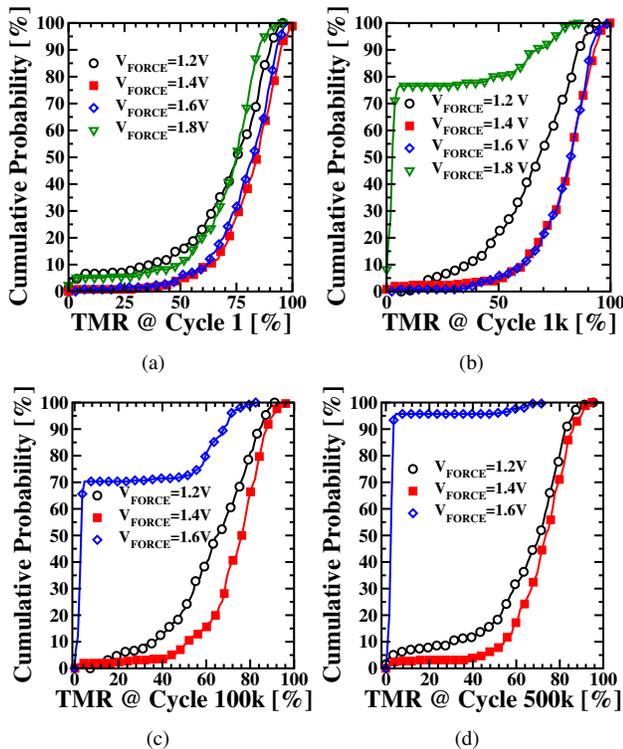


Fig. 10. TMR measured during cycling with different V_{FORCE} conditions at cycle 1 (a), 1k (b), 100k (c) and 500k (d).

V. CONCLUSIONS

The cell-to-cell variability and the switching reliability evolution during cycling have been evaluated on 1kbits TAS-MRAM. Both cell-to-cell variability and switching reliability depend on the chosen switching voltages. The relationship among characteristic switching parameters and operating conditions have been thoroughly investigated.

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REFERENCES

- [1] W. Gallagher, D. Abraham, S. Assefa, S. Brown, J. DeBrosse, M. Gaidis, E. Galligan, E. Gow, B. Hughes, J. Hummel, S. Kanakasabapathy, C. Kaiser, M. Lamorey, T. Maffit, K. Milkove, Y. Lu, J. Nowak, P. Rice, M. Samant, E. O'Sullivan, S. Parkin, R. Robertazzi, P. Trouilloud, D. Worledge, G. Wright, and S.-H. Yang, "Recent advances in MRAM technology," in *IEEE VLSI-TSA Int. Symp.*, April 2005, pp. 72–73.
- [2] S. Senni, L. Torres, G. Sassatelli, A. Bukto, and B. Mussard, "Power efficient thermally assisted switching magnetic memory based memory systems," in *Inter. Symp. on Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC)*, May 2014, pp. 1–6.
- [3] R. Sousa, I. Prejbeanu, D. Stanescu, B. Rodmacq, O. Redon, B. Dieny, J. Wang, and P. Freitas, "Tunneling hot spots and heating in magnetic tunnel junctions," *J. of App. Phys.*, vol. 95, pp. 6783–6785, 2004.
- [4] J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri-Sanial, J. Alvarez-Herault, and K. Mackay, "A complete resistive-open defect analysis for thermally assisted switching MRAMs," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 22, pp. 2326–2335, Nov 2014.
- [5] I. Prejbeanu, S. Bandiera, J. Alvarez-Hérault, R. Sousa, B. Dieny, and J. Nozières, "Thermally assisted MRAMs: ultimate scalability and logic functionalities," *Journal of Physics D: Applied Physics*, vol. 46, no. 7, p. 074002, 2013.
- [6] I. Prejbeanu, W. Kula, K. Ounadjela, R. Sousa, O. Redon, B. Dieny, and J.-P. Nozieres, "Thermally assisted switching in exchange-biased storage layer magnetic tunnel junctions," *IEEE Trans. on Magnetics*, vol. 40, pp. 2625–2627, 2004.
- [7] I. Prejbeanu, M. Kerekes, R. Sousa, H. Sibuet, O. Redon, B. Dieny, and J.-P. Nozieres, "Thermally assisted MRAM," *J. Phys.: Condens. Matter*, vol. 19, pp. 165 218–165 241, 2007.
- [8] S. Chaudhuri, W. Zhao, J.-O. Klein, C. Chappert, and P. Mazoyer, "Design of TAS-MRAM prototype for NV embedded memory applications," in *IEEE Int. Memory Workshop (IMW)*, May 2010, pp. 1–4.
- [9] R. Ferreira, S. Cardoso, and P. Freitas, "Dynamic thermo-magnetic writing in tunnel junction cells incorporating two GeSbTe thermal barriers," in *IEEE Int. Magnetics Conf.*, May 2006, pp. 394–394.
- [10] J. Azevedo, A. Virazel, A. Cheng, A. Bosio, L. Dilillo, P. Girard, A. Todri, and J. Alvarez-Herault, "Performance characterization of TAS-MRAM architectures in presence of capacitive defects," in *Int. Conf. on Advances in System Testing and Validation Lifecycle*, Oct 2013, pp. 39–44.
- [11] A. Grossi, C. Zambelli, P. Olivo, P. Pellati, M. Ramponi, J. Alvarez-Herault, and K. Mackay, "Automated characterization of TAS-MRAM test arrays," in *IEEE Int. Conference on Design Technology of Integrated Systems in Nanoscale Era (DTIS)*, April 2015, pp. 1–2.
- [12] S. Yuasa, A. Fukushima, K. Yakushiji, T. Nozaki, M. Konoto, H. Maehara, H. Kubota, T. Taniguchi, H. Arai, H. Imamura, K. Ando, Y. Shiota, F. Bonell, Y. Suzuki, N. Shimomura, E. Kitagawa, J. Ito, S. Fujita, K. Abe, K. Nomura, H. Noguchi, and H. Yoda, "Future prospects of MRAM technologies," in *IEEE Int. Electron Devices Meeting (IEDM)*, Dec 2013, pp. 3.1.1–3.1.4.