Analysis and Design Methodology of RF Energy Harvesting Rectifier Circuit for Ultra-Low Power Applications

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ABSTRACT This paper reviews and analyses the design of popular radio frequency energy harvesting systems and proposes a method to qualitatively and quantitatively analyze their circuit architectures using new square-wave approximation method. This approach helps in simplifying design analysis. Using this analysis, we can establish no load output voltage characteristics, upper limit on rectifier efficiency, and maximum power characteristics of a rectifier. This paper will help guide the design of RF energy harvesting rectifier circuits for radio frequency identification (RFIDs), the Internet of Things (IoTs), wearable, and implantable medical device applications. Different application scenarios are explained in the context of design challenges, and corresponding design considerations are discussed in order to evaluate their performance. The pros and cons of different rectifier topologies are also investigated. In addition to presenting the popular rectifier topologies, new measurement results of these energy harvester topologies, fabricated in 65nm, 130nm and 180nm CMOS technologies are also presented.

INDEX TERMS RF energy harvesting, RF rectifier, Internet-of-Things (IoT), implantable device, matching network, ultra-low-power.

I. INTRODUCTION

ENERGY harvesting from solar, thermal, vibration, and radio-frequency (RF) are increasingly being used to realize batteryless operation for Internet-of-Things (IoT) and biomedical applications [1]–[4]. Among these techniques, RF energy harvesting is particularly promising for biomedical devices where other sources are not readily available. RF energy harvesting is also employed for the RF identification (RFID) system, in IoT applications, among others. Several of these applications are utilizing widely used WiFi and Bluetooth low-energy (BLE) communication standards. These applications along with the wirelessly-powered neural implantable medical devices (*n*-IMD) for neural stimulation and recording are also benefiting from ultra-low power (ULP) circuits and systems design advancements [1].

For RF energy harvesting applications, integrated circuit (IC) design goals include developing high efficiency energy harvesting circuits across a wide input power range to maximize the output power. Often, we also need to maintain
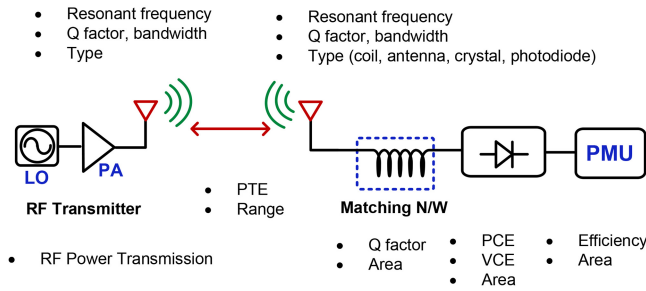
FIGURE 1. Block diagram of a typical radio frequency energy harvesting system. Design parameters that need to be optimized are shown for each stage.

FIGURE 2. Half-wave diode rectification circuits.

a minimum required input power level to maintain the normal functionality of the system. These circuits and system design approaches have provided new design methods as well as analysis for underlying circuits designs [5]–[7]. Most applications mentioned above utilize the characteristics of RF-to-DC rectifier but often also need to address concerns in their application space. Several applications, including n-IMD require higher level of on-chip integration to keep the device size small for lower cost, decreased invasiveness, and higher longevity [8]–[10]. As the size of the energy harvester along with the matching network decreases, the optimal powering frequency increases [11] which drives the operating frequency in the sub-GHz to tens of GHz range [8].

A typical RF energy harvesting system configuration is shown in Fig. 1. The antenna receives the RF signal and transmits it to the rectifier through a matching network. The rectifier converts the RF into a DC output. The main challenges of this procedure is to achieve a high power conversion efficiency (PCE) which is defined as the ratio of the delivered output power and the received input power. In most cases when the input RF signal amplitude is small, a low-loss rectifier is required in addition to a good matching network. Apart from PCE, the other important parameters such as sensitivity and output DC voltage can also be used to evaluate the system performance. The sensitivity means the minimum input power level that can achieve the desirable output voltage.

While several circuit architectures are generally well known [7], [12]–[15], the analysis of underlying circuits is quite involved. In [6], [16], [17], authors have performed analysis to obtain the model for output voltage and power of a rectifier. However due to complex equations and dependence of output on several design parameters, design optimization task is not simplified. In this paper, we propose a new square-wave approximation to achieve a simpler analysis. This helps us in obtaining design insights and upper limits on circuit performance which has not been reported previously. The main contributions of this paper are; (i) a new simplified method for analyzing RF rectifier topologies using the square-wave approximation, (ii) design optimization techniques based on the simplified analysis, and (iii) measurement results across three technologies to validate the analysis and optimization method.
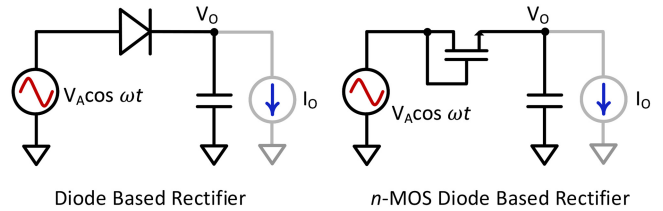
Using the proposed analysis, we can establish (i) independence of no-load output voltage of rectifiers on its threshold voltage, (ii) upper limit on its efficiency, and (iii) its output power characteristics. We draw these conclusions using square-wave approximation which cannot be easily drawn from analysis carried out in prior works. Further, we present a comparative study of designs across technologies through chip measurement results which will also provide useful perspective for designers. The paper is organized as following. Our analysis is presented in Section II. Section III presents other topology of energy harvesters. Section IV discusses how different applications utilize the physical mechanism of the energy harvester to serve their purposes and other design considerations, e.g., matching network design and the EMI effect. The discussion in the paper will be substantiated by several measurement results in Section V, including chip measurement results where new unpublished measurement data and circuit designs are also be included.

II. BASIC RECTIFIER ARCHITECTURE

RF energy harvesting circuits are built from multiple stages of a rectifier circuit. A typical half-wave rectifier is composed of a diode and a capacitor as shown in Fig. 2. In IC design, the rectifier stage is typically implemented using transistors as a diode as shown in Fig. 2. The input power received in RF energy harvesting applications is often low [18] due to FCC regulations on output power from a transmitter and associated path loss. Transistors operated as a diode in RF energy harvester circuits therefore operate more often in the sub-threshold or near-threshold regions. The usual RF input power is lower than −10dBm, even in cases where transmitter is very close to the receiver [5], [13], [19]. For this analysis, we will primarily focus on sub-threshold and near-threshold operation of the transistor.

A. HALF-WAVE RECTIFIER DESIGN

The half-wave rectifier stage as shown in Fig. 2 will provide an output voltage V_O and an output current I_O. For a fixed output load, V_O will be close to a DC voltage with small ripple as rectifier capacitor is usually large. The drain current of a transistor operated in the sub-threshold region is given by

$$I_D = I_S e^{(V_{GS}-V_{TH})/\eta V_t}\left(1 - e^{-V_{DS}/V_t}\right) \qquad (1)$$

where I_S is the sub-threshold saturation current, η is the ideality factor, and V_t is the thermal voltage given by kT/q. For
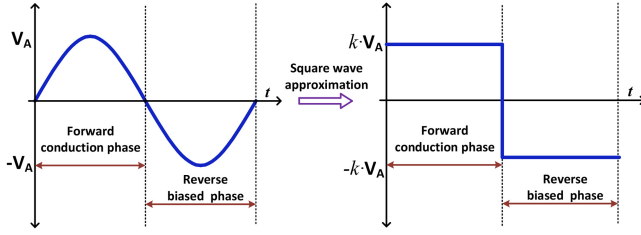
FIGURE 3. Square wave approximation for analysis.

TABLE 1. Notations used in the paper.

Variable Name	Physical Definition
V_t	Thermal voltage
V_{TH}	Threshold voltage
I_S	Sub-threshold saturation current
η	Ideality factor
k	Amplitude scaling factor
V_{ON}	No-load output voltage
T	Time Period of RF power

a diode in the RF energy harvester, its $V_{GS} = V_O - V_A cos\omega t$. The average current from the rectifier can be calculated by

$$I_O = \frac{1}{T} \cdot \int_0^T I_D \cdot dt \qquad (2)$$

However, this results in an involved output equation [20]. To further simplify the analysis, we approximate the sinusoidal input of an amplitude V_A with a square wave with an approximate amplitude of $k \cdot V_A$ as shown in Fig. 3. We assume that the scaling factor k for the square wave is such that both square wave and the sine wave input provides same output power. We will later show that this approximation is valid and provides a simplified solution for the output current, voltage, and power of the rectifier circuit. The resulting equation assuming a square wave input is given by

$$I_O \cong \frac{I_{ST}}{T} \cdot \int_0^{T/2} e^{(k \cdot V_A - V_O)/\eta V_t}\left(1 - e^{(-k \cdot V_A + V_O)/V_t}\right) \cdot dt$$
$$- \frac{I_{ST}}{T} \cdot \int_{T/2}^T e^{(0)/\eta V_t}\left(1 - e^{-(k \cdot V_A + V_O)/V_t}\right) \cdot dt \qquad (3)$$

where $I_{ST} = I_S \cdot e^{-V_{TH}/\eta V_t}$, and $V_{GS} = 0$ during the reversed bias phase. The equation resolves to

$$I_O = \frac{I_{ST}}{2}\left[e^{(k \cdot V_A - V_O)/\eta V_t}\left(1 - e^{(-k \cdot V_A + V_O)/V_t}\right) - 1\right] \qquad (4)$$

The expression of I_O is the general expression that can be further analyzed for two popular energy harvesting scenarios. In one scenario, we focus on the maximum efficiency of the energy harvesting system. In another scenario, no-load output voltage (V_{ON}) is of interest as it provides the maximum energy storage for the system through $E = C_{OUT}V_O^2/2$.

No-load Output Voltage: The no-load output voltage is given by eq. (4) when $I_O = 0$ and results into the following solution.

$$\left[e^{(k \cdot V_A - V_{ON})/\eta V_t}\left(1 - e^{(-k \cdot V_A + V_{ON})/V_t}\right) - 1\right] = 0 \qquad (5)$$

$$\left[\left(1 - e^{(-k \cdot V_A + V_{ON})/V_t}\right) - e^{(-k \cdot V_A + V_{ON})/\eta V_t}\right] = 0 \qquad (6)$$

Assuming that V_{ON} and $k \cdot V_A$ are close, we obtain,

$$\left[\left(1 - \left(1 - \frac{-k \cdot V_A + V_{ON}}{V_t}\right)\right) - \left(1 - \frac{-k \cdot V_A + V_{ON}}{\eta V_t}\right)\right] = 0$$

This results in the output expression for V_{ON} as

$$V_{ON} = k \cdot V_A - V_t\left[\frac{\eta}{1 + \eta}\right] \qquad (7)$$

Several conclusions can be drawn from eq. (7) that shed light on the rectifier design. First, it shows that the only process dependent parameter that affects V_{ON} is η indicating that transistor choice and size has a very low impact on the value of V_{ON} reached. Second, V_{ON} is a linear function of V_A which is anticipated because output should increase with input amplitude. Finally, it also shows V_{ON} to be complimentary to absolute temperature (CTAT) due to the $-V_t$ term. Another useful conclusion is that the rectifier will not produce meaningful output voltage for $V_A \lessapprox V_t$ as eq. (7) shows that V_{ON} will be negative in that case.

A key outcome of eq. (7) is independence of output voltage on V_{TH} which can be explained qualitatively as well. The average output current is zero in the no load condition which means that the sum of currents in the forward conduction path is equal to the leakage current in the reverse conduction path. In the reverse conduction path, $V_{GS} = 0$ and therefore the leakage is dependent on V_{TH}. In the forward conduction path, V_{GS} will only be slightly higher than 0 and forward current is also determined by V_{TH}. This means that a low V_{TH} transistor, which can supply high current in the forward path, will also have high leakage in the reverse path. Similarly a high V_{TH} transistor will have low conductance in the forward path but since its leakage is low as well, it will still reach higher voltage. Since currents in the forward and reverse phase depends on V_{TH} in the same way, therefore no load output shows no dependence on V_{TH} in the first order. The charging and discharging currents are influenced in the same way by V_{TH}.

To verify the results obtained from eq. (7), we performed the simulation of a single-stage rectifier across various conditions and with different transistor types. The output capacitors used in these simulations were very large based on energy harvesting applications. Simulations were carried out using foundry supplied process design kit (PDK) which uses comprehensive BSIM-4 model of transistors in 65nm CMOS technology. We performed the SPICE simulation of the circuit based on these models using Cadence Spectre SPICE simulation tool. Fig. 4a shows the simulation result of V_{ON} with varying V_A. We used an RF signal at $1.7GHz$ as V_A for this simulation. Two different transistors, NCH (V_{TH}=0.48V) and NCH$_{LVT}$ (V_{TH}=0.3V) in 65nm CMOS technology were used for these simulations. Despite a $180mV$ difference in their threshold voltage, both designs produce almost the same output voltage. A difference of $14mV$ when V_{ON} is $322mV$ is seen when V_A is 0.5V. We also note that the output remains
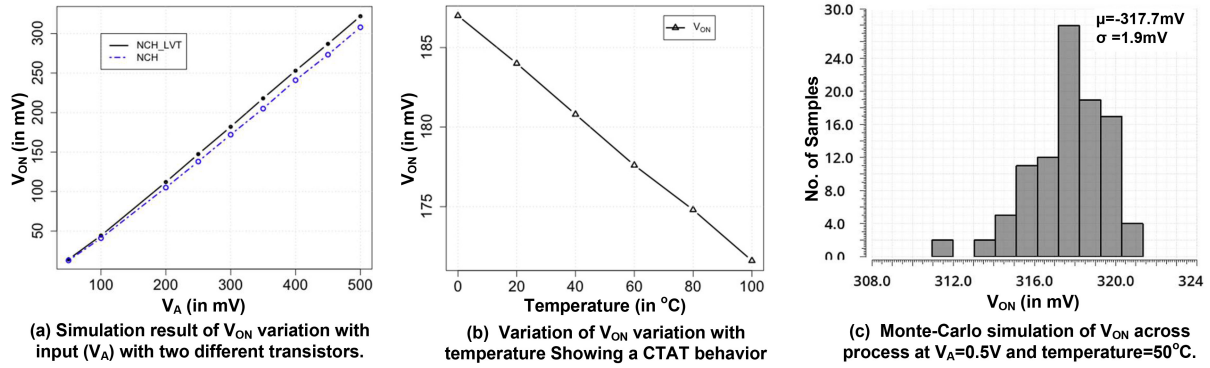
FIGURE 4. Simulation results of a half-wave rectifier stage output in no-load case.

linear with varying input power. This is an important outcome considering the square-wave approximation. We would see a non-linear V_{ON} behavior if k was not a constant and changing with input voltage. However, a linear V_{ON} confirms the trend predicted by eq. (7). The simulation result also indicate that the scaling factor k remains constant and our square wave assumption holds true across input power. This can be partly explained by the fact that the square wave contains higher order harmonics but due to low-pass nature of diode and capacitor, higher order harmonics do not contribute meaningfully to the output. Consequently, a sine wave and an equivalent square wave will show similar output voltages. Fig. 4b shows temperature variation of the single-stage rectifier output when V_A is $0.3V$ showing a CTAT behavior. Fig. 4c shows the simulation result of the variation of V_{ON} due to the statistical process variation. The Monte-Carlo simulation shows a 3σ process variation of 6% showing a low process variation while still operating in the sub-threshold region. Simulation results show that k has a value of 0.87.

Loaded Output Condition: In the loaded output condition, the average output current, I_O is approximately given by eq. (4). Also, as the output current will be much larger in the forward biased case than in the reverse biased case. The leakage current in the reverse biased case can be ignored. Also, $k \cdot V_A - V_O >> V_t$ in loaded condition for reasonable input voltages, the output current from eq. (4) can be approximated as,

$$I_O = \frac{I_{ST}}{2}\left[e^{(k \cdot V_A - V_O)/\eta V_t} - 1 \right] \quad (8)$$

The output power from the rectifier can be then written as

$$P_O = V_O \cdot I_O = V_O \cdot \frac{I_{ST}}{2}\left[e^{(k \cdot V_A - V_O)/\eta V_t} - 1 \right] \quad (9)$$

P_O comes out as a function of V_O and a quick inspection of eq. (9) shows that when V_O increases I_O decreases. It leads to a unique value of V_O at which P_O can be maximized when $dP_O/dV_O = 0$. For sub-threshold operation, the output power is maximized for a V_O value of $V_{O,max}$ is given by

the analytical equation,

$$V_{O,max} = \eta \cdot V_t\left[1 - e^{-(k \cdot V_A - V_{O,max})/\eta V_t} \right] \quad (10)$$

Although approximate, eq. (10) indicates that the maximum output power is realized when output voltage reaches a constant voltage of close to ηV_t. In reality, $V_{O,max}$ has a weak dependence on V_A in sub-threshold. It also shows that the transistor type has less impact on $V_{O,max}$ value in sub-threshold. It shows that as V_A increases, $V_{O,max}$ becomes constant. However, as V_A increases the transistor leaves sub-threshold and goes into saturation, $V_{O,max}$ is given by,

$$V_{O,max} = \frac{k \cdot V_A - V_{TH}}{3} \quad (11)$$

which shows dependence on both V_A and V_{TH}.

Rectifier Efficiency: Using the square wave approximation and $V_{O,max}$ values obtained from the previous analysis, we can obtain the peak efficiency expression for the rectifier. For the half wave design, the rectifier conducts only in the positive cycle while there is small leakage in the negative. Since the leakage power will be significantly smaller than the power transferred in the positive cycle, the input power can be given as,

$$P_{IN} = k \cdot V_A \cdot I_{IN} \quad (12)$$

Since rectifier conducts in only half cycle, average transferred power from the source is $k \cdot V_A \cdot I_{IN}/2$. Further, applying ideal impedance matching for the rectifier in the conduction cycle, maximum available power for the rectifier is $1/2 \cdot k \cdot V_A \cdot I_{IN}/2$. Total charge transfer in one cycle using square wave approximation can be given as $I_{IN} \cdot T/2$ which should be equal to the total output charge of $I_O T$ which sets $I_{IN} = 2I_O$. The corresponding power conversion efficiency (PCE) is given by

$$PCE = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{0.5 k V_A I_{IN}/2} = \frac{V_O I_O}{k V_A I_O/2} = \frac{2V_O}{k V_A} \quad (13)$$

Using this, we obtain the expression for maximum efficiency in sub-threshold for higher values of V_A can be approximately given as,

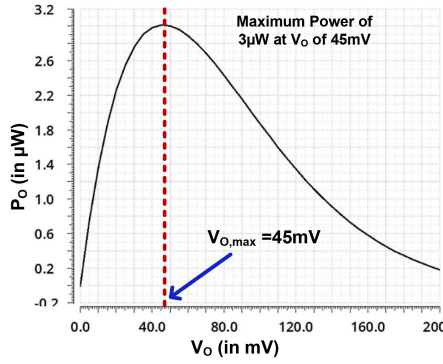$$PCE_{Sub} = \frac{2\eta V_t}{k V_A} \quad (14)$$

FIGURE 5. Simulation of a output power of a half-wave rectifier stage as function of output voltage with $V_A = 0.4V$ and temperature = 27°C.

FIGURE 6. Simulation of $V_{O,max}$ as a function of V_A and temperature.

Eq. (14) shows that the maximum efficiency can be reached when $kV_A = 2\eta V_t$. Since $V_{O,max}$ is close to ηV_t in sub-threshold, the above condition indicates impedance matching between input and output. Also, it shows that the efficiency will degrade for higher input power. This happens due to the increase in input power but output voltage remains ($\approx \eta V_t$) low for maximum efficiency. This means that we need to add more stages to increase the efficiency. This will increase the value $V_{O,max}$ to increase the output power.

The expression for efficiency in saturation region ($kV_A > V_{TH}$) using eq. (11) and (13) can be given as,

$$PCE_{Sat} = \frac{2}{3}\left(1 - \frac{V_{TH}}{kV_A}\right) \quad (15)$$

From this equation, we observe that rectifier efficiency can be increased by increasing the input power. We also observe that when the output power is maximum, the overall rectifier efficiency is always lower than 66.7%. This upper limit is based on approximation and slightly higher efficiencies can be realized. However, this observation is generally in line with the reported efficiencies in the literature where peak efficiency of CMOS rectifiers has remained below 70%.

We simulated the half-wave rectifier circuit in SPICE using foundry supplied PDK model to verify our analysis. Fig. 5 shows the output power as a function of output voltage. A maximum power of $3\mu W$ is realized at $V_{O,max} = 45mV$ for an input voltage of $400mV$ at $27°C$. The output power will increase linearly for lower values of V_O owing to the small contribution $e^{-V_O/\eta V_t}$ function but will decrease exponentially at higher values V_O owing to exponential decay function due to $e^{-V_O/\eta V_t}$. In between it will have a peak. The simulation result in Fig. 5 matches closely with the trend predicted by eq. (9) verifying our underlying analysis. We further swept the V_A to obtain the corresponding $V_{O,max}$ value. Fig. 6 shows the variation of $V_{O,max}$ with V_A for NCH and NCH$_{LVT}$ designs. In the sub-threshold region, the slope of the curve is small. Also, difference of $V_{O,max}$ of NCH and NCH$_{LVT}$ is small. In the saturation region, the slope of the curve is large. Note that the output power does depend on the transistor type. For maximum output power, the transistor that provides the highest current should be
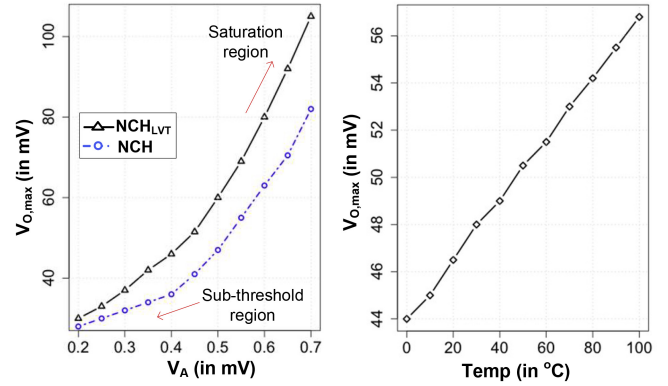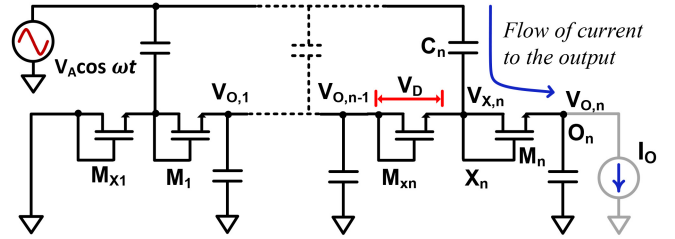

FIGURE 7. A multi-stage rectifier topology.

used. It indicates an advantage for bigger and lower V_{TH} designs. For maximum voltage designs, as discussed earlier, transistor size or types have less impact.

B. MULTISTAGE RECTIFIER DESIGN
The half-wave rectifier analysis carried out in the previous section lays the foundation for analyzing multi-stage (n-stage) designs. Fig. 7 shows the circuit architecture of a multi-stage rectifier we analyze in the following section.

Operating Principle: The multi-stage rectifier operates in the following manner. When the RF input is negative, M_{X1} is forward-biased and M_1 is reverse biased. The DC node 1 voltage (V_1) is slowly charged up whenever M_1 is conducting through the forward bias. During the positive cycle, M_1 is conducting when the voltage difference between V_1 and $V_{O,1}$ is positive or higher than the threshold voltage and the charge accumulated during the previous cycle on C_1 is dumped to C_2 until there is no voltage difference. By stacking multiple number of stages (n), the output voltage can be built up to the desirable level according to the application requirements.

No-load Output Voltage: The no-load output voltage of a half-wave rectifier can be directly applied in a multi-stage rectifier. The no-load output voltage of the first half-wave stage, in a multi-stage rectifier, will be the same as the output of a stand-alone half-wave rectifier. For the next stage, its input voltage swings on top of the DC level of the first stage, which will result in an output voltage $2\times$ of the half-wave rectifier and so on. Note that the body biasing of the transistor will result in an elevated threshold voltage of the higher stage transistors. However, our analysis for the single
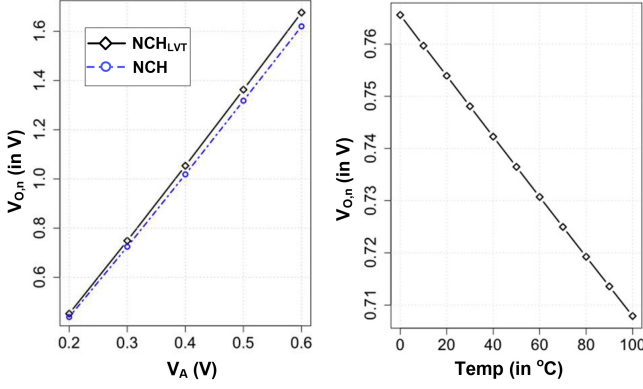
FIGURE 8. No-load output voltage of a multi-stage rectifier with input voltage and temperature variation.

FIGURE 9. Simulation result showing variation of maximum power point in a 2-stage rectifier. a) Variation of maximum power point with V_A, b) simulation showing output power as a function of output voltage $V_{O,n}$.

stage design reveals that no-load output voltage does not depend on the threshold voltage which will also apply here. Finally, the no-load output voltage for an n-stage rectifier, $V_{O,n}$ is given by

$$V_{O,n} = 2n \cdot V_{ON} \cong 2n \left\{ k \cdot V_A - V_t \left[\frac{\eta}{1 + \eta} \right] \right\} \quad (16)$$

Fig. 8a shows the simulation result of a 2-stage rectifier providing no-load output voltage for NCH and NCH$_{LVT}$ transistor type. It shows the expected linear behavior with V_A with only 3% difference in output voltage. Note that the body effect of transistors in a multi-stage design also does not directly affect the open circuit voltage. Fig. 8b shows the temperature variation of $V_{O,n}$ which shows the anticipated CTAT behavior similar to a single stage design.

Loaded Output Condition: To analyze the loaded output condition in a multi-stage rectifier, we rely on our half-wave rectifier analysis. Fig. 7 shows this circuit where the internal nodes are named to help understand the analysis. The nodes whose output is connected using a capacitor to an RF source are called X_i and the output node whose capacitors are connected to ground are called O_i. The average voltage of each internal node are designated as $V_{X,i}$ and $V_{O,i}$ which are constituted out of half-wave stages. Node X_n connects the final half-wave stage to the output whose average voltage is given by $V_{X,n}$. The output voltage is given by $V_{O,n}$ and it sees the output load current I_O. When a positive voltage is applied at X_n, it will see $k \cdot V_A + V_{X,n}$ which will be greater than $V_{O,n}$ and supplies current to the output. When the negative voltage is applied at X_n, it will see $V_{X,n} - k \cdot V_A$ and the transistor M_n gets reversed biased supplying very small leakage current to the output in this stage. However, M_{Xn} gets forward biased in this phase, which supplies the charge in the negative phase to maintain the average voltage $V_{X,n}$. Owing to this scenario, average voltage across each half-wave stage, V_D would be approximately be equal. In reality, there will be some difference between the voltages each half-wave stage but it is ignored for this analysis. For an n-stage rectifier, there are $2n$ half-wave stages, therefore, $V_{O,n} = 2n \cdot V_D$. This sets the value of $V_{X,n} = V_{O,n} - V_{O,n}/2n$.
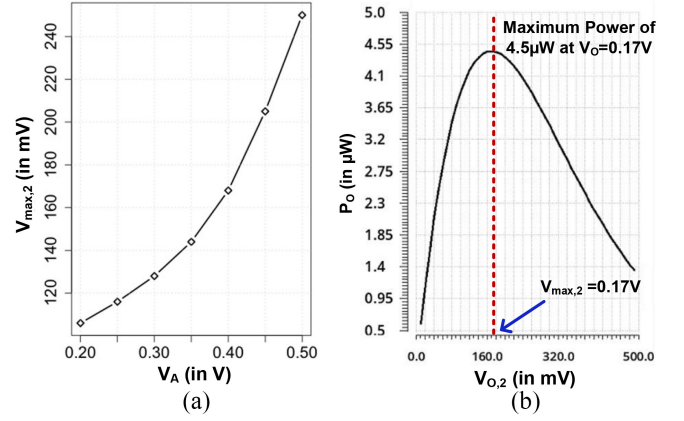
Therefore, when M_n is forward biased, it sees gate-source voltage of $V_{X,n} + k \cdot V_A - V_{O,n} = k \cdot V_A - V_{O,n}/2n$. The average current coming out of M_n is the output load given by

$$I_O = \frac{I_{ST}}{2} \left[e^{(k \cdot V_A - V_{O,n}/2n)/\eta V_t} - 1 \right] \quad (17)$$

The output power in this case is given by

$$P_O = V_{O,n} \cdot \frac{I_{ST}}{2} \left[e^{(k \cdot V_A - V_{O,n}/2n)/\eta V_t} - 1 \right] \quad (18)$$

Maximizing this expression with respect to $V_{O,n}$ gives the expression for voltage corresponding to maximum power,

$$V_{max,n} = 2n \cdot \eta \cdot V_t \left[1 - e^{-(k \cdot V_A - V_{max,n}/2n)/\eta V_t} \right] \quad (19)$$

Eq. (19) is similar to eq. (10) and similar to half-wave rectifier, multi-stage rectifiers will also have linear increase with V_A in the saturation region, while eq. (19) relates the behavior in the sub-threshold region. Fig. 9a shows the variation $V_{max,n}$ with V_A in a 2-stage rectifier showing a similar trend. Fig. 9b shows the variation of output power as a function of output voltage clearly showing a peak response. We also note that the output power increases as with transistor's drive strength. Since the output power directly depends on transistor's drive strength, body-effect in a multi-stage design will adversely affect rectifier's efficiency. Also deep n-Well transistors are commonly used to alleviate the body effect.

C. STAGE-SELECTION IN MULTI-STAGE RECTIFIER
Stage-selection requirement for the no-load condition would require a design that can realize the maximum output voltage but the strategy diverges for the loaded condition. For a given transistor type, increasing the drive current increases maximum output power in half-wave and multi-stage rectifier. In this section we analyze, how the maximum power varies, both with transistor size and number of stages. In our previous analysis, the input resistance of the source is not included as the analysis directly focused at the input voltage level V_A. However, as we move our analysis towards maximum obtainable power, source resistance
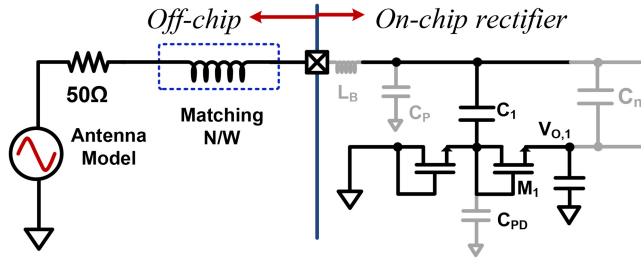
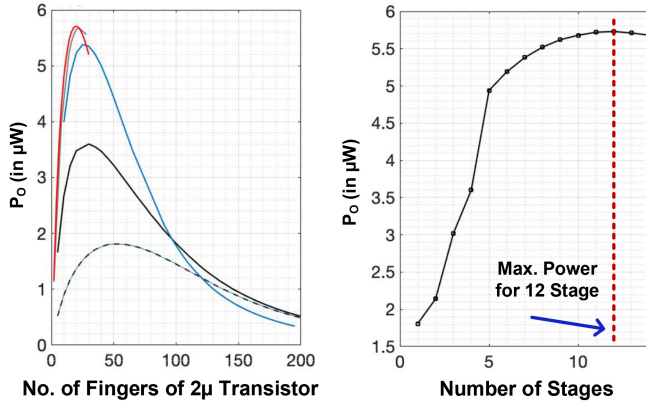**FIGURE 10.** Block diagram of the multi-stage rectifier with matching network and interconnect parasitics.

FIGURE 11. Simulation result to obtain maximum power by sweeping device size and number of stage for a multi-stage rectifier design for a $400mV$ input voltage.

has to be factored. In this case, 50Ω series resistance is used to model an antenna. Further, we have assumed that an input voltage 400mV with a source resistance of 50Ω drives the rectifier. The bondwire, pad, and ESD parasitic were included into a 2nH inductance and 200fF capacitance at the input.

We earlier showed that a fixed output voltage, $V_{max,n}$ is obtained for the maximum power. Consequently, transistor size can be increased to obtain more power by increasing the current. However, this will reduce the level of V_A seen at the input. For an n-stage rectifier, an optimal device size exists for maximum output power. However, as we change the number of stages, the output power and device size will also change. This requires a nested sweeping of transistor size and number of stages to obtain the maximum power for a given input power. Fig. 11a shows maximum output power variation with device size. We swept the device width from $2 - 400\mu m$ for different n-stage rectifier. As the number of stages change, the maximum output power changes and a peak power is realized for different device size inline with eq. (19). We simulated the design for a $400mV$ input voltage. A 12-stage rectifier with a width of $40\mu m$ yielded the maximum power. As the number of stages increased, maximum power increased up to 12-stages after which it started decreasing (Fig. 11b). The maximum achievable efficiency for this circuit is 11.56%.

Role of Matching Network: Eq. (19) clearly indicates that the maximum power increases with an increase in the input voltage swing. The circuit configuration with antenna and rectifier will keep the voltage swing below the received voltage swing due to the resistive drop. However, we can bring a reactive component to the mostly capacitive rectifier by introducing the matching network. Assuming that each rectifier diode stage presents a parasitic capacitor C_{PD}, the input of the rectifier presents a total capacitance of $n \cdot C_{PD}||C_n$. As the capacitor $C_n >> C_{PD}$, the total capacitance presented by the rectifier is approximately equal to $n \cdot C_{PD}$. This will get added to the parasitic capacitor of bond-pads, ESD circuits, and board parastics to yield an equivalent capacitance of C_{EQ}. A single inductor matching will yield the input voltage $V_I/R \cdot 1/j\omega C_{EQ}$. It clearly shows that reducing the C_{EQ}, gives higher voltage at the input of the rectifier. A smaller transistor, a fewer number of stages, and lower parastics will give higher voltage and hence higher efficiency for the design. However, the high quality factor inductor would reduce the total bandwidth of the matching network. In later sections, we will outline the design principles for matching network, role of parasitics, and the optimal device size.

The issue comes up when most energy harvesters adopt n-MOS transistors rather than p-MOS due to its better current driving ability with the same size ratio, but the body of NMOS have to be tied to ground hence V_{SB} increases as source increasing the body effect.

III. COMMON RECTIFIER TOPOLOGIES
Apart from the conventional half-wave topologies discussed in the previous section, bridge-type full-wave rectifiers are also commonly used for energy harvesting applications.

A. BRIDGE-TYPE FULL WAVE RECTIFIER
Full-wave bridge rectifier which is comprised of four diodes and one capacitor is a popular topology. A MOS rectifier structure can thus be formed using only n-MOS and/or p-MOS devices. V_{TH} of MOS transistors will reduce the efficiency of the rectifier. Fig. 12a shows the circuit design of a single stage bridge type rectifier. It conducts current in both phases. The analysis presented in Section II applies for this circuit as well while taking into account conduction in both phases. Note that the no-load output voltage for this circuit will have similar behavior as the half-wave rectifier (eq. (7)). This is because when one set of diodes conduct in the positive phase, the other set will have leakage and a similar operating condition is realized. In case of loaded output condition, the primary design goal is to maximize efficiency. Note that in a full-wave rectifier, the output current increases but so does the associated switching and conduction losses. The efficiency optimization therefore requires proper device sizing for a given operating condition. Apart from device sizing, another general idea to improve efficiency includes improving diode characteristics through circuit design techniques.
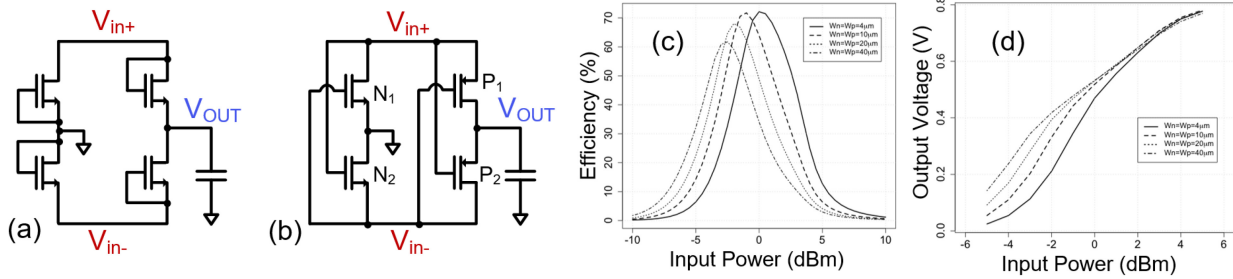
FIGURE 12. Schematic of a (a) bridge-type full wave rectifier, a (b) cross connected bridge rectifier, (c) variation of efficiency with received input power and transistor size for a single stage cross-connected bridge type rectifier ($L_n = L_p = 60nm$, $R_L = 25k\Omega$), and (d)variation of output voltage V_{OUT} with received input power and transistor size for a single stage cross-connected bridge type rectifier ($L_n = L_p = 60nm$, $R_L = 25k\Omega$).

B. CROSS-CONNECTED BRIDGE RECTIFIER

A popular method for improving the performance of a bridge-type rectifier is to reduce its forward voltage drop by using a cross-connected bridge rectifier as shown in Fig. 12b. This type of rectifier uses internal nodes within the rectifier to bias the transistor gates. During positive half-cycles of the input voltage, current flows through P_1 and N_2, while transistors N_1 and P_2 are in the cutoff region. The situation is reversed for negative half-cycles of the input voltage. In each case, the cross-coupled PMOS transistors (i.e., P_1 or P_2) have higher V_{GS} (compared to a diode-based rectifier), therefore lower on-resistance. Due to this self-driven scheme, the cross-connected can operate at lower RF input power levels. To maximize efficiency, the body terminals of the p-MOS and n-MOS transistors should be connected to V_{OUT} and ground, respectively. One major drawback of this design is that for input voltages larger than V_{TH}, the transistors do not turn off immediately after V_{in+} drops below V_{OUT}. Yet, it is one of the commonly used types of topology. The capacitors need to be large enough such that their impedance is small compared to the on-resistance of the MOS transistors. Therefore large transistors lead to large coupling capacitors, which can result in higher area overhead.

Additional design consideration comes from the parasitic device capacitance between input and output. It provides an AC bypass of the input power to the output. In other words, it divides part of the input power and send it directly to the output without rectifying. That results in a reactive power component at the output which will reduce the efficiency of the rectifier. Essentially AC bypass of input through the parasitic series capacitor and rectification by the diode depends on the size and I-drive of the rectifier. If we keep the size of the transistor small, AC bypass will be small, however the rectification will also be small. Therefore, transistor size should increase to increase the rectification of input power. However, after a point increasing the size only increases the output power incrementally but it increases the bypass AC component linearly. Therefore, the AC-bypass due to parasitic capacitor also requires optimal device sizing. It will also impact the matching network design for the rectifier as it creates an output power component which is reactive.

Due to these factors, devices with higher drive current with low capacitance are preferred.

Fig. 12c shows efficiency variation with the transistor size and input power. It achieves peak efficiency at a given input power level for a given transistor size. By increasing the device size, peak efficiency can be realized at lower power levels. However due to the increase of overhead associated with the switching loss, the value of the peak decreases. The output load R_L connected to V_{OUT} in this case was $25k\Omega$. This behavior is also verified by later silicon implementation in Section V. Fig. 12d shows the variation of output voltage, V_{OUT} with transistor sizing and input power at same output load. V_{OUT} value is higher as input power increases. However, it starts saturating at higher input power level due to conduction in the reverse-biased condition.

IV. OTHER DESIGN CONSIDERATIONS

Recent works focus on designing the efficient RF energy harvesting system under low input power conditions. The biggest challenge is to realize high PCE in small form-factor at low input power level. The practical trade-off often limits the improvements in all aspects. In this section, different design scenarios are discussed in order to fairly evaluate them. Fig. 1 shows a typical structure of a energy harvesting system. Designs in [21]–[23] also use a chain of rectifiers to start up the entire system from initial state and maximum-power-point tracking (MPPT) is implemented to extract the maximum power. Since DC-DC converter can achieve $80 - 90\%$ efficiency to step up/down voltage, the rectifier does not need extra stages at the cost of decreasing PCE. In the IMD application, the major design difference from above is to realize high integration with small form-factor. The challenge is to design an energy harvester which could provide high current injection, high PCE with limited silicon area.

A. GENERAL EFFICIENCY OPTIMIZATION DESIGN FLOW

Important goals when designing an energy harvesting circuit is to realize high PCE or voltage conversation ratio (VCR). The VCR is defined as the ratio of the rectified output DC voltage (of the last stage) to the peak amplitude of the input AC voltage of the rectifier (of the first stage). Unfortunately,

techniques used to increase PCE often decrease the VCR. We can prioritize only one for a particular application. We detail an iterative design optimization flow for a rectifier design.

1) The first step is to assign or estimate the design constraints such as the resonant frequency, the output load (an RC model can be used to represent it), and the input voltage swing. The needed output capacitance should also be known early-on during the design optimization limited IC area for an implant.

2) The suitable rectifier topology should be chosen based on application needs, as the rectifier type that displays the highest PCE depends on various parameters such as frequency, input power, transistor size, and desired VCR. Here our analysis serves as the basis for choosing initial device size, type, and number of stages.

3) The third step involves maximizing the PCE. In most rectifiers, this is achieved by finding the optimal transistor width. After the first cut size is provided by our analysis, it is important to simulate the design with the target load for final optimization. As our analysis shows that there is a load value that gives a peak efficiency for a given size (Fig. 9), conversely a device size exists that gives peak efficiency for a given load.

4) Step 3 is repeated in order to find the optimal capacitance and rectifier width simultaneously. Afterwards, the layout is drawn to extract the parasitics which are needed to obtain a more accurate design.

5) Finally, the input impedance of the rectifier is simulated to design the matching network. Note that the matching network has to be tuned such that V_{RF} is achieved. This often means that maximum efficiency is obtained by finding the sweet spot between impedance matching and desired voltage swing.

B. PERFORMANCE COMPARISON

To demonstrate how changing the target rectified voltage (and thus power delivered to the rectifier) changes the optimal topology, we compare L_{VT} cross-connected topology with a Z_{VT} diode-connected topology. For each topology, the transistors were sized for maximum PCE. Fig. 13 shows that for a rectified voltage of 1V, the cross-connected bridge rectifier with L_{VT} transistors shows a higher PCE compared to the diode connected topology Z_{VT} transistors. The opposite is true for a regulated voltage of 3 V. It can be concluded that cross-connected topology is more efficient while producing low output voltage.

C. MATCHING NETWORKS
1) SIGNIFICANCE

The matching network is used for directing maximum AC power towards the rectifier at one or more RF frequencies. In addition, they can also boost the voltage through a passive gain and can act as a low pass filter to reject higher
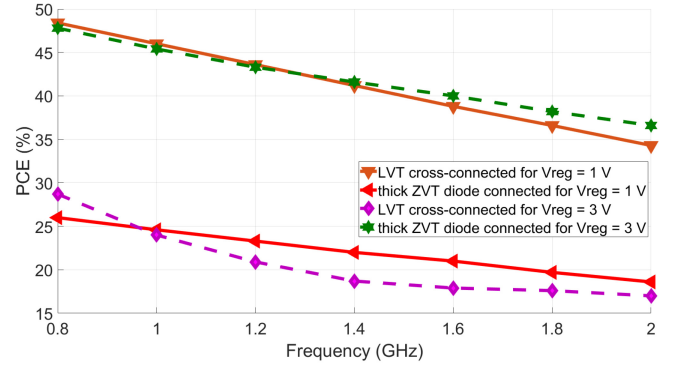

FIGURE 13. Post-simulated PCE over frequency of the 2 rectifier topologies with a load of 30kΩ and a rectified voltage of 1 V and 3 V.
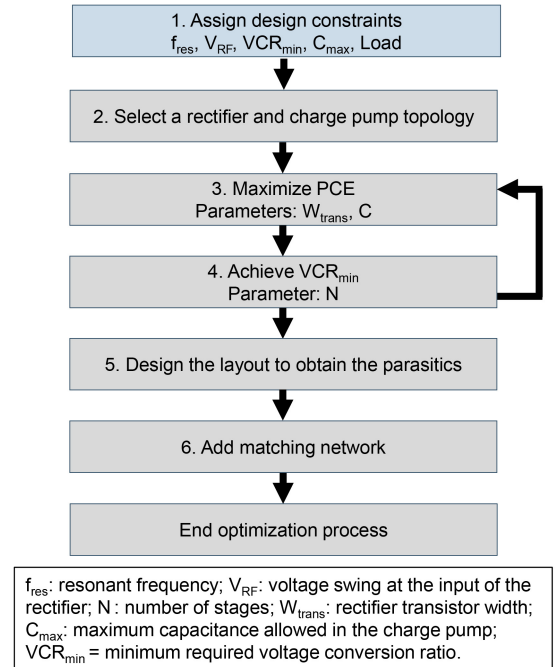

FIGURE 14. Charge pump rectifier iterative design optimization flowchart.

order harmonics generated by the rectifier which can get re-radiated. Often, published results on rectifier efficiency are calculated mathematically from the measured S-parameters in a way that does not include input mismatch power losses. Although PCE is important to consider, it does not give a good idea of how the rectifier performs in a practical circuit. Co-designing the matching network and the PCE of the rectifier is crucial for maximizing the power harvesting efficiency of the system. Some rectifier architectures provide a very large PCE at the expense of a very large input impedance which makes it difficult to design a small area matching network.

2) FIXED MATCHING SYSTEM

The matching network is one of the last blocks to design in the energy harvesting systems because it depends on the input resistance of the rectifier (R_{IN}) which is linked to the

power as,

$$R_{IN} = V_A^2/(2P_{IN}) \qquad (20)$$

where V_A is the input amplitude and P_{IN} is the input power.

To maintain a low loss for matching, reactive matching networks are used. Common matching networks are typically composed *LC*-networks such as π and T networks. High quality factor (Q) matching networks provide a passive voltage gain to increase the voltage swing at the input are desirable to minimize loss, however, they suffer from narrow bandwidth making it sensitive to frequency variations. This is important when using on-chip passive elements whose values can change due to process.

An off-chip matching network provides additional design flexibility while supporting higher Q and larger component values. Unfortunately, off-chip components prevent the miniaturization of the implant and therefore are not always feasible. On the other hand, it is important to note that IMDs limited to *mm*-dimensions will not always have the space to include on-chip matching networks as large inductors are needed.

3) ADAPTIVE MATCHING SYSTEM

The rectifier operates in different regions since the input sees a large AC signal without any DC bias. This results in an impedance variation making it difficult to match at all times. Impedance variations also happens due to changes in received power and output load. Often matching for worst-case scenarios, i.e., when V_A is lowest. If variations are large, then a wideband impedance matching network is used at the expense of a low Q-factor.

An alternative method is to include an auto-tuning impedance matching network that maintains a constant efficiency even when the received RF power or the load changes [24]–[26]. In [27], authors presented an adaptive antenna-impedance tuning unit for ULP IMDs operating at 2.4GHz. The design requires a power amplifier, a tunable matching network, a capacitive attenuator, a mixer, and a g_m-C filter. In [24], authors developed a fully integrated wireless power transfer receiver with a synchronous adaptive matching network that guarantees the maximum achievable efficiency for a given load. A switched capacitor array was controlled according to a sign-based gradient descent algorithm to maximize the power delivered to the rectifier load at the receiver. These techniques address the challenge by adding a processing unit for dynamic calibration. However, the additional circuitry needed to measure the impedance of the rectifier or that of the network increases the power consumption and area and can be used only if a significant efficiency increase can be realized.

D. MEASUREMENT TEST-BENCH SETUPS
1) IMPACT OF BONDPADS ON THE PCE

A bondpad is equivalent to a shunt capacitor which becomes a low-impedance path at high frequency. Table 2 presented
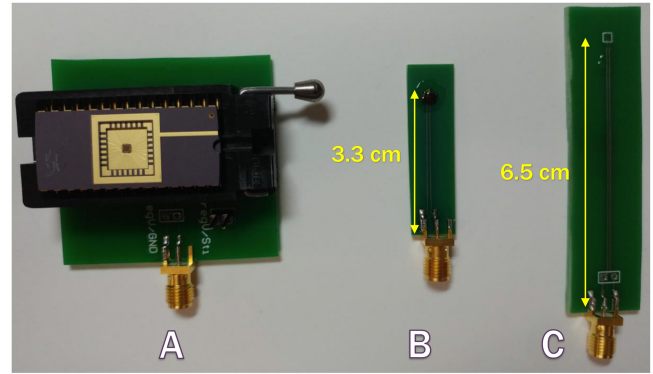

FIGURE 15. Picture of different PCB setups used to measure the regulated voltage generated by the Rx device [28].

TABLE 2. IO pads parasitics @ 915MHz from post-layout simulation.

Size (μm^2)	Resistance (Ω)	Capacitance (fF)
50 x 50	0.91	117.5
80 x 80	0.90	278.5
100 x 100	0.51	415.6
120 x 120	0.58	580.0

the parasitics of different sizes of IO pads. The conventional size bond pads connected to the input of a rectifier could severely reduce PCE. This effect may be minimized by decreasing the size of the bond pads and by using octagonal shapes. Furthermore, relying on precision RF probes instead of wirebonding allows further reduction of the input bondpad area.

Bondpads typically include diodes in order to shield against ESD damage. However, the diodes can leak a significant amount of RF current. Fortunately, due to the nature of rectifiers, the ESD structure can be smaller or not needed as in rectifiers the gate terminals are also connected to source/drain regions of other transistors providing a path for ESD charge.

2) IMPACT OF EMI ON THE MEASUREMENT SETUP

When transmitting large amounts of power at a short distance, the setup becomes affected by unwanted eddy currents in the PCB traces [29]. Eddy currents loss can be minimized in the silicon substrate by using a silicon-on-insulator (SOI) process [30], however, eddy currents in highly conductive PCB traces are difficult to minimize. A common solution to this problem is to cover the PCB with a high-permeability ferrite sheet which deflects the magnetic flux. Unfortunately, commercial ferrite shields are not effective at high frequencies in which μm-sized coils need to operate in order to resonate. One method is the careful design of the PCB layout. The design techniques that have been applied include: i) reducing the area of closed metal loops as much as possible, ii) keeping the number of traces on board to a minimum, iii) reducing the width of the metal traces to a minimum, iv) using coaxial cables to interface with the PCB, v) prioritizing SMA connectors over headers or large BNC connectors and placing them far from the transmitter coil, and vi) prioritizing wire-bonded dies. Fig. 15 shows the our
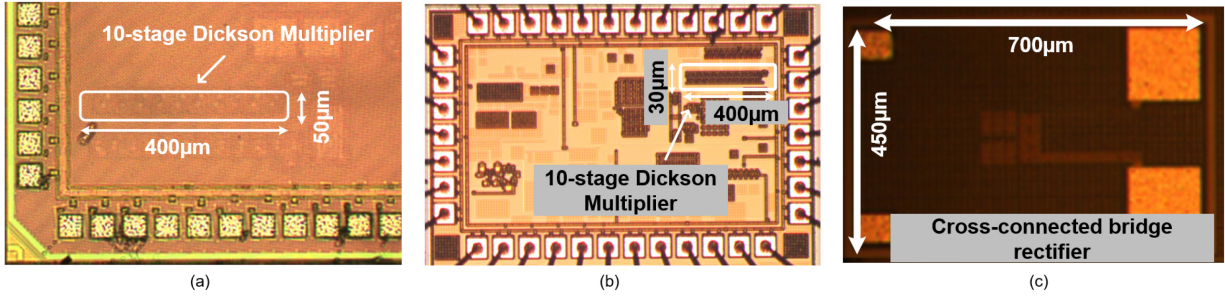
FIGURE 16. (a) Die micro-graphs of a 10-stage Dickson-multiplier rectifier in 65-nm, (b) 130-nm CMOS technology and (c) a cross connected bridge rectifier in 180-nm technology.
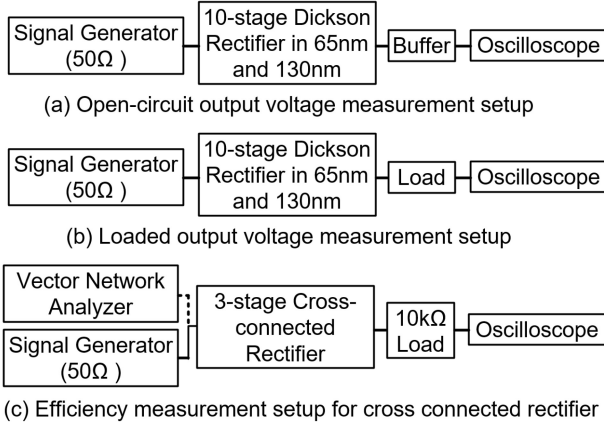

FIGURE 17. Bench-top measurement setup to measure the open circuit voltage and efficiency of rectifier circuits.

test boards designed specifically to minimize the EMI. The induced AC voltages at the output of 3 identical rectifiers from a wireless transmitter have been measured and is found to be 900, 200 and 50 mV, for setups A, B, and C, respectively. EMI in setup B is larger than that of setup C because of the longer PCB traces. Setup A has the largest recorded EMI due to the use of DIP packaging. The Tx coil was placed 5 mm away and was transmitting a 35 dBm 1 GHz power signal. Increasing transmitted power and reducing the Tx-Rx distance increase the effect of EMI.

V. MEASUREMENT RESULT

To verify our analysis and design principles discussed in Section II, we carried out three different chip designs. We designed 10-stage Dickson rectifier circuits in 65nm and 130nm CMOS technologies and a 3-stage cross connected bridge rectifier in 180-nm SoI technology. Measurement setup is presented in Fig. 17. For the open circuit output voltage measurement, a buffer is used to prevent from loading effect of the oscilloscope and the output voltage is read from oscilloscope for loaded Dickson rectifier and cross-connected rectifier while the input power of the rectifier is the product of the power given by the signal generator and the reflection coefficient measured by Vector Network Analyzer (VNA). The purpose of 10-stage Dickson rectifier was to verify no-load/light load output condition while

cross coupled design was carried out for maximum efficiency design.

A. SINGLE-ENDED CONVENTIONAL DICKSON RECTIFIER

The 10-stage rectifier circuits were developed with minimum sized transistors in each of 65nm and 130nm technologies. For the 65nm rectifier design, we used *n*-MOS transistor size of 200nm/60nm while the 130nm design used *n*-MOS transistor size of 160nm/120nm. Both designs use approximately 200fF metal-insulator-metal (MIM) capacitors to implement the rectifier capacitors. Fig. 16 shows the die-micrograph of the two designs. Fig. 16a shows the die-micrograph of the 65nm design which has an area of $400 \times 50 \mu m^2$. Fig. 16b shows the die-micrograph of 130nm design and it has an area of $400 \times 30 \mu m^2$. 130nm technology offers higher density MIM capacitor and consequently has lower area. Fig. 16c shows the die-micrograph of 3-stage cross coupled design in SoI technology. This design included large bond-pads to be able to probe the rectifier inputs. Its size is $450 \times 700 \mu m^2$.

The Dickson multiplier designs were additionally targeted to generate higher output voltage which is desirable for animal tissue stimulation. Our designs target a high output voltage from -10 dBm to 0 dBm incident power which is below the specific absorption rate (SAR) requirement mandated by FCC. Therefore we adopted 10 stages to amplify the limited input swing. Fig. 18 presents the measured output voltage at open circuit condition and at $1M\Omega$ load condition of the Dickson multiplier manufactured in 65-nm ($V_{TH} = 0.48V$) and 130-nm CMOS ($V_{TH} = 0.35V$) technology respectively. The measured open circuit output voltage for both designs are close to each other and supports the notion that the technology or transistor type does not have a large impact on the open circuit output voltage as laid out in our analysis and eq. (19) with respect to no-load output voltage in a Dickson stage. It also shows a linear output voltage with respect to the input at the ultra-low-power condition which further verifies our analysis in Section II. The linear output of both rectifiers as well as their similar output voltages despite the technology difference agrees with our no-load analysis.

As the 10-stage rectifier designs in both technologies were carried out with minimum sized transistors, they are not

TABLE 3. Performance comparison with previous energy harvesting circuits.

	TCAS-I'15 [13]	TCAS-I'17 [31]	JSSC'17 [32]	TBioCAS'18 [33]	JSSC'19 [34]	TCAS-I'19 [5]	JSSC'19 [7]	JSSC'21 [35]	**This work**
Technology	$0.13\mu m$	$0.13\mu m$	$0.18\mu m$	$0.13\mu m$	$0.18\mu m$	$0.13\mu m$	65nm	65nm	$0.18\mu m$
Freq (GHz)	0.9 - 0.92	0.953	0.915	1.3	0.915	0.896	2.45	2.45	1.05
Area (mm^2)	0.25	0.095	2.3×2.3	0.2×0.2	0.61×0.65	0.2×0.3	0.005×0.025	NA	0.315 (max.)
Application	IoT	IoT	IoT	IMD	IoT	IoT	IoT	IoT	Implants
Architecture	Adaptive threshold compensated	Differential cross-coupled	Reconfigurable 8-stage	Cross-connected bridge	Reconfigurable 12-stage	V_{TH} compensated	Cross-coupled	Cross-coupled	Cross-connected
# of stages	12	3	1,2,4,8	4	2,3,4,6,12	4	1	1	3
Pin (μW) @ Peak PCE	32	3162	1000	36	1260	316	500	38.9	631
Load @ Peak PCE	$1M\Omega$	$2k\Omega$	N/A	N/A	MPPT controller	$300k\Omega$	PMU	PMU	$10k\Omega$
Sensitivity	-20dBm @ 1V Vout	-8dBm @ 1V Vout wtih 50kΩ	-14.8dBm@ 1V Vout	N/A	-18.1dBm@ 1V Vout	-20.5dBm @ 1V Vout	-22.7 dBm @0.4V Vout	-26.7 dBm @0.4V Vout	-10dBm @ 1V Vout with 470kΩ
MN	off-chip	none	on-chip	none	off-chip	off-chip	off-chip	off-chip	**none**
Peak PCE	32%	73.9%	25%*	38%	36%*	35.5%*	48.3%	32.3%	**45%**

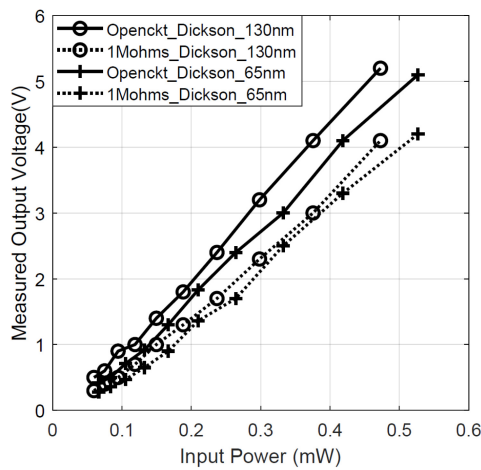*End-to-End efficiency including the reflection loss

FIGURE 18. Measured output voltage comparison of traditional 10-stage Dickson multiplier at 950MHz between 65nm technology and 130nm technology.
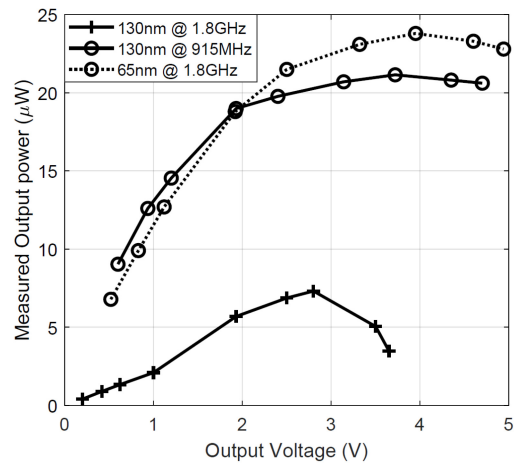

FIGURE 19. Measured maximum output power with different output voltage at −2 dBm input power.

optimized for PCE. Fig. 19 demonstrates the received output power at fixed −2 dBm input power with different output voltage by changing the load resistance. It can be observed that there is an optimal output condition for each energy harvester design that draws the maximum power. Due to the existence of the ESD diode, the output voltage cannot go higher than 5V but this trend is still visible in the figure. After the peak-power, the output power decreases, a trend that is predicted by our maximum power analysis carried out in Section II. The measured output voltage trend agrees with eq. (9). This conclusion is meaningful because if the load condition of certain application is known beforehand, the energy harvester can be optimized to provide the most amount of power. It can also be noticed that, at the same received power level, the rectifier with 65nm outperforms the one with 130nm at high frequency, i.e., 1.8GHz

due to the high driving current of 65nm transistor. Our analysis on loaded output condition also indicates that transistors with higher drive current will supply higher power. However, when the RF signal frequency goes down to sub-GHz, this advantage become less significant because while both devices are well matched, the input voltage amplitude is larger at low frequency than the voltage at high frequency, which contributes to the similar performance shown in the figure.

B. CROSS CONNECTED BRIDGE RECTIFIER

Following the design flow to optimize the parameters mentioned in the previous section, we implement the 3-stage conventional cross connected bridge rectifier in 180-nm SOI technology and its die photo is demonstrated in Fig. 16c.
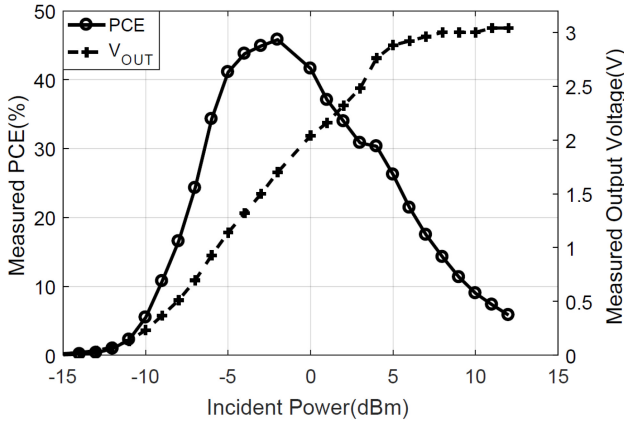
FIGURE 20. Measured rectifier efficiency and output voltage with 10 kΩ load resistor vs. incident power of the cross-coupled differential rectifier.

This design is optimized for maximum efficiency. The measurement results is shown in Fig. 20 which shows that we achieve a maximum PCE of 45% at −2 dBm. Further the peak power behavior also confirms our analysis carried out in Section II.

We further compared our 3-stage cross connected bridge rectifier in terms of PCE and other typical rectifier metrics with the state-of-the-art compact RF energy harvesting circuits in Table 3. For PCE, we mostly compare our $0.18\mu m$ design with other designs. We achieve a peak efficiency of 45% which is among the best reported PCE. The peak efficiency is achieved at a $10k\Omega$ load with −2dBm in power. This design is designed with a 50Ω termination so it doesn't require a matching network. And our 10-stage Dickson rectifiers serve different purpose of high output voltage operation so it's not included in the comparison table. Further, using eq. (15), peak PCE is given by $0.667 \cdot (1 - \eta V_{TH}/kV_A)$. Using the value of $V_{TH} = 0.2$ and $k = 0.87$ (obtained from simulations), the peak efficiency comes out to be 48%. Our peak efficiency results shows conformation with the mathematical derivation of efficiency in Section II.

VI. CONCLUSION

This paper reviews and provides analysis for common circuit topologies for RF CMOS rectifiers for energy harvesting applications using square-wave approximation technique. Mathematical analysis of the operation of a half-wave and multi-stage n-MOS based rectifier, which is widely used in ultra-low-power energy harvesting applications such as IoT sensors, wearable applications, and miniaturized n-IMDs, is also presented in this paper. The analysis is conducted keeping in consideration that the RF power gathered in these applications is generally very low due to attenuation and propagation loss in the medium, and the relative small coil or antenna dimensions. Open circuit and loaded output conditions of the rectifier are discussed to meet different application requirements. The analysis shows that the output voltage in no-load condition does not depend on

the transistor's V_{TH}. The square-wave approximation analysis also provided an upper limit of rectifier efficiency of 66.7%. The other design considerations like the stage selection, flow of designing the RF energy harvesting system, matching network design, the impact of bondpads ESD, and EMI effects are also covered in this paper. Measurement results are presented to show the characteristics of a 10-stage Dickson multiplier in 65nm and 130nm CMOS technologies and a 3-stage cross connected rectifier in $0.18\mu m$. Measurements of open circuit and loaded output condition were performed to verify analytical results. Measurement of open circuit voltage, output power characteristics, and peak efficiency show agreement with the theoretical analysis. Further these design methods were used to achieve a 45% efficient rectifier which is in close agreement of our mathematically obtained peak efficiency of 48%.

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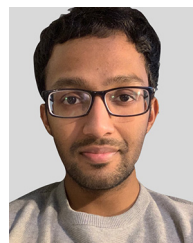
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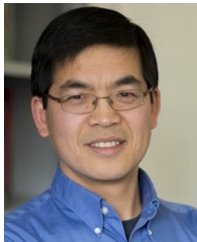
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