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Subthreshold-based m-sequence code generator for ultra low-power body sensor nodes

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Abstract—power dissipation is one of the challenges of body sensor nodes (BSNs) transceivers in which ultra low power consumption is essential for the sensor QoS. In this paper, m-sequence code generator designs for different code lengths are presented and analyzed to demonstrate their efficiency within the region of subthreshold voltage. The proposed m-sequence generators are investigated at a transistor level and their quality and reliability are verified using the auto-correlation and eye diagram characterizations. The maximum switching frequency is obtained at different supply voltages and the power consumption is measured at the maximum achieved frequencies. Simulation and results reveal the capability of our design schemes to work efficiently within the region of subthreshold voltage.

Index Terms—m-sequence code, LFSR, flip-flop (FF), power consumption, CMOS design.

Fig. 1. Some medical applications of BSNs.

I. INTRODUCTION

Body sensor nodes (BSNs) are used in many areas due to the development of wireless communication techniques. Recently, BSNs have been deployed in medical applications to improve and monitor human health as it can be placed in/on the human body, as shown in Fig. 1. In medical sensor nodes, the transceiver design is faced with numerous challenges in terms of power dissipation, size restrictions and power supply [1]. The use of large power supply (battery) will cause the node to be uncomfortable to wear, unlike the little battery which obliges regular changing and decreases patient compliance. Energy harvesting is an alternative technique to power the transceiver of the node with a continuous energy through converting the ambient energy to electrical energy [2]. However, the performance of energy harvesting technique varies based on the type of the harvester which is, in general, provides relatively low power. Thus, the need for an ultra low power wireless transceiver becomes essential to overcome the limitations of conventional batteries and to be within the capabilities of existing harvesters. Spread spectrum is one of the common transmission techniques used by the transceiver. It enhances the link quality by spreading the user data to a wider bandwidth as well as has the ability to resist the jamming. Pseudo-noise (PN) code has been used to spread the information signal by multiplying the PN code by the user data [3]. However, the transceivers that deploy spread spectrum have a complex system structure and tend to consume large power. Thus, designing a low-power and complexity PN code
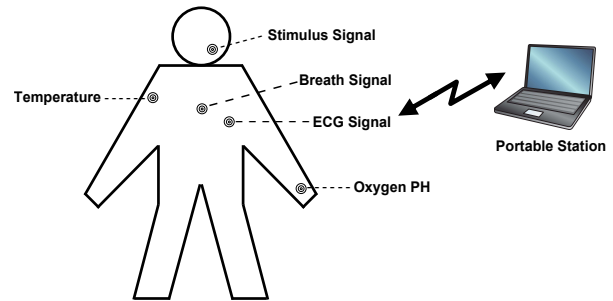
generator can lead to enhanced efficiency. Moreover, the use of CMOS electronic circuits in such applications has boosted their performance and reduced their size and power consumption [4]. Therefore, it is essential to analyze the power dissipation of CMOS implementations to investigate the effect of variations of the supply voltage and switching frequency on power consumption.

Maximum-length sequence (m-sequence) is one of the PN code types that plays a key role in many communication technologies such as spread spectrum. Numerous digital circuits have used m-sequence code due to its simplicity in the design and stability in generating the code using a linear feedback shift register (LFSR) [5].

In this paper, we focus on the design and implementation of an m-sequence code generator circuit at a transistor level to operate at ultra low power consumption that can be used in conjunction with a spread-spectrum transceiver. The contributions of this paper can be summarized as follows:

1) Designing a low power consumption m-sequence code generator circuit that can produce a code within the region of subthreshold voltage.
2) Modifying the conventional flip-flop to be used for the code generator circuit and to provide low power consumption, small cell size and satisfactory performance.
3) Providing a comprehensive analysis of the power consumption at a transistor level.

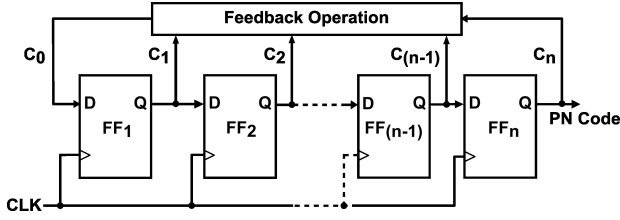The remainder of the paper is structured as follows: Section

Fig. 2. General schematic of m-sequence code generator.

TABLE I
SOME FEEDBACK TAPS OF LFSR [3].

Number of stages N	Code length $L = 2^N - 1$	No. of possible codes	Feedback polynomials (Octal form)
3	7	2	13
4	15	2	23, 37
5	31	6	45, 75
6	63	6	103, 155
7	127	18	211, 217
8	255	16	435, 551
9	511	48	1021, 1131
10	1023	60	2011, 2415

II presents the concept of m-sequence. In Section III, the circuit design and its implementation are introduced, while the measurement results are given in Section IV. Finally, the paper is concluded in Section V.

II. CONCEPT OF m-SEQUENCE

m-sequence code is a cyclic sequence which consists of binary numbers of 1's and 0's in a pseudo-random way [6]. Among different flip-flop (FF) types, D-FF is used in this paper where registers are connected linearly to form a shift register. The outputs of the FFs of the shift register are combined using an exclusive-OR (XOR) gate to provide feedback to input of the first FF, as shown in Fig. 2. Additionally, a clock distribution network is required that activates the FFs. The length of the resulting code depends on the number, N, of shift registers. A maximum code length of $L = 2^N - 1$ bits can be generated if the feedback connections are selected based on a primitive polynomial [7]. The initial state of the LFSR, referred to as the *seed*, controls the code phase [6]. All initial states are allowed, except the all-zero state, as it leads to an all-zero bit sequence. Table I shows feedback tap connections for different length sequences.

III. CIRCUIT DESIGN AND IMPLEMENTATION

In this section, a CMOS circuit design for an m-sequence code generator is proposed. The power consumption for different code lengths and switching frequencies is investigated and analyzed at transistor level. For investigation purposes, three m-sequence code generators are implemented for code lengths of 7, 31 and 511 bits. The m-sequence code generators can be represented in terms of polynomials of variable x such that

$$13_8 \equiv 1011_2 : \quad f_1(x) = x^3 + x + 1, \text{ for } N = 3, \quad (1)$$

$$45_8 \equiv 100101_2 : f_2(x) = x^5 + x^2 + 1, \text{ for } N = 5, \quad (2)$$

$$1021_8 \equiv 1000010001_2 : f_3(x) = x^9 + x^4 + 1, \text{ for } N = 9, \quad (3)$$

where N is the number of FFs and the subscripts 8 and 2 denote octal and binary number representations of the primitive polynomials.

In this paper, three different stages of LFSR are implemented by Cadence simulator using 90 nm CMOS technology. As shown in Table I, different number of feedback taps can be used to build the feedback operation of the generator. However, only two feedback taps are used in the proposed implementation to minimize power consumption, whereby the feedback is constructed using two inputs of XOR gates.

A. Flip-Flop CMOS Design

In VLSI systems, FFs might dissipate a power up to 60% of the total circuit power dissipation [8]. Therefore, an efficient FF design may significantly enhance the circuit power consumption. In this paper, a positive edge-triggered D-type FF is utilized to construct the shift register. The suggested D-type FF consists of two latches that are connected in cascade.

In literature, various circuits of D-FFs are proposed and investigated for low power application, each of which has its own pros and cons [9], [10], [11], [12]. Optimal D-FF designs must achieve a trade-off between the number of transistors (circuit size) and the functionality at ultra low voltage supply. In practice, conventional FFs are used in chip design, where they provide moderate power consumption, small cell size and well performance [13].

The schematic diagram of the modified transmission gate (TG)-based D-FF is shown in Fig. 3. The suggested design is based on conventional TG FF with major additions to the basic structure. Two more inputs PRESET and CLEAR are added to the conventional circuit as these inputs are needed to load each FF in the m-sequence generator with an initial bit (*seed* bit). The PRESET input is used to get high voltage on the output Q regardless of the value of the input D, and it can be activated by a logic 0. Moreover, the CLEAR input is used to get low voltage on the output Q regardless of the value of the input D, and can also activated by a logic 0. To demonstrate the effect of PRESET and CLEAR on the output waveform, the transient response of the modified FF is illustrated in Fig. 4. The results were obtained via simulation carried out in Cadence at a clock frequency of 200 MHz and a VDD voltage of 500 mV.

Conserving chip area while operating the circuit at ultra low supply voltage is achieved by appropriately dimensioning the transistors using matching conditions. To this end, the same channel length is selected for all transistors, so that matching can be achieved by designing the width of the pMOS transistor to be two to four times the width of the
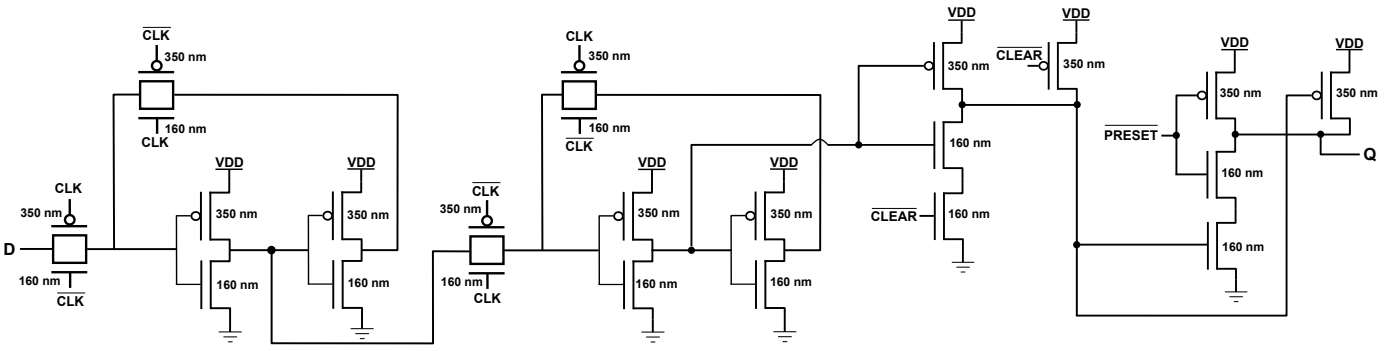
Fig. 3. Modified TG-based D-FF with PRESET and CLEAR.

nMOS transistor. Furthermore, the minimum width of the later is one and a half times the size of the channel length [14]. Matching the transistors leads to improved dynamic performance of the circuit since the low-to-high, (t_{PLH}), and high-to-low, (t_{PHL}), propagation delays are equalized. The numerical values next to the transistors shown in Fig. 3 represent the optimized channel width of each transistor.

B. Exclusive-OR CMOS Design

Two input XOR gates are required to perform the feedback operation of the m-sequence generator. In this paper, different designs of XOR circuits are compared and evaluated in terms of propagation delay and power consumption [15], [16], [17], [18]. In Fig. 6 (a), a pass transistor logic style is characterized by its low power consumption at low supply voltages, however, it produces a very poor output for some input combinations. A static inverter has been used in another design presented in Fig. 6 (b). Although the existence of a static inverter results in a good driving capability, the output waveform exhibits a poor logic 1 when the input pattern changes to 01, and a large delay when the input pattern changes to 00. Fig. 6 (c) shows a TG-based design that surpasses other designs in terms of low power consumption and good delay characteristics over all supply voltages, however, due to the use of an inverter, it requires larger circuit area.

In Fig. 6 (d), a design using 8 transistors is shown with a good output level at low voltages, however, the output deteriorates at higher voltages. In addition, it consumes more power than other designs due to the availability of two static inverters. To overcome the problem of poor output level, a design of 6 transistors and good output level with driving capability is proposed in [17] and shown in Fig. 6 (e), however, it is not efficient in terms of power and delay specifically at low voltages. Another design of 4 transistors based on pass style is presented in [18] and shown in Fig. 6 (f), which is an efficient design in terms of power, nonetheless, it suffers from the same problem of poor delay characteristics due to its limited driving capability.
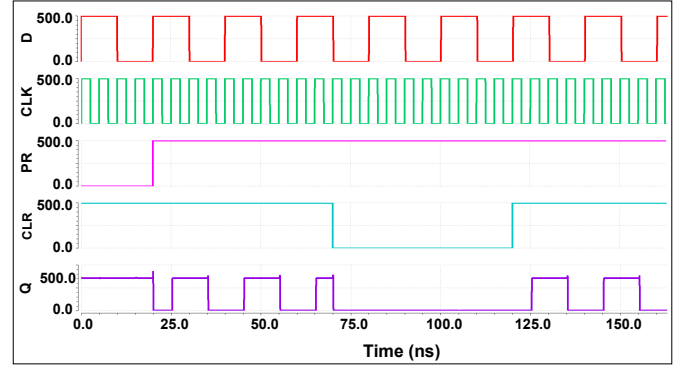

Fig. 4. Transient response of the modified FF, the magnitude of all waveforms is in (mv).

The power consumption of each design shown in Fig. 6 is computed by Cadence simulator and a comparison between them is illustrated in Fig. 5, where we can clearly see that the TG-based design shown in Fig. 6 (c) is consuming significantly less power than other designs for varying supply voltages. Owing to these results, this design is chosen to be included in our work as a feedback function for the m-sequence generator.
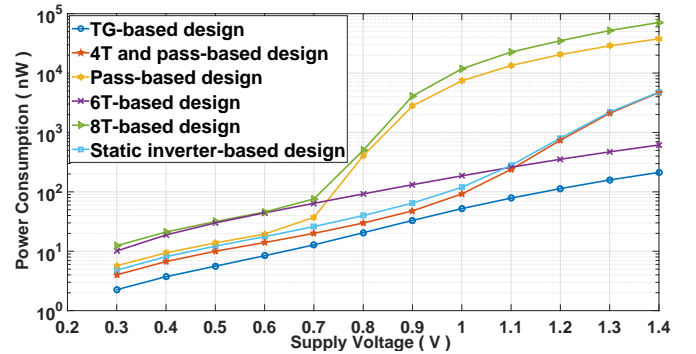

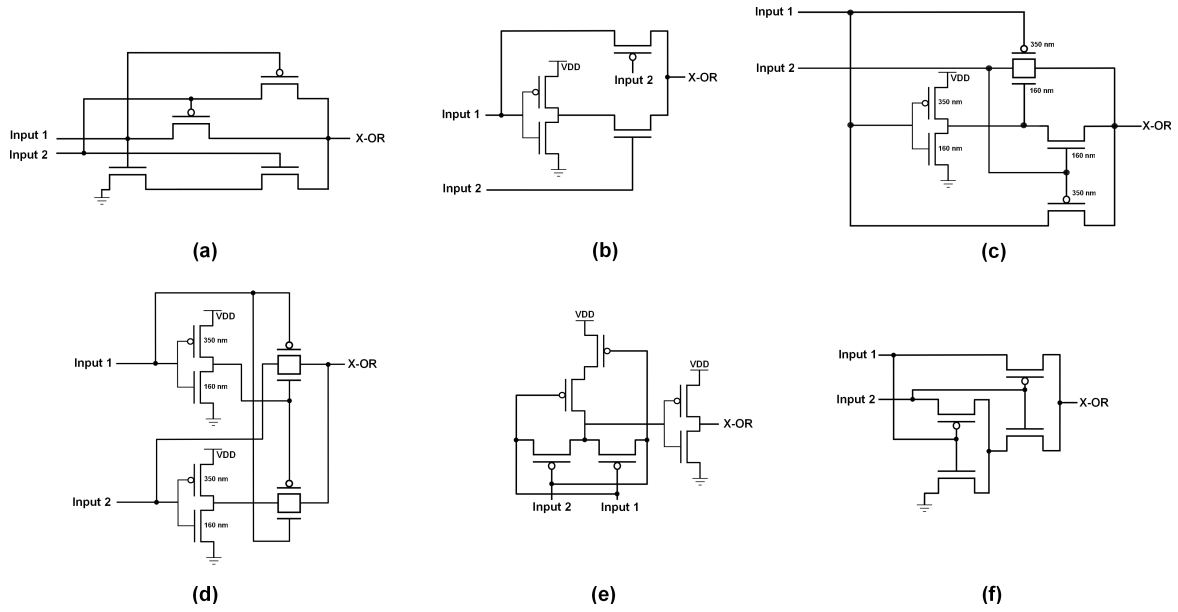
Fig. 5. Power consumption of different XOR designs.

Fig. 6. Different XOR Designs.

C. Architecture of 7-bit m-sequence Generator

To generate a 7-bit m-sequence code, a 3-stage of LFSR are used as shown in Fig. 7. According to the feedback polynomial described in (1), the activated feedback taps are c_1, and c_3. The phase of the generated code depends on the initial seed of the LFSR. The seed value can be determined using PRESET and CLEAR, where both of them can be activated with low voltage. Control and high voltage signals are used to activate or deactivate the PRESET and CLEAR of each FF. The control signal is used to activate the PRESET and CLEAR, and to load the FF with a logic `1` or `0`, respectively. The control signal consists of two states; the low voltage state is used for one clock period for activation purposes, while the high voltage state is utilized for deactivation.

Fig. 7 illustrates how to load the FFs with a seed of `010`. The control signal needs to be connected to CLEAR of the first and third FF, and to the PRESET of the second FF to generate the code `1001110`.

For analysis purposes, further code generators are required to determine the effect of the switching frequency and supply voltage on the power consumption of the circuit. Therefore, two more m-sequence of 31-bit and 511-bit code generators are implemented to assess the reliability of the codes produced as a function of the aforementioned constraints.

IV. SIMULATION AND RESULTS

A. Auto-correlation

The property of auto-correlation of m-sequence code is one of the reliable methods to assess the quality of our generators.
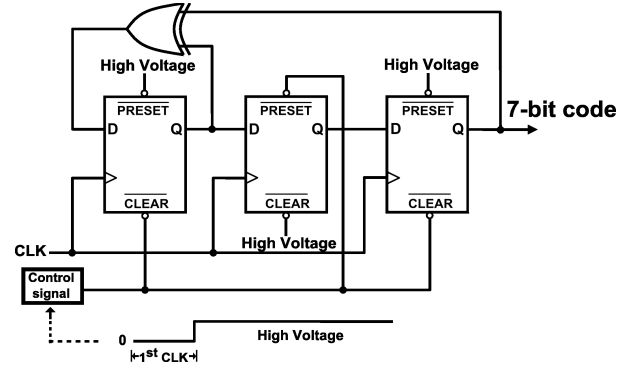

Fig. 7. 7-bit m-sequence code generator producing the code `1001110`.

The sample auto-correlation function of a discrete sequence $x(n)$ is mathematically defined as

$$R(\tau) = \sum_{n=0}^{L-1} x(n)x(n+\tau), \qquad \tau = \pm 1, \pm 2, \ldots, \quad (4)$$

where the correlation lags are presented as follows

$$R(\tau) = \begin{cases} L & \text{when } \tau = 0 \\ -1 & \text{when } \tau \neq 0 \end{cases}. \quad (5)$$

The resulted auto-correlation has an impulse shape with a peak amplitude proportional to the code length L. We successfully tested the output of the three designed generators at different voltages and frequencies. However, we only present

the output result of the 9-stage code generator. Fig. 8 (top) shows a single period of the 511-bit code generated at a clock speed of 130 MHz using a supply voltage of 0.3 V. Although the used clock speed was the maximum frequency that achieved when the supply voltage is 0.3 V, the output sequence still retains its characteristics within the subthreshold region. The sample auto-correlation of the complete 511-bit code is shown in Fig. 8 (bottom) demonstrating the reliable detection of the generated code.
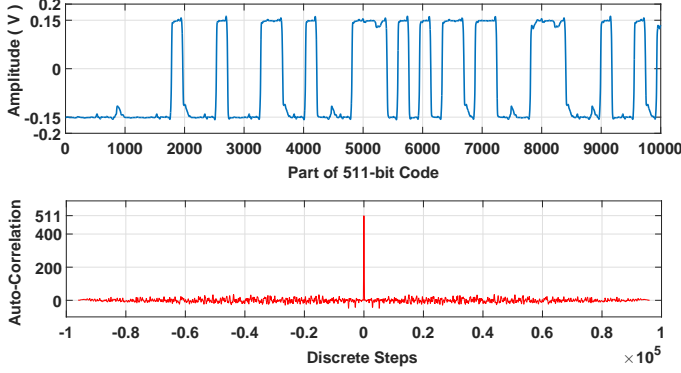

Fig. 8. 511-bit m-sequence code and its auto-correlation function.

Fig. 9. The top eye diagram is measured at 20 MHz whereas the bottom eye is measured at 130 MHz.

B. Eye Diagram

Further analysis using the eye diagram is introduced to assess the quality of the output sequence. The results of eye diagrams did not show any significant noise in all produced codes of each generator. The output eye diagrams depicted in Fig. 9 are measured at 0.3 V using the Cadence simulator and reveal a norrowing of the eye openings at high frequencies. However, the eye opening still permits the detector to distinguish clearly between logic 1's and 0's at ultra low voltages and high frequencies. One unanticipated finding is the asymmetry in the eye opening as the crossing point is marginally closer to the logic 1 voltages. The asymmetry problem is due to amplitude distortion as shown in Fig. 8 (top), where the logic 1 pulse duration is longer than its logic 0 equivalent.

C. Power Consumption and Frequency Analysis

In order to validate the performance of the design, three m-sequence code generators, i.e. for 7, 31 and 511 bit codes, are analyzed and compared using Cadence IC simulator. The simulation is carried out using 90 nm CMOS technology. For comparison purposes, a unified transistor size is utilized for all FFs and XOR gate in each generator. In Fig. 10, the average power consumption P_{avg} of the three code generators is measured at the maximum achievable code frequency and for different supply voltages. The measured power consumption includes the static and dynamic powers, denote as P_s and P_d, respectively, defined as [14]
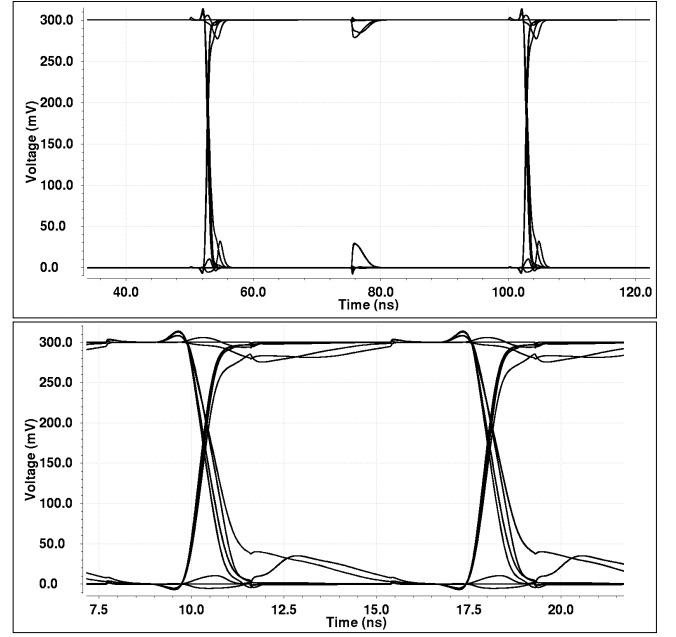
$$P_{avg} = P_d + P_s, \tag{6}$$

where P_s refers to the consumed power in the absence of transistor switching and depends on V_{dd} and leakage current $I_{leakage}$, i.e.

$$P_s = I_{leakage} V_{dd}, \tag{7}$$

where $I_{leakage}$ is attributed to the parasitic elements of the CMOS transistors. From Fig. 10, it is obvious that the code generators show an increasing power consumption with the increase of supply voltage and code length. This is attributed to the fact that the dynamic power consumption P_d of CMOS digital circuits depends quadratically on the supply voltage V_{dd}, and linearly on the capacitance load C_L, and switching frequency f, that is

$$P_d = f C_L V_{dd}^2. \tag{8}$$

Therefore, optimizing the voltage level can significantly mitigate the power consumption of CMOS circuit.

Further analysis is performed by measuring the maximum frequency of each code generator, where the circuit can produce the output sequence without any flipped sign chips. It is interesting to note that the maximum obtained frequencies, shown in Fig. 11, for the three generators have the same values as the supply voltage in the range between 0.3 and 0.7 V. However, the 7-bit code generator exhibits higher switching frequency over the other code generators at a supply voltage ≥ 0.8 V due to lower number of FFs required, which in

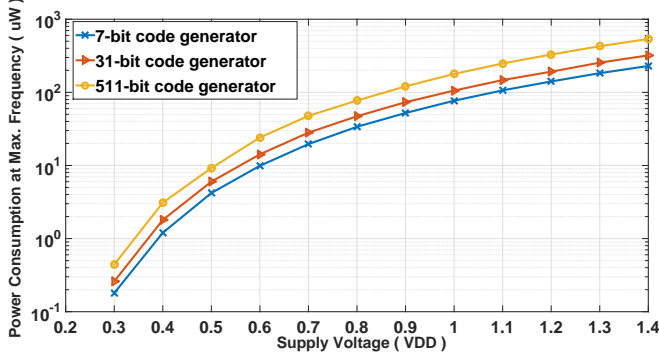turn enables faster operation at the same power supply voltage level.

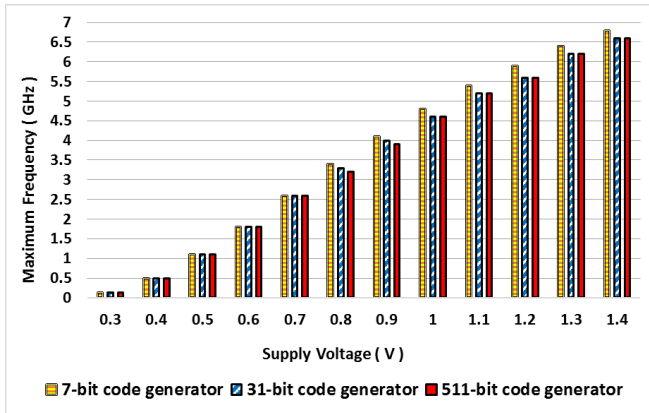Fig. 10. Variation of power consumption with VDD for three m-sequence code generators.

Fig. 11. Maximum frequency of three m-sequence code generators.

The code generators will be used in conjunction with spread spectrum-based BSNs, so it is profoundly advantageous to investigate the effect of generators heat out, produced from the consumed power, on the human body. The temperature difference ΔT between the code generator and the human body is computed using the relationship of heat flow [19], that is,

$$\Delta T = \frac{Q \times L}{K \times A},\qquad(9)$$

where ΔT is calculated as a function of the power Q (W) consumed by the code generator at maximum achievable frequency, the distance L (m) between the code generator device and the human body, the physical dimensions of the device A (m^2) and the thermal conductivity K (W/m$°$C) of water in 37 $°$C. In our calculations, K=0.629 and we assumed that the dimensions of the generator is 0.5 cm^2 and the distance L=1 cm.

Fig. 12 shows that increasing the supply voltage from 0.3 to 1.4 V for the three code generators is safe for the human health as it does not exceed the temperature raising limit of 1$°$C recommended by International Commission on Non-Ionizing Radiation Protection (ICNIRP)[20].
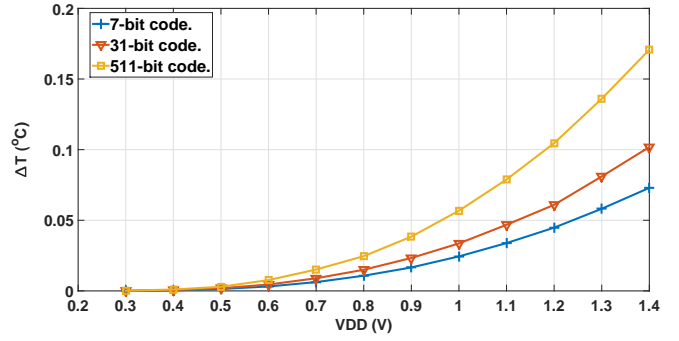

Fig. 12. The effect of using different code lengths on ΔT over a range of VDD values.

V. CONCLUSION

In this research, we proposed an m-sequence code generator design using a TG-based modified FF. Three different code length generators were implemented and their performance was assessed at a transistor level. The power consumption analysis of the proposed design demonstrated the significant implications for the understanding of how to achieve a critical balance between the power consumption and the code length. Furthermore, the output of each code generator was evaluated using the auto-correlation and eye diagram characterization to demonstrate the quality and reliability of the code. It was shown that all three generators can achieve approximately the same maximum allowable switching frequency within a supply voltage region between 0.3V and 0.7V. Thus, a balance must be achieved between the power consumption and the length of the generated code. The preference of one code generator over another is adhered to the detection efficacy, error rate, power consumption and immunity to channel changes. The longest the code generator leads to highest detection rate, power consumption and immunity to channel changes achieving thus the lowest chip error rate. For ultra low power transceivers, a supply voltage of 0.3, 0.4, and 0.5 V can be used as the maximum achieved frequency at these low voltages is 130 MHz, 500 MHz, and 1.1 GHz, respectively.

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