Modelling Reversion Loss and Shoot-through Current in Switched-Capacitor DC-DC Converters with Petri Nets

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***Abstract*— For a Switched-Capacitor DC-DC converter (SCC) in a low power design, reversion losses and shoot-through currents may lead to substantial efficiency degradations and voltage reductions at the output. These reversion losses and shoot-through currents are caused by undesired conduction in MOS devices under certain combinations of internal SCC signals including clocks. This paper proposes a new method that models reversion losses and shoot-through currents in SCCs with Petri nets, providing a formal way of tracking them. With reachability analysis on the Petri Net models, reversion losses and shoot-through currents can be verified and investigated, which is helpful for avoiding these problems in designs. This paper takes cross-coupled voltage doublers as examples. Analysis examples where these properties are identified are presented, together with the finding of healthy traces, which do not contain them. Besides tool-supported reachability analysis capabilities, the natural causal event traceability of Petri net models allows the design of SCCs and other analog and mixed signal (AMS) circuits to be more transparent and understandable, and hence easier to reason about, debug and validate.**

Keywords—Switched Capacitor DC-DC converter; Reversion loss; Petri Nets; Modeling; Reachability Analysis; Cross-coupled voltage doubler.

I. INTRODUCTION

Power efficiency is a critical issue for Switched-Capacitor DC-DC converters (SCCs) in low power designs. Generally, for maximum power efficiency, an SCC is driven by non-overlapping clocks with a minimal dead-time to avoid the shoot-through current loss, which may be caused by PMOS and NMOS conducting at the same time [1]. However, the use of non-overlapping clocks does not always lead to higher power efficiency. For instance, non-overlapping clocks may cause reversion losses from load to flying capacitors and/or from flying capacitors to power source in the cross-coupled voltage doubler described in [2].

These reversion losses, also known as undesired charge transfers or undesired charge losses, are normally generated in an SCC with NMOS and PMOS device switchers under certain clock and internal signal combinations. For an SCC in low power design, it causes an amount of power loss and results in the degradation of power efficiency, because of the temporary reversal of the power delivery path. To alleviate the problem of undesired power loss, new techniques have been proposed. For example, [2] proposed an improved cross-coupled voltage doubler driven by both overlapping clocks and non-overlapping clocks; [3] proposed a charge pump employing charge transfer switchers with a complementary branch scheme; [4] eliminated the reversion loss by adopting a pre-charge operation and other designs in [5]-[6] utilized extra level shifters or blocking transistors to avoid the reversion loss.

However, these papers describe and analyse the reversion losses by natural language descriptions, intuitive diagrams and verbal reasoning. They do not provide a formal way to verify if reversion losses occur in their proposed SCCs.

In addition, certain state of the art high efficiency designs [16]-[17] seem to overlook reversion loss problems and just employed non-overlapping clocks directly without any further clock signal analysis.

Petri nets, first introduced in the early 1960s [7], have been widely used in the areas of concurrent systems, distributed control systems, manufacturing, etc. [8]. They can be used for the modelling and analysis of a wide range of systems in different aspects [9]-[11]. For example, in the asynchronous circuit design area, they can be employed to detect deadlocks and hazard problems [12].

A Petri net SCC model could potentially help verify and detect reversion losses and shoot-through currents. With the appropriate representation of reversion losses and shoot-through current events as states, qualitative verification can be realized by reachability analysis, with which all possible states of an SCC can be explored and investigated. Consequently, related traces leading to a reversion loss or shoot-through current can be detected and healthy traces that do not cause these events may be captured. Analysis tools for Petri net, such as Workcraft [13] and Petrify [14], provide researchers and engineers with systematic ways to verify and detect these energy efficiency issues in an SCC design. This is especially important for systems of larger size and higher complexity, which may present difficulties for ad-hoc analysis.

In [15], a form of Petri nets, known as signal transition graphs (STGs), was extended to form SC-STGs for modelling SCC behaviours. The SC-STG models targeted the functional correctness of SCC designs by focusing on causality and concurrency relations in SCCs, as well as explicitly differentiating the multiple voltage levels in these devices, by extending normal STGs, which assume Boolean signals with

two voltage levels. This work demonstrated that Petri net models might be used for the analysis of functional correctness. However, non-functional properties such as energy efficiency were not covered by existing Petri net-based models of SCCs. Issues such as reversion losses and shoot-through currents are not monitored by these models.

In this paper, a method of modelling SCC operations with Petri nets is proposed, to form a formal foundation to support analysis and verification of these types of systems. This method specifically targets the non-functional properties of SCCs such as energy efficiency. The models are then demonstrated to be relevant for the qualitative studies of reversion loss and shoot-through currents.

This paper is organised as follows. Section II prepares the research case by introducing two cross-coupled voltage doublers in paper [2] and discusses reversion losses in these circuits. Section III presents the new modelling approach and corresponding Petri net models for reversion loss and shoot-through current. Section IV provides analysis and discussions for these reversion loss and shoot-through current models and the results obtained by using them. Section V concludes the paper.

II. BACKGROUND

A simple cross-coupled voltage doubler design is described in [2], which is shown in Figure 1(a).

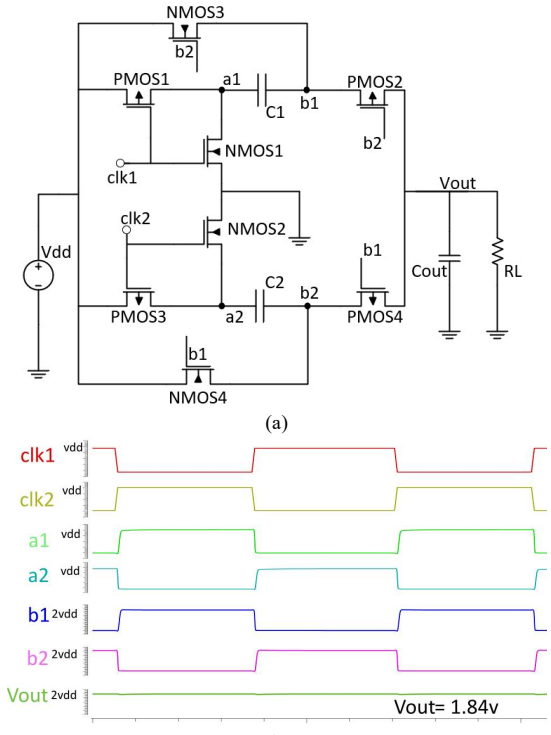


Figure 1. Cross-coupled voltage doubler in [2] and its simulation waveform.

This voltage doubler actually includes two voltage doublers with MOS based switchers. MOS switches NMOS1, NMOS3, PMOS1, PMOS2 and flying capacitor C1 form the first voltage doubler, while the other consists of switches NMOS2, MOS4, PMOS3, PMOS4 and flying capacitor C2. MOS switches NMOS3, NMOS4, PMOS2 and PMOS4 are cross-coupled, since these MOS devices are gated by internal signals from their opposite voltage doublers. These two voltage doublers share a common input Vdd and an output capacitor Cout. Figure 1(b) shows the waveform for this voltage doubler obtained from Cadence simulations (AMS 350nm CMOS technology). In all simulations of this paper, all flying capacitors are set to 100pf, Cout set to 200pf, the frequency of clock signals is 100MHz and the load is 10KΩ.

During phase 1 (clk1=Vdd, clk2=0), a1 is connected to ground and a2 is connected to Vdd. As the flying capacitor C2 was charged to Vdd in the previous cycle, b2 goes to 2Vdd because of the capacitor coupling effect. At the same time, C1 will be charged to Vdd by the end of this phase as b2 turns on switch MOS3. Because b1 is around Vdd and b2 is 2Vdd, PMOS2 is off and PMOS4 is on. As a result, Vout is charged to 2Vdd through PMOS3 and PMOS4. In phase 2 (clk1=0, clk2=Vdd), C2 is recharged to Vdd and Cout is charged to 2Vdd through PMOS1 and PMOS2, again with Vout=2Vdd, which is the aim of 'voltage doubling'. An SC-STG model for this voltage doubler in [15] covers the detailed causality and concurrency relations among all the events. It also tracks the different voltage levels at the signals. A detailed discussion of SC-STG can be found in [15].

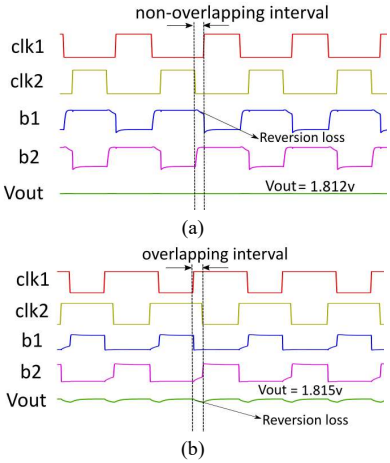


Figure 2. Simulation results for the cross-coupled voltage doubler with (a) non-overpping clocks and (b) overlapping clocks.

However, if this voltage doubler is driven by non-overlapping clocks as shown in Figure 2(a), undesirable reversion loss current occurs during the interval between t1 and t2. Specifically, as clk1 and clk2 are both at ground, a1 and a2 are connected to Vdd and then b1 and b2 are both at 2Vdd. As a result, NMOS3 and NMOS4 are turned on at the same time. It results in reversion loss currents from C1 and C2 to Vdd. As can be seen from the simulation results shown in figure 2(a), there is an obvious voltage drop for the internal signals b1 and b2 during the interval that clk1 and clk2 are both 0. At the same time, the output Vout drops compared with the simulation result in Figure 1(b). It means a lower power efficiency as the energy transferred from Vdd to Vout is reduced.

Another reversion loss current occurs when the clock signals change to overlapping clocks as shown in Figure 2(b). During the time interval that clk1 and clk2 are both Vdd, a1

and a2 are both connected to ground, and b1 and b2 are connected to Vdd. As a consequence, there are reversion loss currents from Vout to C1 and C2 since PMOS2 and PMOS4 are turned on at the same time. It can be seen clearly that a voltage drop occurs during the interval that clk1 and clk2 are both Vdd. As a result, the power effiency reduces because of these reversion losses.

Figure 3 shows the output voltage curves for the voltage doubler under different overlapping and non-overlapping clocks supplying a 10kΩ. Generally speaking, when the overlapping or non-overlapping time gap increases from 0us to 30us, the output voltage of the voltage doubler drops slightly indicating the presence of reversion loss. When the time gap exceeds 35us, reversion losses are such that the device fails to behave as a reasonable voltage doubler, with Vout suffering a subsantantial drop. Interestingly, when both clocks are precisely inverse synchronized, the device shows the greatest Vout values. This phenomenon will be discussed later.

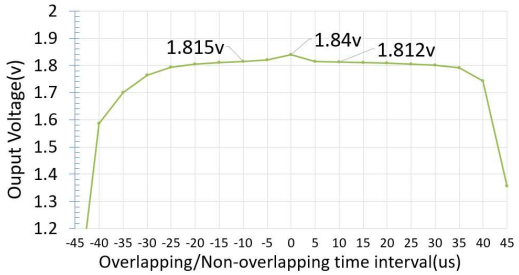


Figure 3. Ouput voltages for different overlapping and non-overlapping clocks.

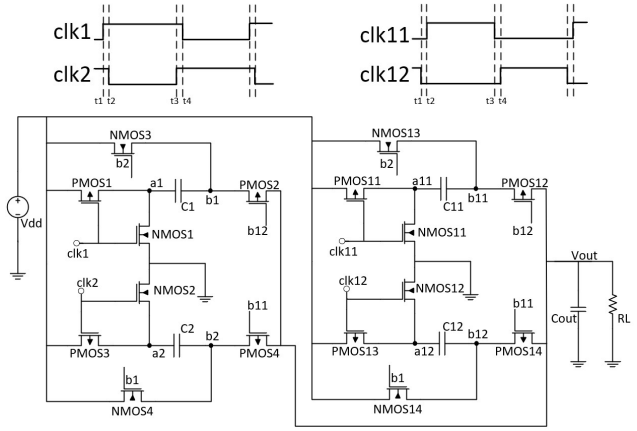


Figure 4. Improved cross-coupled voltage doubler that eminates reversion losses [2].

To solve the reversion loss problem, [2] proposed an improved cross-coupled voltage doubler, which is shown in Figure 4. It includes two copies of the cross-coupled voltage doubler shown in Figure 1. The left one is driven by overlapping clocks while the right one is driven by non-overlapping clocks. In addition, a further level of cross-coupling exists between the two doubler blocks. PMOS2 and PMOS4 are driven by internal signals b12 and b11 from the right cross-coupled voltage doubler instead of b2 and b1 from their own block. Similarly, the NMOS13 and NMOS14 in the right cross-coupled voltage doubler are controlled by internal signals b2 and b1 from the left block.

During the interval t1 to t2, b1 and b2 are both connected to Vdd as described previously. Similarly, b11 and b12 are both at 2Vdd. In this situation, for the left cross-coupled voltage doubler, there is no reversion loss from Vout to C1 and C2 as PMO2 and PMOS4 are closed by signal b12 and b11. For the right cross-coupled voltage doubler, there is no reversion loss from C11 and C12 to Vdd as NMOS13 and NMOS14 are turned off by signals b2 and b1.

Compared to the original voltage doubler (shown in Figure 1), another advantage of this improved voltage doubler (shown in Figure 4) is the elimination of the shoot-through current. In reality, as shown in Figure 5, clock transitions do not happen instantaneously and there is a time interval for the process.

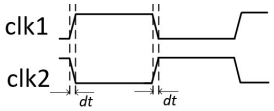


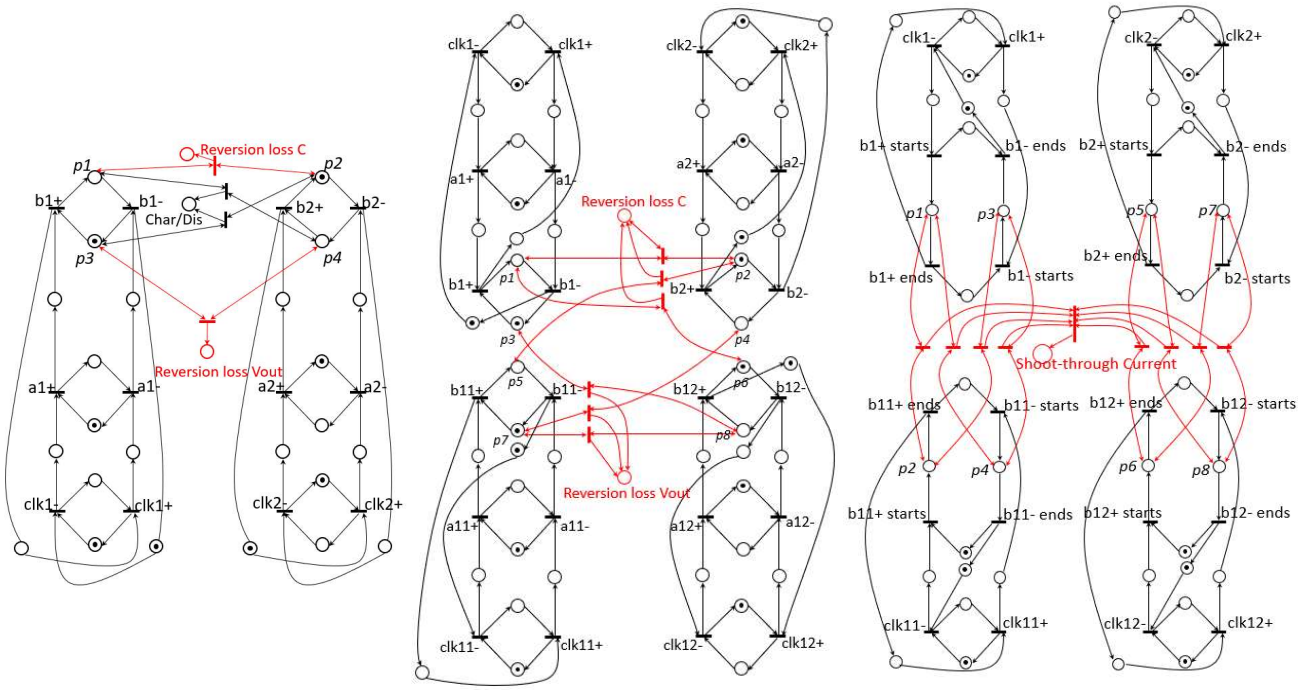
Figure 5. Shoot-through current happens when clock signals transit.

During this rising/falling edge process, PMOS and NMOS may conduct at the same time, which causes a shoot-through current. In the original voltage doubler, since NMOS3 and PMOS2 are both gated by b2, there must be a shoot-through from Vout to Vdd when b1 transits. However, in the improved voltage doubler, PMO2 is controlled by signal b12. There will not be shoot-through current as transitions b12 and b2 do not happen at the same time. To summarise, whether reversion losses and shoot-through currents happen or not is associated with the clock signals, since the MOS devices in the cross-coupled doubler are all controlled by these clock signals or internals signals (associated with clock signals). Therefore, if there is a Petri net that describes all the causality relations between all events in a voltage doubler, including clock events, all the clock signals that potentially result in a reversion loss or shoot-through current can be determined.

III. MODELLING APRROCHING

Formally, a petri net structure C is a tuple $C= (P, T, I, O)$. $P= \{p_1, p_2, p_3, ..., p_n\}$ is a finite non-empty set of places. $T= \{t_1, t_2, t_3, ..., t_m\}$ is a finite non-empty set of transitions. P and T are disjointed, $P \cap T= \emptyset$. I is the input function $(P \rightarrow T)$ while O is the output function $(T \rightarrow P)$. A marking M of a Petri net C is a function from P to the nonnegative integers N. $M: P \rightarrow N$, where $M(p_i)$ is the number of tokens in the place P_i, $i=1, 2, ..., N$.

In a Petri Net graph, places are represented by circles, bar or rectangles represent transitions and oriented arcs mean input functions or output functions. A marking is represented by a set of tokens (solid disks) inside the places of a Petri net, which indicates the current state of the net. These states of the net change with the firings of transitions. A transition is enabled if all of its input places have tokens and an enabled transition may fire. The firing of a transition reduces the number of tokens in every one of its input places by one, and increases the number of tokens in every one of its output places by one.



(a) (b) (c)

Figure 6: (a) Petri net model for the cross-coupled voltage doubler (Char/Dis means the charging and discharging process for flying capacitors C1 and C2); (b) Petri net model for the improved cross-coupled voltage doubler ; (c) Petri net model for the shoot-through current (Partly shown).

In [15], to describe the causality relations between events in a formal way, internal signals variations are represented by a logical transition (e.g. the voltage at a1 changing from 0 to Vdd is represented by a1+). In this paper, we continue to represent signal level changes as transitions. Since in this paper we do not focus on the multiple voltage levels such as 2Vdd and Vdd, we no longer differentiate the different types of + and – signals. We also add explicit places to represent signal values, the combinations of which may indicate reversion losses. We then add monitoring sub-nets for reversion losses to record the occasions when these combinations of signal values occur. Aiming for qualitative analysis, it is not important that we track the number of occurrences of these signal combinations correctly. With reachability analysis in mind, the model must provide and only needs to provide the possibility of monitoring places becoming marked if the monitored events happen.

Based on the above discussions, a Petri net model for the cross-coupled voltage doubler can be derived. This is shown in Figure 6(a).

This Petri net model shows the causality relations among the reversion losses and the internal signals. For example, in this model, we can find that the transition ‘Reversion loss C’ may fire if there are tokens in places p1 and p2 at the same time, which means the reversion loss from capacitor C1 and C2 to Vdd occurs when both b1 and b2 are 2Vdd. In the mean time, the tansition ‘Reversion loss Vout’ may fire when there are token in places p3 and p4, which means reversion loss from the Vout to the capacitor C1 and C2 happens when both b1 and b2 signals are Vdd. On the other hand token pairs in p3 and p2 or in p1 and p4 at the same time indicate that the capacitors in the voltage doubler are having a normal charging and discharging process. Base on the causality relations shown in this Petri net, all the clock signals that may trigger a reversion loss can be traced by using a rechability analysis. Corresponding rechability analysis results will be shown and discussed in Section IV.

Figure 6(b) shows the Petri net model for the reversion losses in the improved cross-coupled voltage doubler found in [2], which contains all events that may happen for two cross-coupled voltage doublers and shows their causality relations. All the charging and discharging processes for the capacitors are removed for simplicity. All states that may include reversion losses are included in this model. For instance, when there are tokens in p1 and p2, the transition ‘Reversion loss C’ may fire as the reversion loss from capacitor C1 and C2 to Vdd occurs when both b1 and b2 are 2Vdd. Similarly, the transition ‘Rerversion loss Vout’ may fire if there are tokens in places p7 an p8 since there is a reversion loss from Vout to the capacitors C11 and C12 when b11 and b12 are both Vdd.

Shoot-through currents can also be modelled in a similar way. But it requires a further extension of the Petri net model. The Petri net model for the shoot-through current in the improved voltage doubler is shown in Figure 6(c) (Some internal signals are removed for simplicity).

In this model, the value changes of internal signals b1, b2, b11 and b12 are represented by two transitions and one place, where the two transitions represent the start and end of the value change and the place represents the relevant value being changed. This is because to check for shoot-through current, we must view the change processes of clock and internal signals as non-atomic. In this way, clock seqeunces that lead to shoot-through currents can also be detected with a reachability analysis.

In this Petri net, the causality relations between the internal signals and the shoot-through current monitoring are described clearly. Take a simple example, when there is a token pair in any of the following pairs of places (p1, p2), (p1, p4), (p3, p2) or (p3, p4) the place for monitoring shoot-through current may become marked. It means that shoot-through current occurs when internal signals b1 and b11 transit at the same time as the token in places p1 or p2. The same arguments lead to the other pairs of places being minitored in the same way.

The method of modelling the reversion loss and shoot-through current in an SCC can be summarized as follows. An SC-STG model of the concurrency and causality relations in an SCC can be firstly derived from a waveform. By using simulations and/or other forms of experimental study, an understanding of the crucial factors that affect the existence of potential reversion losses and shoot-through currents is obtained. Simplifying the SC-STG by removing explicit multiple voltage level representations, adding places monitoring crucial signal values and signal changes, and adding monitoring sub-nets using these additional places lead to Petri net models targeting the issues of reversion loss and shoot-through current. With reachability analyses for these models, clock sequences that enable or not enable a reversion loss (or shoot-through current) can be verified and investigated, which will be helpful for an SCC design.

IV. Analysis

Reachability analysis can be run in Workcraft [13], which provides a flexible framework for the development of interpreted models, including visual editing, simulation and analysis. For any Petri net model, it not only can run any specific reachability analysis but also can provide a correctness check.

Results for the original Cross-coupled voltage doubler.

	clock sequence	Reversion loss Vout	Reversion loss C
1	clk1-,clk1+,clk1-,clk1+	No	Yes
2	clk1-,clk1+,clk1-,clk2+	No	Yes
3	clk1-,clk1+,clk2+,clk2-	Yes	Yes
4	clk1-,clk1+,clk2+,clk1-	Yes	Yes
5	clk1-,clk2+,clk1+,clk1-	Yes	Yes
6	clk1-,clk2+,clk2-,clk1+ (Non-overlapping clocks)	Yes	Yes
7	clk1-,clk2+,clk2-,clk1+	No	Yes
8	clk1-,clk2+,clk2-,clk2+	No	Yes
9	clk2+,clk2-,clk2+,clk2-	Yes	No
10	clk2+,clk2-,clk2+,clk1-	Yes	No
11	clk2+,clk2-,clk1-,clk1+	Yes	Yes
12	clk2+,clk2-,clk1-,clk2+	Yes	Yes
13	clk2+,clk1-,clk2-,clk1+	Yes	Yes
14	clk2+,clk1-,clk2-,clk2+	Yes	Yes
15	clk2+,clk1-,clk1+,clk2- (Overlapping clocks)	Yes	No
16	clk2+,clk1-,clk1+,clk1-	Yes	No
17	(clk1-, clk2+), (clk1+, clk2-), (clk1-, clk2+), (clk1+, clk2-)	No	No

Figure 7. Reachability analysis results for the Petri net in Figue 6(a).

Reachabilty analysis results of the Petri net model shown in Figure 6(a) is shown in Figure 7. Since the results for the model with different initial states are the same because of the model's symmetry, they are not shown here.

If clock signals change one at a time (1 to 16), all the clock sequences cause at lease one reversion loss and most of them cause both types of reversion losses. It is also shown that the so-called overlapping and non-overlapping clock sequences are only sub-sets of all possible clock signal orders. The reversion loss behaviours of these two sequences found from the model agree with those oberved in simulation (cf. Figures 2(a) and 2(b) with rows 6 and 15 in Figure 7).

Interestingly, the result changes when the two clocks clk1 and clk2 change at the same time, the clock transition sequences (clk1-, clk2+), (clk1+, clk2-), (clk1-, clk2+), (clk1+, clk2-) (See row 17 of Figure 7) do not cause any reversion losses. This sequence is acutally the inverted clock signals shown in Figure 1. To investigate if there is any reversion losses generated with these clock signals, a simulation is run in Cadence, the result of which is shown in Figure 8.

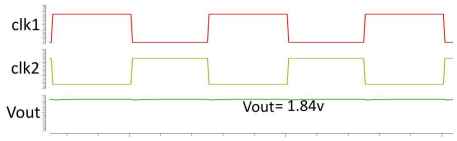


Figure 8. Waveform for the cross-coupled voltage doubler with inverted clock signals.

Compared to the waveforms in Figures 2(a) and Figure 2(b), the waveform in Figure 8 clearly has a higher Vout showing the lack of reversion loss. For the original voltage doubler in Figure 1, it is clear that the only healthy clock sequence that do not cause reversion losses is when both clocks are synchronized and are exact inversions of each other. However, this synchronization of the clocks may cause shoot-through currents, which will be analysed with the more complex example below.

Results for the improved Cross-coupled voltage doubler.

The number of states for the improved voltage doubler is too large to enumerate here. We ignore the clock sequencies that may cause reversion losses and only show the healthy sequences that do not cause reversion losses in Figure 9.

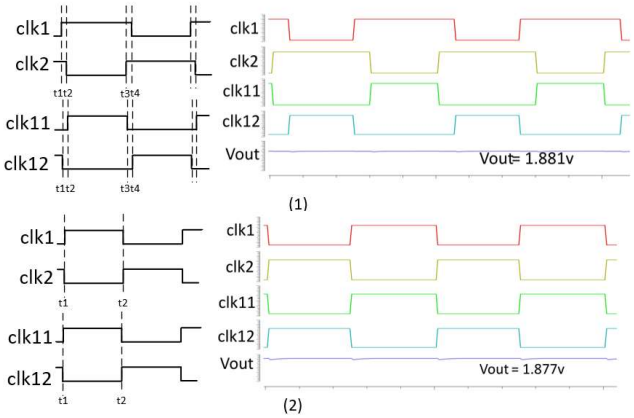


Figure 9. The traced clock signals that will not lead to reversion losses and their simualtion waveforms.

The first clock sequence is proposed in [2]. The second is similar to the synchronized inverse clock signals shown in

Figure 8. This was ignored by [2], most likely because of shoot-through current losses, as discussed below.

In addition, a reachability analysis for the shoot-through current is carried out for these two clock signals. The result shows that shoot-through current is not caused in the improved voltage doubler with the first clock signal (shown in Figure 9(1)), while shoot-through current exists at every clock transit when the improved voltage doubler is driven by the second clock sequence where all clocks are synchronized (shown in figure 9(2)).

Further verifications and discussion for the results.

Cadence simulation results from running the improved voltage doubler with the two clock sequence types are also shown in Figure 9.

Comparing the waveforms, the Vout of the doubler with clock signals (1) has a higher value at 1.881V while the one with clock signal (2) has a lower maximum output voltage at 1.877V. In fact, Vout with clocks (2) is similar as Vout in Figure 8. Both of them get a little voltage drop when clock signals transit, which is caused by shoot-through currents.

It is worth noting that the improved voltage doubler in Figure 4, similar to the original simple voltage doubler in Figure 1, requires the synchronization of inverted clock signals to be free of reversion loss, as shown in Figure 9. For instance, in the scheme of Figure 9 (1), clk1 needs to be precisely synchronized to clk12 and clk2 needs to be precisely synchronized to clk11 to avoid reversion loss. Any misallignment between the relevant clock edges causes reversion loss being found in our reachability analysis. This is qualitatively the same requirement for the simpler voltage doubler, which under synchronized inverse clock signals also exhibits no reversion loss as shown in Figure 7. What the improved doubler achieves is the additional elimination of shoot-through current, once reversion loss has been removed by clock synchonization. Quantitatively, this may not bring a very significant voltage enhancement, depending on the implementation.

In summary, through a reachability analysis for the Petri net models of thoes two voltage doublers, all the clock signals that may cause a reversion loss can be traced and verified. In addition, by stretching the model for singal changes from transitions to places, shoot-through current conditions can also be found with the help of extended models.

V. Conclusion

This paper proposes a new way to model reversion losses and shoot-through current conditions in SCC with Petri nets. By representing all local causality and concurrency relations, this method of modelling allows the straightforward assembly of parts into larger models. By using Petri net places to represent conditions that need checking, this type of model is demonstrated to be useful for verifying the occurrences and causes of properties such as shoot-through current losses and reversion losses in SCCs.

This work demonstrates three advantages of bringing in a formalism such as Petri nets into the study of SCCs. Firstly the distributed representation of Petri nets makes it easy to derive models for SCCs which are fundamentally distributed architectures with distributed signals, switches and capacitors. Secondly, the tool-supported reachability analysis capability of Petri nets facilitates the process of analysis. Thirdly, the natural causal event traceability of Petri net models allows the design of SCCs and other analog and mixed signal (AMS) circuits to be more transparent and understandable, and hence easier to reason about, debug and validate.

There exist types of Petri net extensions that allow quantitative representations and analysis. This work opens up opportunities for future research on the quantitative studies of reversion and shoot-through losses of SCCs.

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