# Fast polar codes for terabits-per-second throughput communications

Jiajie Tong, Member, IEEE, Xianbin Wang, Member, IEEE, Qifan Zhang, Member, IEEE, Huazi Zhang, Member, IEEE, Rong Li, Member, IEEE, Jun Wang, Member, IEEE and Wen Tong, Fellow, IEEE

Abstract—Targeting high-throughput and low-power communications, we implement two successive cancellation (SC) decoders for polar codes. With 16nm ASIC technology, the area efficiency and energy efficiency are  $4Tbps/mm^2$  and 0.63pJ/bit, respectively, for the unrolled decoder, and  $561Gbps/mm^2$  and 1.21pJ/bit, respectively, for the recursive decoder. To achieve such a high throughput, a novel code construction, coined as fast polar codes, is proposed and jointly optimized with a highly-parallel SC decoding architecture. First, we reuse existing modules to fast decode more outer code blocks, and then modify code construction to facilitate faster decoding for all outer code blocks up to a degree of parallelism of 16. Furthermore, parallel comparison circuits and bit quantization schemes are customized for hardware implementation. Collectively, they contribute to an  $2.66 \times$  area efficiency improvement and 33% energy saving over the state of the art.

*Index Terms*—Fast polar codes, Tbps communication, fast decoding, recursive decoder, unroll decoder.

#### I. INTRODUCTION

#### A. Motivations and Background

Higher throughput has always been a primary target along the course of mobile communications evolution. Driven by high data rate applications such as virtual/augmented reality (VR/AR) applications, the sixth generation wireless technology (6G) requires a peak throughput of 1Tbp/s [1]. This is roughly a  $50\times 100\times$  increase over the  $10\sim 20Gbp/s$  target throughput for 5G standards.

To support such a high data rate, we need to propose new physical layer design to further reduce implementation complexity, save energy, and improve spectral efficiency. This is particularly true when the peak throughput requirement is imposed on a resource constrained (limited processing power, storage, and energy supply etc.) device. Since channel coding is well-known to consume a substantial proportion of computational resources, it poses a bottleneck for extreme throughput. To this end, channel coding is one of the most relevant physical layer technologies in order to guarantee 1Tbp/s peak throughput for 6G.

Polar codes, defined by Arıkan in [2], are a class of linear block codes with the generator matrix  $G_N$  of size N, defined by  $G_N \triangleq F^{\otimes n}$ , in which  $N = 2^n$  and  $F^{\otimes n}$  denotes the n-th

Part of this paper was presented in an invited talk at the 2021 International Symposium on Information Theory (ISIT).

Jiajie Tong, Xianbin Wang, Huazi Zhang, Rong Li and Jun Wang are with Huawei Technologies Co. Ltd., China.

Qifan Zhang, Huazi Zhang and Wen Tong are with Huawei Technologies Canada Co. Ltd., Canada.

Kronecker power of  $F = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ . Successive cancellation (SC) is a basic decoding algorithm for polar codes.

Although the SC decoding algorithm seems unsuitable for high-throughput applications due to its serial nature, state-ofthe-art SC decoders [3] [4] [5] [6] [7] managed to significantly simplify and parallelize the decoding process such that the area efficiency of SC decoding has far exceeded that of belief propagation (BP) decoding for low-density parity-check codes (LDPC). In particular, these works represent SC decoding as a binary tree traversal [3], as shown in Fig. 1(a). Each subtree therein represents a shorter polar code. The original SC decoding algorithm traverses the tree by visiting all the nodes and edges, leading to high decoding latency. Simplified SC decoders can fast decode certain subtrees (shorter polar codes) and thus "prune" those subtrees. The resulting decoding latency is largely determined by the number of remaining edges and nodes in the pruned binary tree. Several tree-pruning techniques have been proposed in [3], [8] and [9]. To achieve 1Tbp/s throughput, more aggressive techniques need to be proposed on both the decoding and encoding sides.

#### B. Contributions

This paper introduces a novel polar code construction method, coined as "fast polar codes", to facilitate parallelized processing at an SC decoder. In contrast to some existing decoding-only techniques, we take a joint encoding-decoding optimization approach. Similar to existing methods, our main ideas could be better understood from the binary tree traversal perspective. They are (a) pruning more subtrees, (b) replacing some non-prunable subtrees with other fast-decodable short codes of the same code rates and then prune these "grafted" subtrees, (c) eliminating the remaining non-prunable subtrees by altering their code rates. As seen, both (b) and (c) involve a modified code construction. Consequently, we are able to fast decode any subtree (short code) of a certain size, without sacrificing parallelism.

The algorithmic contributions are summarized below:

1) We introduce four new fast decoding modules for nodes with code rates  $\{\frac{2}{M}, \frac{3}{M}, \frac{M-3}{M}, \frac{M-2}{M}\}$ . Here  $M=2^s$  is the number of leaf nodes in a subtree, where s is the stage number. These nodes are called dual-REP (REP-2), repeated parity check (RPC), parity checked repetition (PCR), dual-SPC (SPC-2) nodes, respectively. More importantly, these modules reuse existing decoding circuits for repetition (REP) and single parity check (SPC) nodes.

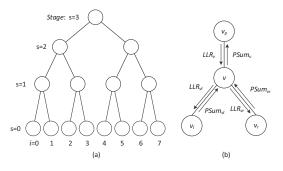


Fig. 1. (a) decoding architecture as a binary tree; (b) node v received/response information

- 2) For medium-code-rate nodes that do not natively support fast decoding, we graft two extended BCH codes to replace the original outer polar codes. BCH codes enjoy good minimum distance and natively support efficient hard-input decoding algorithms, thus strike a good balance between performance and latency. The extension method is also customized to enhance performance.
- 3) We propose to re-allocate the code rates globally, such that all nodes up to a certain size support the above mentioned fast decoding algorithms. This approach completely avoids the traversal into certain "slow" nodes.

For code length N=1024 and code rate R=0.875, the proposed fast polar codes enable parallel decoding of all length-16 nodes. The proposed decoding algorithm reduces 55% node visits and 43.5% edge visits from the original polar codes, with a cost of within 0.3dB performance loss. Two types of decoder hardware are designed to evaluate the area efficiency and energy efficiency.

The implementation-wise contributions are summarized below:

- 1) We design a recursive decoder to flexibly support any code rates and code lengths  $N \leq 1024$ . This decoder layout area is only  $0.045mm^2$ . For code length N=1024 and code rate R=0.875, it achieves a 25.6Gbp/s code bit throughput, with an area efficiency of  $561Gbps/mm^2$ .
- 2) We also design an unrolled decoder that only supports one code rate and code length. The decoder layout area is  $0.3mm^2$ . For code length N=1024 and code rate R=0.875, it provides a 1229Gbp/s code bit throughput, with an area efficiency of  $4096Gbps/mm^2$ .

## II. FROM SIMPLIFIED SC DECODING TO FAST POLAR CODES

Following the notations in [3], a node v in a tree is directly connected to a parent node  $p_v$ , left child node  $v_l$  and right child node  $v_r$ , respectively<sup>1</sup>. The stage of a node v is defined by the number of edges between node v and its nearest leaf node. All leaf nodes are at stage s=0. The set of nodes of the subtree rooted at node v is denoted by v. Thus  $v_{root}$  denotes the full binary decoding tree. The set of all leaf nodes

is denoted by U, the index of a leaf u [3] is denoted by l(u), and the indices of U is denoted by l(U). Meanwhile, the set of the leaf nodes in subtree  $V_v$  is denoted by  $U_v$ , and the indices of  $U_v$  is denoted by  $l(U_v)$ .

The set of all information bit positions is denoted by  $\mathcal{I}$  and that of all frozen bits by  $\mathcal{I}^c$ . The set of the information bit positions in subtree  $V_v$  is denoted by  $\mathcal{I}_v$  and the remaining frozen bit positions therein by  $\mathcal{I}_v^c$ .

#### A. Simplified SC Decoding

If  $\mathcal{I}_v^c$  matches patterns, a so-called pattern-based simplified decoding can be triggered to process the node in parallel rather than bit-by-bit. From the binary tree traversal perspective, all the child nodes of v do not need to be traversed. Thus decoding latency is reduced.

The existing so-called pattern-based simplified decoding includes 4 different types. A node v is a Rate-1 node [3] if all leaves in the subtree  $V_v$  are information bits, and a Rate-0 node [3] if all leaves in the subtree  $V_v$  are frozen bits. To improve the decoder's efficiency, [8] defines single parity check (SPC) and repetition (REP) nodes. We can employ pattern-specific parallel processing for each type of nodes. Obviously, we need to identify and exploit more special nodes or patterns for latency reduction.

In this paper, we present four new types of corresponding nodes:

- Define a node v as a dual-SPC (SPC-2) node if  $V_v$  includes only two frozen bits, and the frozen bits indices are the two smallest in  $l(U_v)$ .
- Define a node v as a dual-REP (REP-2) node if  $V_v$  includes only two information bits, and the information bits indices are the two largest in the  $l(U_v)$ .
- Define a node v as a repeated parity check (RPC) node if  $V_v$  includes only three frozen bits, and the frozen bits indices are the three smallest in the  $l(U_v)$ .
- Define a node v as parity checked repetition (PCR) node if  $V_v$  includes only three information bits, and the information bits indices are the three largest in the  $l(U_v)$ .

We describe their corresponding fast decoding methods in Section III.

Pattern-based simplified decoding skips the traversal of certain subtrees when it matches the above patterns.

Currently, there are eight pattern types to cover eight code rates of a sub tree:  $\{0, \frac{1}{M}, \frac{2}{M}, \frac{3}{M}, \frac{M-3}{M}, \frac{M-2}{M}, \frac{M-1}{M}, 1\}$ . In other words, nodes with other code rates cannot be fast decoded. We need to work on the following two parameters.

- 1) Ratio of simplified nodes: currently eight out of the M+1 code rates support simplified decoding. The ratio is thus  $\frac{8}{M+1}$ . Note that only the lowest and highest codes rates can be simplified, meaning code rates between  $\frac{3}{M}$  and  $\frac{M-3}{M}$  do not benefit from the fast decoding algorithm. For short and medium length codes, many nodes fall into this range due to insufficient polarization. We hope to further reduce latency by introducing more fast-decodable patterns to cover more code rates.
- 2) Degree of parallelism: it can be represented by M, since the M bits in a simplified node are decoded in parallel.

 $<sup>^{1}\</sup>mathrm{A}$  leaf node  $v_{leaf}$  has no child node, and a root node  $v_{root}$  has no parent node.

The larger M is, a larger proportion of the binary tree can be pruned due to simplified decoding. we hope to increase M for higher throughput as well.

For M=8, the ratio of simplified nodes is 8/9, with only one code rate  $\frac{4}{8}$  unsupported, but the degree of parallelism is only 8. For M=16, the ratio of simplified nodes reduces to 8/17, leaving a wide gap of nine unsupported code rates  $\frac{4}{16},...,\frac{12}{16}$ , but the degree of parallelism doubles.

#### B. BCH node

To cover medium code rates, we need to find some patterns which can be fast decoded with good BLER performance. The bad news is, to the best of our knowledge, there exists no parallel decoding method for polar codes with code rates between  $\frac{3}{M}$  and  $\frac{M-3}{M}$ . The good news is that the outer codes represented by a subtree can be replaced by any codes, as shown in many previous works [10] [11] [12]. A good solution is removing the polar nodes with code rate falling into the gap, and grafting a different code that allows fast decoding.

BCH codes are good candidates due to their good minimum-distance property and fast hard-input decoding algorithms. If the error correcting capability is t, it is easy to design BCH codes whose minimum Hamming distance is larger than  $2 \times t$ . This leads to good BLER performance. Meanwhile, the Berlekamp-Massey (BM) algorithm can decode a BCH code with t=1 or t=2 within a few clock cycles. When grafted to polar codes as fast-decodable nodes, hard decisions are applied to the LLRs from the inner polar codes (parent nodes) before sending to the outer BCH codes (child nodes). Here the BCH codes are called "BCH nodes".

But BCH codes do not readily solve our problem. They only support a few code rates and code lengths, meaning they cannot cover all the codes rates within the gap. For the degree of parallelism M=16, the target code length is  $2^4$ , so the nearest code length of BCH is 15. Meanwhile, BCH codes only support code rates  $\frac{7}{15}$  and  $\frac{11}{15}$  within the gap and the corresponding number of information bits are k=7, k=11.

To overcome the issues, we first extend the code length to 16 bits. For the BCH codes with k=7 and t=2, the original codes can correct two error bits. We add an additional bit to be the parity check of all BCH code bits. The proposed two-step hard decoding works as follows. When the hard decision incurs three bit errors, and one of the errors has the minimum amplitude, the SPC bit can help correct one error bit first. Then the remaining two error bits can be corrected by the BM algorithm. But the same SPC extension no longer works for BCH codes with k=11 and t=1. The reason is as follows. If there are two or more bit errors in the node, the SPC function and BM algorithm both fail. Else if there is one error, the failure of SPC decoding will lead to more errors during BM decoding. Instead of SPC extension, we repeat one BCH code bit to improve its reliability.

Now that we have grafted two types of BCH nodes, the pattern-based decoding can support 10 code rates. The ratio of simplified nodes increases to 10/17, and the maximum gap reduces to  $\frac{4}{16}$ . Figure 3 shows the code rates supported by pattern-based decoding for degree of parallelism M=16.

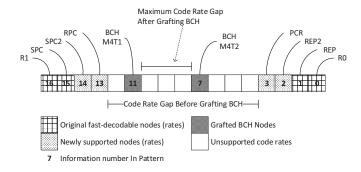


Fig. 2. Nodes (code rates) supporting fast decoding for degree of parallelism M = 16.

#### C. Fast polar codes via rate re-allocation

Even with the inclusion of BCH nodes, the fast decoding algorithm could not cover all the code rates of length-16 subtrees. As the second part of the solution, we propose to construct fast polar codes to avoid the "slow" nodes, and only use the existing ten patterns. Here "fast" resembles that of fast SC decoding but is achieved by altering the code construction instead of decoding. We show that it greatly reduces decoding latency and increases throughput with only slight performance loss

The following steps show how to construct fast polar codes only with node patterns of discontinuous code rates:

- Employ traditional methods such as Gaussian approximation (GA) or polarization weight (PW) to build polar codes with the parameter of code length N and code rate R.
- 2) Split all N synthesized sub-channels to N/16 segments. Each segment constitutes a 16-bit long block code, or equivalently a subtree with 16 leaf nodes.
- 3) Find out all "slow" segments which do not match the supported code rates or patterns. Re-allocate the code rates among segments to match the nearest supported code rate or pattern, which has K information bits.
- 4) If the number of information bits of the current segment exceeds or fall short of K, we remove or add a few information bits according to reliability. Apply this process to the remaining "slow" segments until all segments become fast-decodable.

The resulting code is coined as "fast polar code". A detailed description of the construction algorithm for fast polar codes can be found in Appendix A.

Take code length N=1024, code rate R=0.875 as an example, we count the number of fast-decodable nodes to be visited,  $f_{+/-}$ -functions [13] to be executed and edges to be traversed. These numbers provide a good estimate of SC decoding latency [3] [8], and are thus used to compare between the construction proposed in this section and the GA construction in Table I. As seen, the traversed nodes and edges reduce by 55% and 43.5%, respectively, while the  $f_{+/-}$ -function executions reduce only by 8.9%. Note that the former two parameters have a greater influence than  $f_{+/-}$ -functions because it cannot be parallelized in any form.

TABLE I Comparison of traversed nodes, edges and executed  $f_{+/-}$  Between GA construction and the proposed Fast Polar code Construction

		Distribution (	of fast	-decodable no	odes						
GA Construction				Fast Polar Code Construction							
Rate-1	4	SPC	20	Rate-1	2	SPC	9				
SPC-2	2	RPC	0	SPC-2	1	RPC	0				
PCR	1	REP-2	1	PCR	3	REP-2	1				
REP	11	Rate-0	1	REP	1	Rate-0	1				
BCH t=1	0	BCH t=2	0	BCH t=1	3	BCH t=2	2				
Count with respect to binary tree traversal											
	GA		Fast		Reduction(%)						
Nodes	40		22		55%						
$f_{+/-}$	4160		3792		8.9%						
edges	76		43		43.5%						

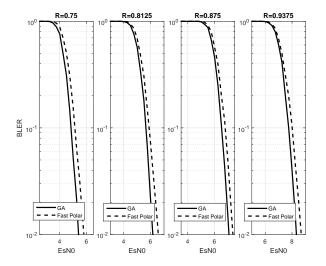


Fig. 3. BLER Performance comparison between GA and fast polar code construction.

It is worth noting that the proposed fast polar code construction algorithm reallocates the code rates of some nodes against their actual capacity derived from channel polarization. This inevitably incurs BLER performance loss. To evaluate the loss, we run simulations and Fig. 3 compares the BLER curves of both constructions under code length N=1024, and code rates  $R=\{0.75,0.8125,0.875,0.9375\}$ . There is a maximum of 0.3dB loss at BLER  $10^{-2}$  between GA polar codes and the fast polar codes when adopting QPSK modulation.

#### III. FAST DECODING ALGORITHMS

In this section, we describe the algorithms to support fast decoding of the newly defined SPC-2, REP-2, RPC and PCR nodes. For BCH nodes, we employ the classic BM algorithm which takes hard inputs and supports hardware-friendly fast decoding.

Each fast-decodable node v at stage s can be viewed as an outer code of length  $M=2^s$ . The code bits of v as an outer code are denoted by  $X_v$ , with M bits.

#### A. SPC-2

For a dual-SPC node v, we divide its code bits  $X_v$  into two groups,  $X_v^{even}$  whose indices are even numbers, and  $X_v^{odd}$  whose indices are odd numbers. According to the definition of an SPC-2 node, there are two parity-check bits in the subtree  $V_v$ , and the corresponding parity functions p[0] and p[1] can be written as

$$\begin{cases} p[0]: \bigoplus x = 0, x \in X_v \\ p[1]: \bigoplus x = 0, x \in X_v^{odd} \end{cases}$$

We add the two parity functions to get a parity function p[2]:

$$p[2] = p[0] \oplus p[1] : \bigoplus x = 0, x \in X_v^{even}$$

Since the two parity functions p[1] and p[2] involve two disjoint sets of code bits, the decoding of an SPC-2 node can be parallelized to two SPC nodes. Each SPC node inherits half of the elements from  $X_v$ . We can reuse two SPC decoding modules to fast decode an the SPC-2 node.

#### B. REP-2

For a dual-REP node v, we divide its code bits  $X_v$  into two groups,  $X_v^{even}$  whose indices are even numbers, and  $X_v^{odd}$  whose indices are odd numbers. According to the definition of an REP-2 node, there are two information bits in the subtree  $V_v$ . They are denoted by  $u_{M-2}$  and  $u_{M-1}$ .

It can be easily verified that  $X_v^{odd}$  are the repetition of  $u_{M-1}$  and  $X_v^{even}$  are the repetition of  $u_{M-2} \oplus u_{M-1}$ . Accordingly, we can divide a length-M dual-REP node into two M/2 REP nodes. We can reuse two REP decoding modules in parallel to fast decode a the REP-2 node.

#### C. RPC

For an RPC node v, we divide its code bits  $X_v$  into four groups as follows:

$$X_v^i = \{x \in X_v, mod(l(x), 4) = i\}, i \in \{0, 1, 2, 3\}$$
 (1)

According to the definition of an RPC node, there are three parity-check bits in the subtree  $V_v$ , and the parity functions p[0], p[1] and p[2] can be written as

$$\left\{\begin{array}{l} p[0]:\bigoplus x=0, x\in X_v^0\cup X_v^1\cup X_v^2\cup X_v^3\\ p[1]:\bigoplus x=0, x\in X_v^1\cup X_v^3\\ p[2]:\bigoplus x=0, x\in X_v^2\cup X_v^3 \end{array}\right.$$

We add the latter two parity functions to get parity function p[3]:

$$p[3] = p[1] \oplus p[2] : \bigoplus x = 0, x \in X_v^1 \cup X_v^2$$

And add this parity function to the first one to get parity function p[4]:

$$p[4]=p[0]\oplus p[3]:\bigoplus x=0, x\in X_v^0\cup X_v^3$$

We define  $\hat{c}_i = \bigoplus x, x \in X_v^i, i \in [0, 1, 2, 3]$ . According to parity functions p[1] to p[4], one can easily verify that the following relationship holds:

$$\hat{c}_1 \oplus \hat{c}_3 = \hat{c}_2 \oplus \hat{c}_3 = \hat{c}_1 \oplus \hat{c}_2 = \hat{c}_0 \oplus \hat{c}_3 = 0 \tag{2}$$

Equation (2) implies the existence of a virtual repetition code of rate  $\frac{1}{4}$ , because:

$$\hat{c}_0 = \hat{c}_1 = \hat{c}_2 = \hat{c}_3 = 0$$
$$\hat{c}_0 = \hat{c}_1 = \hat{c}_2 = \hat{c}_3 = 1$$

where  $\hat{c}_0, \hat{c}_1, \hat{c}_2, \hat{c}_3$ , are the virtual repeated code bits.

Given the above knowledge, the decoding algorithm for an RPC node at stage s where  $s \leq 2$ , can be easily derived as Algorithm 1, in which  $sig(\alpha) \triangleq \left\{ \begin{array}{l} 0, \alpha \geq 0 \\ 1, \alpha < 0 \end{array} \right.$ .

### Algorithm 1 Decoding a repeated parity check (RPC) node.

#### Input:

or

The received signal  $\alpha_v = \{\alpha_{v_k}, k = 0 \cdots M - 1\}$ ; Output:

```
The codeword to be recovered: \hat{\mathbf{x}} = \{\hat{x_k}, k = 0 \cdots M - 1\};
 1: Initialize: \Delta_0 = 0, \Delta_1 = 0
 2: Initialize: \delta_i = \infty, c_i = 0, p_i = 0 for i = 0 \cdots 3;
 3: Initialize: \hat{x_k} = sig(\alpha_{v_k}) for k = 0 \cdots M - 1;
 4: for i = 0 \cdots 3 do
         for j = 0 \cdots M/4 do
 5:
            k = i \times 4 + i;
 6:
            c_i = c_i \oplus sig(\alpha_{v_k});
 7:
            if |\alpha_{v_k}| < \delta_i
 8:
               p_i = k;
 9:
                \delta_i = |\alpha_{v_k}|;
10:
         end for
11:
         if c_i = 1
12:
            \Delta_0 = \Delta_0 + \delta_i
13:
14:
            \Delta_1 = \Delta_1 + \delta_i
15:
16: end for
17: for i = 0 \cdots 3 do
         if((\Delta_0 > \Delta_1) \cap (c_i = 0)) \cup ((\Delta_0 < \Delta_1) \cap (c_i = 1))
18:
            \hat{x}_{p_i} = \sim \hat{x}_{p_i}
19:
20: end for
```

#### D. PCR

For a PCR node v, we divide its code bits  $X_v$  into four groups in the same way as in (1). According to the definition of an RPC node, there are three information bits in this node. They are denoted by  $u_{M-3}$ ,  $u_{M-2}$  and  $u_{M-1}$ .

We define  $c_i, i \in \{0, 1, 2, 3\}$  according to the following equation

$$[c_0 \ c_1 \ c_2 \ c_3] = [0 \ u_{M-3} \ u_{M-2} \ u_{M-1}] \times G_4$$
 (3)

It can be easily verified that  $X_v^0$  are the repetition of  $c_0$ ,  $X_v^1$  are the repetition of  $c_1$ ,  $X_v^2$  are the repetition of  $c_2$ , and  $X_v^3$  are the repetition of  $c_3$ . Thus, we divide the input signal  $\alpha_v$  into four groups according the indices and combine the input signals within each group into four enhanced signals  $\Delta_i$ ,  $i \in \{0, 1, 2, 3\}$ , as in an REP node.

Equation (3) implies the existence of a virtual single parity check code of rate  $\frac{3}{4}$ , with virtual code bits  $c_i$ ,  $i \in \{0, 1, 2, 3\}$ , so we can reuse SPC module to decode it. A detailed description of PCR decoding is given in Algorithm 2.

**Algorithm 2** Decoding a parity checked repetition (PCR) node.

```
Input:
     The received signal \alpha_v = \{\alpha_{v_k}, k = 0 \cdots N - 1\};
Output:
     The codeword to be recovered: \hat{\mathbf{x}} = \{\hat{x_k}, k = 0 \cdots N - 1\};
 1: Initialize: \Delta_i = 0 for i = 0 \cdots 3;
 2: for i = 0 \cdots 3 do
        for j = 0 \cdots N/4 do
 3:
            k = j \times 4 + i
            \Delta_i = \Delta_i + \alpha_{v_k}
 5:
        end for
 7: end for
 8: \{\hat{c_0}, \hat{c_1}, \hat{c_2}, \hat{c_3}\} = SPC\_DEC(\{\Delta_0, \Delta_1, \Delta_2, \Delta_3\})
 9: for i = 0 \cdots 3 do
        for j = 0 \cdots N/4 do
10:
            k = j \times 4 + i
11:
12:
            \hat{x_k} = \hat{c_i}
        end for
13:
14: end for
```

#### IV. HARDWARE IMPLEMENTATION

We designed two types of hardware architectures to verify the performance, area efficiency and energy efficiency.

- Recursive Decoder: It supports flexible code length and coding rates of mother code length N from 32 to 1024 with the power of 2. With rate matching, flexible code length with  $0 < N \le 1024$  and code rate with  $0 < R \le 1$  are supported. The  $f_{+/-}$  functions in nodes are processed by single PE (processing element) logic, and one decision module to support all 9 patterns<sup>2</sup>. The decoder processes one packet at a time.
- Unrolled Decoder: It only supports a fixed code length and code rate. In our architecture we hard coded code length N = 1024, and code rate R = 0.875. This fully unrolled pipelined design combines exclusive dedicated PEs to process each f<sub>+/-</sub> function in the binary tree. Same to the decision modules that 21 dedicated node specific logic are implemented to support 21 nodes patterns. With 25 packets simultaneously decoding, thanks to the unrolled fully utilization of processing logic and storage, this decoder provides extreme high throughput with high area efficiency and low decoding energy.

Both the above mentioned decoder implementations adopt successive cancellation algorithm accelerated by pattern-based fast decoding. The maximum degrees of parallelization are 128 for SPC and SPC-2 nodes, and 256 for R1 nodes. All other nodes enjoy a degree of parallelism of 16.

#### A. Parallel Comparison Circuit

We observe that there are several large SPC nodes in the right half of the binary tree. As described, these SPC nodes need to be processed with a higher degree of parallelism to achieve a higher throughput. The SPC decoding algorithm is

<sup>&</sup>lt;sup>2</sup>R0 node is bypassed in SC decoding.

very simple as follows. First, get the signs of an SPC node's input signals, find the minimum amplitude of input signals and record its position. Then, do a parity check of the signs. If it passes, then return these signs, else reverse the sign of recorded minimum-amplitude position and return the updated

To process a large SPC node, a circuit is required to locate a minimum amplitude from a large amount of input signals. The traditional pairwise comparison method requires a circuit of depth  $log_2(M)$ , where M is the number of amplitudes to be compared. Finding the smallest among eg., 128 amplitudes takes 7 steps comparison, considering clock frequency is at 1Ghz, it is very challenging to meet timing constraints completing all comparisons in one clock cycle.

We advocate a parallel comparison architecture to replace the traditional one. For a node v at stage s, its input signals  $\alpha_v$  include  $M=2^s$  elements, the amplitudes of which are denoted as  $[A_0 \ A_1 \ \cdots \ A_{M-1}]$ . Each amplitude has x-bit quantization. We fill the x-bit quantized binary vectors into the columns of a matrix as follows:

$$[A_0 \cdots A_i \cdots A_{M-1}] = \begin{bmatrix} b_0^0 & \cdots & b_i^0 & \cdots & b_{M-1}^0 \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ b_0^j & \cdots & b_i^j & \cdots & b_{M-1}^j \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ b_0^{r-1} & \cdots & b_i^{r-1} & \cdots & b_{M-1}^{r-1} \end{bmatrix}$$

Rewrite the matrix with respect to its row vectors matrix and we have  $[B_0 \cdots B_j \cdots B_{x-1}]^T$ , in which  $B_j =$  $\begin{bmatrix} b_0^j & \cdots & b_i^j & \cdots & b_{M-1}^j \end{bmatrix}, j \in \{0, 1 \cdots x - 1\}$  is a row vector.  $B_j$  can be represented as an M-bit variable. We propose Algorithm 3 to find out the minimum-amplitude position through a reverse mask D, in which the bit "1" indicates the minimum.

#### **Algorithm 3** Parallel Comparison Algorithm.

The received signal  $\alpha_v = \{\alpha_{v_k}, k = 0 \cdots M - 1\};$ **Output:** 

The Reverse Mask: D is an M-bit Variable;

- 1: Initialize:  $[B_0 \cdots B_i \cdots B_{x-1}]^\mathsf{T}$  from  $\alpha_v$ ;
- 2: Initialize: An N-bits variable  $C = \mathbf{0}$ , .
- 3: **for**  $j = x 1 \cdots 0$  **do**
- M-bit Variable  $E = (C|B_i)$
- if(Not all bits in E are "1") 5:
- C = E
- 7: end for
- 8: Reverse Mask  $D = \sim C$

The parallel comparison algorithm reduces the comparison logic depth from  $log_2(M)$  to 1. But the reverse mask D may have two or more minimum positions. That means the input signals  $\alpha_v$  include two or more minimum amplitudes. It must generate an error if there are two minimum amplitudes. To avoid this error occur, we can apply an additional circuit to ensure the uniqueness of the selected minimum position.

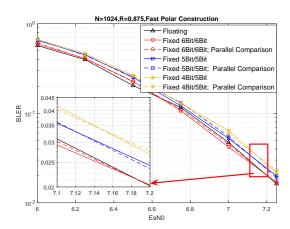


Fig. 4. Performance comparison between Floating Point and Fixed Point.

#### B. Bit quantization

An attractive property of polar codes is that SC decoding works well under low-precision quantization (4 bits to 6 bits). Lower precision quantization is the key to higher throughput, as it effectively reduces implementation area and increases clock frequency.

There are two types of quantization numbers, one is for channel LLR and the other is for internal LLR. We first test the case with 6-bit input quantization and 6-bit internal quantization. According to Fig 4, this setting achieves the same performance as floating-point. The second one is 5-bit quantization/5-bit internal quantization. It incurs < 0.1dB loss. Finally, 4-bit input quantization/5-bit internal quantization incurs < 0.2dB loss. In this paper, we evaluate the physical implementation result under 5-bit quantization both input and internal signals to strike a good balance between complexity and throughput.

At the same time, we also compare the BLER performance between the original SPC and parallelized SPC. None of the quantization schemes yields harmful loss.

#### C. Layout View

We carry out the two physical implementations for both the recursive and unrolled architecture.

With TSMC 16nm technology, the recursive decoder synthesis area is  $0.032mm^2$ , the clock frequency is 1.00Ghz. The decoder's layout size is  $192\mu m \times 234\mu m = 0.045mm^2$ . With the same ASIC technology node, the unrolled decoder synthesis area is  $0.17mm^2$ , the clock frequency is 1.20Ghz. The decoder's layout size is  $500\mu m \times 600\mu m = 0.3mm^2$ . Figure 5 shows the two layout graphs of the decoders. Note that the area of the unrolled decoder is actually much larger than the recursive decoder.

#### V. KEY PERFORMANCE INDICATORS

The key performance indicators (KPIs) are reported in this section. First of all, we evaluate the area efficiency using equation  $AreaEff(Gbps/mm^2) = \frac{InfoSize(bits)}{Latency(ns) \times Area(mm^2)}$ . The recursive decoder takes 40 clock cycles to decoder one

packet under fast polar code construction with code length

Implementation	This Work (Unroll)	This Work (Recursive)	[5]	[16]	[7]				
Construction	Fast-Polar	Fast-Polar	Polar	Product-Polar	Polar				
Decoding Algorithm	Fast-SC	Fast-SC	SC	PDF-SC	OPSC				
Code Length	1024	1024	32768	16384	1024				
Code Rate	0.875	0.875	0.864	0.864	0.83				
Technology	All in TSMC 16nm								
Clock Frequency $(Ghz)$	1.20	1.00	1.00	1.05	1.20				
Throughtput/Coded-bit (Gbps)	1229	25.6	5.27	139.7	1229				
Throughtput/Info-bit (Gbps)	1075	22.4	4.56	120.73	1020				
Area/Layout $(mm^2)$	0.30	0.045	0.35	1.00	0.79				
Area Eff/Coded-bit( $Gbps/mm^2$ )	4096	561	15.1	139.7	1555				
Power(mW)	784	30.9	-	94	1167				
Energy $(pJ/bit)$	0.63	1.21	-	0.67	0.95				

TABLE II COMPARISON WITH HIGH THROUGHPUT POLAR DECODER

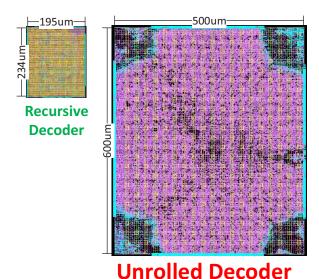


Fig. 5. Layout Graph of Recursive and Unrolled Decoder under the same scale.

N=1024, and code rate R=0.875. Thus the throughput is  $(1024\ bits \times 1\ Ghz)/40\ cycles = 25.6Gbps$  for coded bits, and  $((1024\times 0.875)\ bits \times 1\ Ghz)/40\ cycles = 22.4Gbps$  for information bits. With TSMC 16nm process, the area efficiency for coded bits is  $561Gbps/mm^2$ .

The unrolled decoder takes 25 clock cycles to decoder one packet. It is fully pipelined, meaning a new packet of decoded results would be generated continuously every cycle after the first 25 clock cycles of the first packet processing time. The throughput is thus  $1024\ bits \times 1.2\ Ghz = 1229Gbps$  for coded bits, and  $(1024\times0.875)\ bits\times1\ Ghz = 1075Gbps$  for information bits. With TSMC 16nm process, the area efficiency for coded bits is  $4096Gbps/mm^2$ .

We further evaluate the power consumption and decoding energy per bit through a simulation in which 200 packets are decoded. The process, voltage and temperature (PVT) condition of evaluation is TT corner, 0.8V and  $20^{\circ}C$ , and the resulting of recursive decoder's power consumption is 30.9mW, and decoding each bit costs 1.21pJ of energy on average; while the unrolled decoder's power consumption is 784mW, and decoding each bit costs 0.63pJ of energy on

average.

We also compare the decoding throughput, area efficiency and power consumption with several high-throughput decoders in literature, and present the results in Table II. From the KPIs, we conclude that unrolled decoders are more suitable for scenarios requiring extremely high throughput but only support fixed code length and rate; recursive decoders are much smaller, which are better for resource constrained devices, and at the same time provides flexible code rates and lengths - a desirable property for wireless communications.

#### VI. CONCLUSIONS

In this paper, we propose a new construction of fast polar codes, which is solely composed of fast-decodable special nodes at length 16. By viewing the decoding process as a binary tree traversal, the fast polar codes can reduce 55% of node visits, 8.9% of  $f_{+/-}$  calculation and 43.5% of edge traversal over the original polar construction at code length N=1024, and code rate R=0.875, at the cost of slight BLER performance loss.

We implement two types of decoders for the fast polar codes. The recursive decoder can support flexible code lengths and code rates, and support code length up to 1024. This decoder layout area is only  $0.045mm^2$ , and can provide 25.6Gbps coded bits throughput, with an area efficiency of  $561Gbps/mm^2$ .

The unrolled decoder only supports one code length N=1024 and one code rate R=0.875. However, the fully pipelined structure leads to hardware with ultra-high area efficiency and low decoding power consumption. This decoder layout area is  $0.3mm^2$ , and can provide 1229Gbps code bit throughput, with an area efficiency as high as  $4096Gbps/mm^2$ .

These results indicate that fast polar codes can meet the high-throughput demand in the next-generation wireless communication systems. And the recursive hardware design and unrolled hardware design can be adopted to satisfy different system requirements.

#### APPENDIX

A. Fast Polar Code Construction Algorithm

#### **Algorithm 4** A method to construct fast polar codes.

#### Input:

Code length N, information length K, the set of fast-decodable modes  $\Theta$ .

#### **Output:**

Re-allocate node-wise code rates such that all nodes support fast decoding.

- Construct an (N, K) polar code based on GA or PW methods.
- 2: Divide the code into segments of length 16 and the number of segments is denoted by  $N_{\rm s}$ .
- 3: Progressively refine the code construction as follows. All the frozen bit positions are intialized as active states and "active" bit position can be transformed to an informtaion bit position in the refining process.
- 4: for  $t = 1 \cdots N_s$  do
- 5: **while** the t-th segment does not belong to  $\Theta$  **do**
- 6: Denote by *i* the least reliable information bit position in the *t*-th segment.
- 7: Denote by j the most reliable frozen bit position of active states in the subsequent segments, and denote by  $k_j$  the number of information bits in that segment.
- 8: **if**  $k_j \ge 11$  and  $k_j < 16$  or  $k_j < 3$  **then** 
  - Mark i as a frozen bit position and j as an information bit position.
- 10: **els**

9:

- 11: Mark j as inactive state.
- 12: end if
- 13: end while
- 14: end for

#### REFERENCES

- W. Saad, M. Bennis, and M. Chen, "A vision of 6G wireless systems: applications, trends, technologies, and open research problems," *IEEE Network*, 2019.
- [2] E. Arıkan, "Channel polarization: a method for constructing capacity-achieving codes for symmetric binary-input memoryless channels," *IEEE Transactions on Information Theory*, vol. 55, no. 7, pp. 3051-3073, Jul. 2000
- [3] A. Alamdar-Yazdi and F. Kschischang, "A simplified successive-cancellation decoder for polar codes," *IEEE Communications Letters*, vol. 15, no. 12, pp. 1378-1380, Dec. 2011.
- [4] O. Dizdar and E. Arıkan, "A high-throughput energy-efficient implementation of successive cancellation decoder for polar codes using combinational logic," *IEEE Transactions on Circuits and Systems I*, vol. 63, no. 3, pp. 436-447, Mar. 2016.
- [5] X. Liu, Q. Zhang, P. Qiu, J. Tong, H. Zhang, C. Zhao, J. Wang, "A 5.16Gbps decoder ASIC for polar code in 16nm FinFET," in *International Symposium on Wireless Communication Systems (ISWCS)*, Lisbon, 2018, pp. 1-5.
- [6] A. Sral, E. G. Sezer, Y. Ertugrul, O. Arıkan and E. Arıkan, "Terabits-persecond throughput for polar Codes," in *IEEE International Symposium* on Personal, Indoor and Mobile Radio Communications (PIMRC Workshops), 2019, pp. 1-7.
- [7] A. Śral, E. G. Śezer, E. Kolagasioglu, V. Derudder, K. Bertrand, "Tb/s polar successive cancellation decoder 16nm ASIC implementation," Available on http://www.polaran.com/documents/EPIC\_Polar\_Code\_Paper.pdf.
- [8] S. A. Hashemi, C. Condo, and W. J. Gross, "Fast and flexible successive-cancellation list decoders for polar codes," *IEEE Transactions on Signal Processing*, vol. 65, no. 21, pp. 5756–5769, Nov. 2017.
- [9] G. Sarkis, P. Giard, A. Vardy, C. Thibeault and W. J. Gross, "Fast polar decoders: algorithm and implementation," *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 5, pp. 946-957, May 2014.

- [10] Y. Wang, K. Narayanan, "Concatenations of polar codes with outer BCH codes and convolutional codes," in *Annual Allerton Conference on Communication Control and Computing (Allerton)*, pp. 813-819, 2014.
- [11] H. Saber, I. Marsland, "Design of generalized concatenated codes based on polar codes with very short outer codes," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 4, pp. 3103-3115, 2017.
- [12] D. Goldin, D. Burshtein, "Performance bounds of concatenated polar coding schemes", *IEEE Transactions on Information Theory*, vol. 65, no. 11, pp. 7131-7148, 2019.
- [13] A. Balatsoukas-Stimming, M. B. Parizi and A. Burg, "LLR-based successive cancellation list decoding of polar codes," *IEEE Transactions* on Signal Processing, vol. 63, no. 19, pp. 5165-5179, Oct. 2015.
- [14] X. Wang, H. Zhang, R. Li, J. Tong, Y. Ge, and J. Wang, "On the construction of  $G_N$ -coset codes for parallel decoding," in *IEEE Wireless Communications and Networking Conference (WCNC)*, Seoul, Korea (South), 2020, pp. 1-6.
- [15] X. Wang, J. Tong, H. Zhang, S. Dai, R. Li, and J. Wang, "Toward terabits-per-second communications: low-complexity parallel decoding of G<sub>N</sub>-coset codes," in *IEEE Wireless Communications and Networking* Conference (WCNC), 2021, pp. 1-5.
- [16] J. Tong, X. Wang, Q. Zhang, H. Zhang, S. Dai, R. Li, and J. Wang, "Toward terabits-per-second communications: a high-throughput implementation of G<sub>N</sub>-coset codes," in *IEEE Wireless Communications and Networking Conference (WCNC)*, 2021, pp. 1-6.