# Quantum circuit optimization for multiple QPUs using local structure

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Abstract—Interconnecting clusters of qubits will be an essential element of scaling up future quantum computers. Operations between quantum processing units (QPUs) are usually significantly slower and costlier than those within a single QPU, so usage of the interconnect must be carefully managed. This is loosely analogous to the need to manage shared caches or memory in classical multi-CPU machines. Unlike classical clusters, however, quantum data is subject to the no-cloning theorem, which necessitates a rethinking of cache coherency strategies. Here, we consider simple strategies of using EPRmediated remote gates and teleporting qubits between clusters as necessary – generally expensive operations that we seek to minimize. Crucially, we develop optimizations at compile-time that leverage local structure in a quantum circuit, so as to minimize inter-cluster operations at runtime. We benchmark our approach against existing quantum compilation and optimization routines, and find significant improvements in circuit depth and interconnect usage.

#### I. INTRODUCTION

Quantum information processing (QIP) hardware have undergone rapid advances in both quality and quantity in recent years [1]–[3]. Nevertheless, most useful algorithms and routines that might be executed on a quantum computer continue to require resources that surpass the scale of current-generation quantum processing units (QPUs). The resource shortfall can be sheer number of qubits on a QPU (i.e. "width"), number of quantum operations being performed before noise and errors accrued become overwhelming (i.e. "depth"), or both. These resource shortfalls are potentially further exacerbated if errorcorrection schemes are employed.

Simply adding more qubits to a QPU is an obvious way to overcome width limitations. Yet in practice, we are prevented by technical obstacles from doing so indefinitely. In most QPU architectures, there are known limits beyond which, naively scaling up qubit-count yields diminishing returns. For instance, in trapped-ion QPUs adding more ions into a trap either increases the complexity or the duration of two-qubit gate operations, and necessitates cooling cycles that undo heating inadvertently introduced in the course of computation and read-out. In another example, solid-state QPUs (e.g. superconducting transmon qubits) grow in surface area with respect to the number of qubits it contains, inevitably running up against high substrate and manufacturing defect rates.

One avenue for increasing qubit count beyond the size limits inherent to many single-QPU systems is simply to interconnect multiple QPUs of bounded size. In classical computing, this is somewhat analogous to interconnecting "chiplets" – usually classical processing units (CPUs) residing on monolithic silicon dies – into a system-on-chip (SoC), or linking up fully functional computers with fast network interfaces. In either case, one ends up with a device with greater combined execution resources.

A crucial distinction when adopting a multi-QPU paradigm in quantum computing is that communication between QPUs must be mediated by quantum channels rather than classical ones. In some implementations, that quantum channel is realised simply by *moving* a physical qubit from one QPU to another. However, quantum mechanics also allows for a preshared "mediator" or "resource" state (usually some highly entangled quantum state). This state is distributed between QPUs and, when it is used alongside *classical* communication and teleportation-like mechanisms, can act as a quantum channel. Leveraging this fact, some multi-QPU schemes eschew physical transport of qubits between QPUs in favour of mechanisms for generating and distributing these resource states.

Properly considering and optimizing for the behaviour of these quantum channels requires careful compiler design. One aspect of the optimization is to ensure, as much as possible, that related data (e.g. those that must be operated on together) remain on the same QPU. This minimizes operations that straddle multiple QPUs, which are often slower and costlier than those that are resident on a single QPU.

#### II. BACKGROUND

## A. Flavours of quantum interconnect

One method for interconnecting multiple QPUs is to transport a qubit physically. This process is generally slow and inefficient. We refer interested readers to [4] for one example where trapped-ions are shuttled between traps in quantum charge-coupled devices (QCCD), and to [5], [6] for discussions on converting a microwave photon, which couples to a solid-state superconducting QPU, into an optical one that can be transported via fiber. With QCCDs, shuttling operations are 6 - 15 times slower than operations "native" to a single QPU. Microwave-to-optical transducers on the other hand are lossy and currently are limited to single-digit efficiencies.

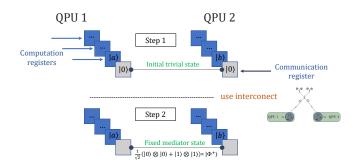


Figure 1. Illustration of an interconnect being used to generate a resource state between two separate quantum processing units (QPUs). In this example each QPU contains a number of data qubits (blue) and one interconnect qubit (gray). The interconnect (right hand figure) collects a single photon from each interconnect qubit and interferes it in order to entangle the two interconnect qubits. The resulting entangled state can be used as a resource to enable quantum communication.

For compilation purposes therefore, these transport operations represent a bottleneck to be minimized.

An alternative to physical transport is to leverage entangled resource states and classical communication [7]. Figure 1 shows an example of two QPUs linked by an interconnect, whose function is simply to generate an entangled resource state. That resource state can be used to mediate interactions across the two QPUs using only *local operations and classical communication* (LOCC). We will briefly describe how this works. Consider the so-called  $\Phi^+$  Bell- or Einstein-Podolsky-Rosen (EPR) state:

$$\left|\Phi^{+}\right\rangle = \frac{1}{\sqrt{2}} \sum_{k \in \{0,1\}} \left|k\right\rangle_{1} \left|k\right\rangle_{2} \tag{1}$$

The subscript in each ket in the summand indicates that the ket addresses states in QPU 1 (or 2) respectively. Now suppose one is interested in performing a coherent XOR (also known as a controlled- $\sigma_X$  or "CNOT") operation, defined as:

$$XOR_{a,b} : |a\rangle |b\rangle \mapsto |a\rangle |a \oplus b\rangle \tag{2}$$

where  $\oplus$  denotes addition modulo 2. Supposing the states  $|a\rangle$  and  $|b\rangle$  reside on QPUs 1 and 2 respectively, the desired XOR operation stipulated here can be mediated by that  $|\Phi^+\rangle$  resource state as follows. Start with the initial state:

$$\begin{split} |\psi\rangle &= |a\rangle_1 \left|\Phi^+\right\rangle |b\rangle_2 \\ &= |a\rangle_1 \otimes \left[\frac{1}{\sqrt{2}} \sum_{k \in \{0,1\}} |k\rangle_1 \left|k\right\rangle_2\right] \otimes |b\rangle_2 \qquad (3) \end{split}$$

Do an XOR between  $|a\rangle_1$  and 2nd register (half of  $\Phi^+$  that resides on QPU 1); as well as between the 3rd register (half of  $\Phi^+$  that resides on QPU 2) and  $|b\rangle_2$ :

$$\begin{aligned} \text{XOR} : |\psi\rangle \\ \mapsto |a\rangle_1 \otimes \left[\frac{1}{\sqrt{2}} \sum_{k \in \{0,1\}} |k \oplus a\rangle_1 |k\rangle_2\right] \otimes |b \oplus k\rangle_2 \quad (4) \end{aligned}$$

Now suppose we measure the 2nd register and find the *classical* bit  $k \oplus a = m$ , which implies  $k = a \oplus m$ . The rules of quantum measurements implies that the quantum state immediately collapses to:

$$|a\rangle_{1} \otimes [|k \oplus a\rangle_{1} |k\rangle_{2}] \otimes |b \oplus k\rangle_{2}$$
$$= |a\rangle_{1} \otimes [|m\rangle_{1} |a \oplus m\rangle_{2}] \otimes |b \oplus a \oplus m\rangle_{2}$$
(5)

If QPU 1 can *classically* communicate the bit m with QPU 2, then the latter can perform a bit-flip conditioned upon that bit, which yields:

$$|a\rangle_1 \otimes [|m\rangle_1 | a \oplus m\rangle_2] \otimes \sigma_X^m | b \oplus a \oplus m\rangle_2 \tag{6}$$

$$= |a\rangle_1 \otimes [|m\rangle_1 | a \oplus m\rangle_2] \otimes |b \oplus a\rangle_2 \tag{7}$$

Finally, we can apply a Hadamard operator to the 3rd register and measure it (obtaining a classical bit n) to disentangle remnants of the EPR-state, leaving us with:

$$(-1)^{(a\oplus m)n} |a\rangle_1 \otimes |b\oplus a\rangle_2 \tag{8}$$

The stray phase here can be corrected by applying  $\sigma_Z^n$ , which QPU 1 can do if the bit *n* is communicated by QPU 2. Note, the result is the desired output of the original XOR operation defined in 2. We had effected this XOR between qubits on separate QPUs by consuming an EPR state and exchanging only one pair of classical bits between QPUs 1 and 2.

A host of other constructions that use EPR resource states to yield common operations (e.g. bit-swap, Tofolli, etc.) can similarly be derived. Particularly noteworthy is basic teleportation [8], which most closely mimics simply moving a qubit like physical transport would.

Ultimately, key to being able to perform any EPR-mediated operations between QPUs is the ability to produce and distribute the resource states to begin with. To that end, optical schemes had been demonstrated that can generate EPR-states between trapped ions at up to  $\sim 200$  Hz [9]–[11]. This is faster than some QCCD shuttling operations, but is still very slow compared to native single-QPU operations [12].

#### B. Quantum compilation

The essential remit of a compiler is to reconstruct a program to be better suited for execution on hardware, while preserving its functionality. In the context of quantum computing, programs are often specified as quantum circuits constructed from basic gates. The quantum compiler must ensure that all gates specified within the quantum circuit are supported in hardware. For single-qubit gates, this is a matter of finding decompositions of a unitary matrix in U(2) in a hardwarecompatible basis.

Gates involving more qubits (like the XOR discussed in Section II-A) incur an additional complication: Many QPUs do *not* support two-qubit operations between arbitrary qubit pairs. This is usually conveyed succinctly as a "coupling map", an undirected graph  $G_{cmap}$  where vertices represent qubits and edges represent supported two-qubit operations. If a desired gate (say a U(4) operation) addresses a pair of qubits that are not directly coupled in hardware (i.e. vertices in  $G_{cmap}$  not connected by an edge), a simple basis change is insufficient. Instead, a common tack is to find an indirect route between relevant vertices in  $G_{\rm cmap}$ , and then re-synthesize the desired gate in terms of supported operations along that route. If  $G_{\rm cmap}$  is disjoint, that is some vertices are simply unreachable from some others, then certain two-qubit (or multi-qubit) operations are simply impossible on that hardware.

This process of resolving two-qubit gates onto a given hardware topology can result in many additional operations being introduced ( $\mathcal{O}(4d)$  for remote operations,  $\mathcal{O}(3d)$  for a swap-based approach without reverse swap; here d is length of the indirect route between qubits targeted by the two-qubit operation). The resulting hardware-mapped circuit therefore can have significantly increased depth [13]. Much work had been devoted to finding hardware-efficient two-qubit gate resynthesis, given a circuit [14]–[16]. Slightly less obvious is the fact that the number of additional gates introduced during re-synthesis can vary wildly depending on how qubits in a quantum circuit (i.e. "logical" qubits) are assigned to particular vertices in  $G_{\text{cmap}}$  (i.e. "physical" qubits). There is every chance that a naive assignment (e.g. simply assigning logical qubit  $0 \rightarrow$  physical qubit 0,  $1 \rightarrow 1$ ,  $2 \rightarrow 2$ , and so on) will be sub-optimal. An important aspect of quantum compilation therefore includes the construction of a logical to physical qubit map that yields an efficient circuit.

Unfortunately, finding an optimal assignment is potentially a hard classical problem. The space of possible logical  $\rightarrow$ physical qubit maps is N!/(N - M)!, where N(M) is the total number of physical (logical) qubits, which rules out a brute-force search for large circuits or QPUs. More formally, suppose we construct a coupling map analogous to  $G_{\text{cmap}}$ but specified *not* by hardware topology but rather from twoqubit gate density in a quantum circuit; call this graph  $G_{\text{circ}}$ . Then, finding the optimal assignment in some cases reduces to finding a graph isomorphism between  $G_{\text{circ}}$  and subgraphs of  $G_{\text{cmap}}$ . This is generally NP-complete and not tractable when N and M are large and neither graph is very sparse or disjoint [17], [18]. In the rest of the manuscript, we will describe "gentler" graph problems relevant to our compilation approach.

## **III. COMPILATION TECHNIQUE**

# A. Choice of Topology

While the qubit assignment problem (mapping logical  $\rightarrow$  physical qubits) generally construed in Section II-B is not tractable, particular instances of the problem *may* be satisfactorily solved in practice [17], [18]. For our purposes in this manuscript however, we will avoid the isomorphism problem entirely by focusing only on hardware topologies that are "well clustered". These are characterised by graphs that admit clusters of qubits that possess denser intra-cluster couplings and comparatively fewer inter-cluster ones.

Given the context of multi-QPU architectures that we are considering, this sort of hardware topology is natural. In Section II we described various realisations of inter-QPU operations, all of which are bottlenecked in rate and cost given currently available hardware. The assumption, that interconnects will remain a scarce resource within multi-QPU architectures, is likely a reasonable one for the foreseeable future. An extreme example is embodied in monolithic ion-trap devices in which native intra-QPU couplings are fundamentally all-to-all (so that  $G_{cmap}$  generally has  $\mathcal{O}(N^2)$  edges), while inter-QPU couplings either through distributed EPR-pairs or shuttled ions will likely remain sparse (possibly  $\mathcal{O}(N)$ ) due to rate limits and cost of multiplexing many simultaneous Hong-Ou-Mandel interactions [10]. In limiting our focus to "well-clustered" hardware topologies, the central thesis is that it becomes far more important optimize for the expensive or scarce resource (i.e. usage of inter-QPU couplings), rather than any and all couplings more generally.

To be more precise, how "well-clustered" a given coupling map is can be evaluated using several measures, one being the graph *conductance*  $\phi_G$ . Supposing one attempts to partition the graph  $G_{\text{cmap}}$  into k disjoint clusters corresponding to separate QPUs, then for  $1 \leq j \leq k$ , conductance is defined as:

$$\phi_G(j) = \min_{\vec{v}} \frac{\vec{v}_j^T (D - A) \vec{v}_j}{\vec{v}_j^T D \vec{v}_j},\tag{9}$$

for our purposes, A is the adjacency matrix which i, j-th entry is 1 if the *i*-th and *j*-th vertices are joined by an edge; D is a degree matrix s.t.  $D_{ij} = \delta_{ij} \sum_k A_{jk}$ ; and  $\vec{v}_j$  is an indicator vector whose k-th entry is 1 if the k-th vertex belong in the *j*-th cluster and is 0 otherwise. A well-clustered graph admits a partitioning s.t.  $\phi_G(j)$  is low for all *j*. As a means for quickly evaluating whether a hardware topology is wellsuited for our compilation approach,  $\phi_G$  is convenient since it is known to be upper-bounded by the k-th eigenvalue of the Laplacian  $\mathcal{L} = D - A$  through an extension to Cheeger's inequality [19]. The eigenvalues of  $\mathcal{L}$ , in turn, can be computed directly without first having to *find* the partitions that specify  $\vec{v}$ . Another important measure for our purposes is the association ratio:

$$R_G(j) = \frac{\vec{v}_j^T A \vec{v}_j}{\vec{v}^T \vec{v}} \tag{10}$$

We consider our methods to be applicable for hardware topologies that exhibit small  $\phi_G$ , and *especially applicable* where  $\phi_G$  decreases with increasing qubit count N and roughly static  $R_G$ .

## B. Global QPU assignment

One consequence of choosing to optimize inter-QPU operations, is that we are now concerned mainly with the problem of assigning logical qubits to QPUs rather than to physical qubits. Suppose, from an input quantum circuit, we construct a coupling graph ( $G_{circ}$ ) s.t. its adjacency matrix entry  $A_{ij}$  is simply the number of 2-qubit gates between qubits *i* and *j*. Without loss of generality assume that there are no multi-qubit gates beyond two-qubit ones<sup>1</sup>. Then, minimizing the number

<sup>&</sup>lt;sup>1</sup>If an input circuit were to contain multi-qubit gates, universality results ensure that we can always efficiently decompose them into more elementary blocks consisting of single- and two-qubit gates at most [20], [21]

of inter-QPU operations in a k-QPU architecture is equivalent to minimizing the cost function:

$$C_{\rm KL} = \sum_{j=1}^{k} \vec{v}_j^T \mathcal{L}_{\rm circ} \vec{v}_j, \qquad (11)$$

where  $\mathcal{L}$  is the Laplacian matrix for  $G_{\text{circ}}$  as defined in Section III-A, and the indicator vector  $\vec{v}_j$  takes value 1 in its *r*-th entry if the *r*-th logical qubit is assigned to QPU-*j*, and 0 otherwise. Finding  $\vec{v}_j$ 's that minimize  $C_{\text{KL}}$  is precisely equivalent to solving the so-called "minimum-cut" problem.

Since the size of QPUs are usually fixed, an additional constraint must be added during minimization of  $C_{\text{KL}}$ :

$$\vec{v}_j^T \vec{v}_j =$$
Size of QPU  $j$ . (12)

Generally, a cardinality-constrained "minimum-cut" problem is substantially harder than the unconstrained variant. However, approximate solvers can efficiently generate satisfactory solutions in practice [22]–[24]. A technique that we adopt and implement here is spectral partitioning. Consider the case where the sizes of all QPUs are the same, i.e.  $\vec{v}_j^T \vec{v}_j = s$  is constant for all j, and the corresponding minimization problem is of the "Kernighan-Lin" variety [25]. Since  $\mathcal{L} = D - A$  is Hermitian, the Courant-Fisher theorem implies that orthonormal eigenvectors ( $\vec{u}_j = \vec{v}_j/\sqrt{s}$ ) of  $s\mathcal{L}$  corresponding to the first k lowest eigenvalues minimizes  $C_{\text{KL}}$  while satisfying the cardinality constraint [26]. While the theorem holds strictly only when  $\vec{u}_j \in \mathbb{C}^N$ , in practice spectral partitioning nevertheless yields good approximate solutions when entries in  $\sqrt{s}\vec{u}_j$  must be rounded to 0 or 1. Partitioning in the case of clusters of unequal sizes have also been studied [24], [27].

Once a good partitioning is found, we assign logical qubits from the input quantum circuit to a random qubit within the target QPU (as specified by  $\{\vec{v}_j\}$ ), whereupon a more traditional swap insertion method as described in Section II-B is used if any one QPU has an internal topology sparser than all-to-all. Note, while we use the language of interand intra-QPU here, the preceding discussion is applicable even if the architecture does not strictly speaking contain interconnected QPUs, so long as it satisfies the conditions laid out in Section III-A.

For the interested reader, previous (static/global) qubit mapping strategies have been proposed and implemented [28], [29]. Our approach differs in that it focuses on the minimization of inter-QPU operations specifically, so we are able to leverage efficient graph-CUT solvers to better handle large QPUs/circuits.

## C. Local optimization

In Section III-B, the coupling map  $G_{\text{circ}}$  had been constructed by considering *all* two-qubit gates in the quantum circuit. For an *initial* assignment of logical qubits to QPUs, it is reasonable to look at the circuit as a whole. However, such a construction strips out the chronological order in which operations are performed during execution of the quantum circuit. Since most quantum gates are *not* commutative (so chronological order matters), and because a significant source of bottlenecks is slow inter-QPU operation times (see Section II-A), it is important to ensure that heuristic we might use for that optimization takes into account temporal structures and correlations in the program being executed.

To give a simple concrete example, suppose a quantum circuit prescribes many two-qubit gates between qubits  $q_1$  and  $q_2$  as well as between  $q_1$  and  $q_3$ . Globally, this implies a strong preference for  $q_1$ ,  $q_2$ , and  $q_3$  all to be clustered. However, if  $q_1$  and  $q_3$  interactions are chronologically localized to times *much later* than  $q_1$  and  $q_2$  interactions (suppose they are temporally separated by much more than relevant hardware timescales), then there is no longer any reason to insist that  $q_2$  and  $q_3$  be clustered – there is no cost to  $q_2$  being "far away" by the time  $q_1, q_3$  couplings need to be realised.

In order to exclude spurious clustering constraints from interactions that are temporally too far separated, we elected to re-construct  $G_{\rm circ}$  based only on a subset of operations in the quantum circuit. To do this, we reasonably assume that the target hardware is sufficiently well-characterized such that operation times for various gates are known. That way, each operation stipulated in the quantum circuit can be assigned an *expected* time-to-execution,  $t_{\rm gate}$ . We then specify a rolling time interval,  $[t_{\rm start}, t_{\rm start} + \Delta t)$ . We then construct a  $G_{\rm circ}$  by considering *only* gates that occur within that rolling window (i.e.  $t_{\rm start} \leq t_{\rm gate} \leq t_{\rm start} + \Delta t$ ). That circuit graph is then subjected to the same minimum cut treatment as in Section III-B.

Discussions of specific techniques for selecting optimal parameters that define the rolling window is outside the scope of this manuscript. For the purposes of ensuing experimental results, one effective choice is simply to select  $\Delta t$  to correspond to the largest limiting timescale of the target hardware, such that the availability of execution resources (like distributed EPR-states) is unlikely to depend on operations performed more than  $\Delta t$  ago. In turn, a set  $t_{\text{start}}$  can simply be chosen so as to produce disjoint time windows that cover the quantum circuit from start to end of execution.

Once an approximate minimum-cut is found on a (temporally) localized  $G_{circ}$ , we can compare the new QPU assignment it implies to the existing one (for the first rolling window, the existing assignment is the one found from the global graph in Section III-B). A decision is then made as to whether to effect a QPU *re*-assignment (by means of EPR-mediated teleportation, swap or physical transport) or to simply leave the current assignment as-is relying instead on logical swap insertions and/or EPR-mediated CNOT (see Section II-A).

We point out that for small  $\Delta t$  and/or very deep quantum circuits, one may have to perform partitioning of many graphs. Fortunately, graphs corresponding to distinct time windows can be partitioned in embarrassingly parallel fashion. Since most quantum algorithms are useful only when they have bounded runtime, the number of time windows in our local optimization scheme is similarly bounded.

## A. Methodology

In order to test our optimization methods, we implemented the techniques discussed in Section III-C as a Python/NumPy/Numba library (referred to as "MultiQopt" below). In order to standardize inputs, we implemented interfaces to the IBM's QISkit software development kit (SDK) so that quantum circuits can be defined in terms of QISkit [30] circuit objects or as Quantum Assembly (QASM) 2.0 strings [31]. Since graph partitioning is central to our technique, our implementation can call external partitioners like KaHyPar [23] and MeTiS [22] as well as an internal spectral partitioner.

In addition to a quantum circuit, the target hardware topology ( $G_{cmap}$ ) can be optionally supplemented with a "roleassignment" for various physical qubits. Among other things, physical qubits can be explicitly assigned to particular QPU objects, and qubits can can be earmarked for "special use" like holding an EPR state. The output of our implementation is an optimized QISkit circuit object, along with logical-to-physical qubit assignment lookup tables and possibly custom QISkit instructions for EPR-mediated operations.

We compiled quantum routines from a suite of benchmark circuits [32], [33], targeting an architecture consisting of two clusters of all-to-all coupled QPUs interconnected with two EPR-mediated interconnects. Given an input quantum circuit occupying N-qubits, we set the size of each target QPU to  $\lceil N/2 \rceil + 2$  (the added two qubits on each QPU serves as an EPR-state reservoir). This architecture choice is deliberate as it falls in the regime where assumptions behind our optimizations hold. But more importantly, it is representative of an architecture that trapped-ion quantum computer builders foresee in the near-future [11].

For comparison, we also compiled the same circuits targeting the same architecture with QISkit (using compile option "optimization\_level=3", stipulating maximum optimizations at the expense of longer compile times) [30]. In all cases, the target "native" gates were selected to be the set  $\{r_x, r_z, h, cx\}$ . Here, cx is the CNOT operation defined in 2 and:

$$r_x(2\theta) = e^{i\sigma_x\theta} = \begin{bmatrix} \cos\theta & i\sin\theta\\ i\sin\theta & \cos\theta \end{bmatrix}$$
(13)

$$r_z(2\theta) = e^{i\sigma_z\theta} = \begin{bmatrix} e^{-i\theta} & 0\\ 0 & e^{i\theta} \end{bmatrix}$$
(14)

$$h = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1\\ 1 & -1 \end{bmatrix}. \tag{15}$$

The benchmark environment is an AMD Ryzen 5 5600X machine with 16GB DDR4-3600 memory, with Arch Linux kernel 5.15.1. Some additional development environment information include Python-3.8, NumPy-1.21.1, Numba-0.54, and QISkit-0.26. The outputs of all compilers were then analyzed for (a) total number of two-qubit gates (b) total number of "expensive" interconnect uses, here defined to be any two-qubit operation that spanned the two all-to-all coupled qubit clusters and (c) compilation time.

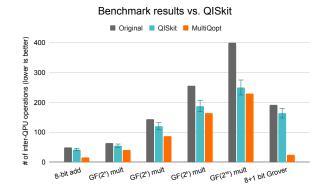


Figure 2. Benchmark result showing number of inter-cluster operations, comparing MultiQopt to QISkit (ver. 0.26). The original circuit (gray) which was compiled onto an all-to-all connected architecture is re-compiled onto the target dual QPU architecture using QISkit (turqoise) and MultiQopt (orange). Compilation with MultiQopt shows a significant reduction in the number of inter-cluster operations.

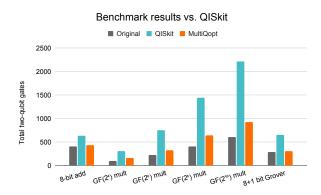


Figure 3. Benchmark result showing total two-qubit gates, comparing Multi-Qopt to QISkit (ver. 0.26). The original circuit (gray) which was compiled onto an all-to-all connected architecture is re-compiled onto the target dual QPU architecture using QISkit (turqoise) and MultiQopt (orange). Compilation with MultiQopt shows a significant reduction in the number of two qubit operations.

## B. Results

We show results for several familiar circuits (an adder, multipliers of various sizes, a Grover routine) in Figure 2 and Tables I - III. Benchmark results for additional input programs are shown in the Appendix. Additionally, current and more extensive sets of benchmark results can be found online at [34].

In Figure 2, we see a clear improvement over QISkit in the quantity of interest, the total number of interconnect uses. Additionally, we also show in Figure 3 that this gain is *not* won at the cost of total two-qubit gates – the latter remains significantly lower with our approach compared to QISkit. We attribute this behaviour to the fact that our approach is naturally suited to mapping classes of graphs that are "clustered" as we've described in Section III-A, whereas QISkit's heuristic algorithm, SABRE, isn't. Table I lists additional details about each input program in their *uncompiled* form as read from their respective QASM files. Logical qubits are assumed to

#### Table I

BENCHMARK BASELINES, SHOWING TWO-QUBIT GATE COUNTS ON SEVERAL SUBROUTINES AS DEFINED IN THEIR RESPECTIVE INPUT QASM FILES. \*THE BASELINE "INTER-QPU" COUNT IS BASED ON A TRIVIAL MAP BETWEEN LOGICAL AND PHYSICAL QUBITS.

		Ba	ase
	#-qb	Total 2-qb	InterQPU*
8-bit add	24	409	49
$GF(2^4)$ mult	12	99	64
$GF(2^6)$ mult	18	221	144
$GF(2^8)$ mult	24	405	256
$GF(2^{10})$ mult	30	609	400
8+1 bit Grover	9	288	192

Table II BENCHMARK RESULTS FOR MULTIQOPT

MultiQopt	Global pass	w/ local op	timization	Runtime
MultiQopt	InterQPU	Total 2-qb	InterQPU	Kultuline
8-bit add	22	433	16	0.73s
$GF(2^4)$ mult	49	157	41	0.41s
$GF(2^6)$ mult	109	329	87	1.47s
GF(2 <sup>8</sup> ) mult	199	646	164	4.36s
$GF(2^{10})$ mult	301	921	229	8.82s
8+1 bit Grover	48	304	24	1.13s

map to physical ones in *naive* fashion; since no attempt is made to map to the target hardware topology, total two-qubit gates tends to be lower in the "original" input circuit owing to the lack of additional swap operations being inserted (see Section II-B). Table II shows results for our MultiQopt optimizer. The column labelled "Global pass" shows results with just the initial global QPU assignment pass (Section III-B) whereas the column labelled "local optimization" shows the full compilation run that includes local optimizations (Section III-C). The former does not report a separate column of total two-qubit gates because by construction, that is *not* affected by the global pass. Finally, Table III shows corresponding results for QISkit (ver. 0.26). Since QISkit outputs exhibit significant run-to-run variation in inter-QPU two-qubit operations, we also report the spread, aggregating results over 30 repeated runs.

# V. DISCUSSION AND CONCLUSION

We have discussed a multi-QPU centric quantum circuit compilation and optimization approach, premised upon the idea that inter-QPU operations are likely to remain expensive and scarce for the foreseeable future, despite being essential to the serious scaling up of quantum computers. Recognizing local structures in input quantum circuits allows for more flexible optimizations. Our approach also reduces to wellunderstood graph theoretic problems that admit approximate solutions that can be found efficiently for large classes of common graphs.

When targeting architectures likely to be typical in multi-QPU architectures in the near future, our benchmarks indicate our optimization approach yields significantly simpler circuits. Despite its multi-QPU centric background however, wellknown bounds suggest that even monolithic QPU architectures with fairly common topologies may well benefit from

Table III BENCHMARK RESULTS FOR QISKIT 0.26 (AGGREGATED OVER 30 RUNS).

	Qiskit 0.	.26 transpile (	opt=3)
	Total 2-qb	InterQPU	Runtime
8-bit add	630	$42 \pm 12$	2.69s
$GF(2^4)$ mult	310	$55\pm 8$	1.34s
$GF(2^6)$ mult	757	$120 \pm 15$	2.75s
GF(2 <sup>8</sup> ) mult	1444	$188 \pm 14$	5.12s
$GF(2^{10})$ mult	2217	$250 \pm 25$	7.83s
8+1 bit Grover	652	$164 \pm 27$	2.77s

our methods; but we leave benchmarking of these alternate topologies for a future work.

Some readers may recognize optimizations like midexecution QPU re-assignment as being vaguely analogous to runtime optimizations that aim to maximize cache coherency and residency in multi-CPU classical architectures. Indeed, they share the common goal of minimizing QPU (or CPU) idle time by attempting to ensure relevant data is nearby when or where they at needed. Unlike classical measures, however, quantum information possess uniquely quantum idiosyncrasies; the no-cloning theorem for example implies that except in very narrow circumstances quantum data almost always needs to be *moved*, *not copied*. But QIP also allows for the use of shared resource states that can be used after-the-fact to generate large arbitrary entangled states without the various QPUs having to interact any further, but for the exchange of *classical* bits.

All of this necessitates careful (re-)thinking of optimization strategies for multi-QPU systems. The present manuscript represents a promising step in that direction.

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#### APPENDIX A: ADDITIONAL BENCHMARK RESULTS.

Tab. IV shows benchmark results for a large variety of other input quantum programs and sub-routines. As described in the main text, we show MultiQopt compared with QISkit 0.26, called with the same target hardware topologies.

		Base	se	Qiskit 0.	Qiskit 0.26 transpile (opt=3)	(opt=3)	EN, globa	EN, global pass only	EN, wit	EN, with local optimization	nization
	dp-#	Total 2-qb	InterQPU	Total 2-qb	InterQPU	Runtime	InterQPU	Runtime	Total 2-qb	InterQPU	Runtime
Barenco (x3)	5	24	16	41	$13 \pm 4$	0.289s	~	0.006179s	28	4	0.061137s
Barenco (x4)	7	48	32	94	$25\pm16$	0.631s	16	0.011019s	56	8	0.163377s
Barenco (x5)	6	72	48	156	$44\pm11$	1.060936s	16	0.016897s	76	8	0.260133s
Barenco (x10)	19	192	128	465	$130\pm25$	3.395s	16	0.060116s	196	12	0.75719s
QCLA (mod 7)	26	382	69	794	$77 \pm 34$	5.676s	56	0.069019s	392	32	2.021352s
QCLA (com 7)	24	155	24	212	$10\pm 6$	1.962s	12	0.026569s	188	10	0.345878s
QSLA (mux 3)	15	80	26	155	$22 \pm 4$	1.356s	15	0.016184s	86	9	0.2112s
HWB (x6)	7	116	55	227	$56 \pm 23$	1.479s	52	0.023293s	126	28	0.767694s
Hamming (low)	17	236	52	652	$121\pm16$	4.531s	44	0.056574s	240	41	1.447838s
Hamming (medium)	17	534	99	1247	$271 \pm 49$	8.593s	53	0.139646s	554	36	4.9049s
$GF(2^7)$ mult	21	300	196	1013	$145\pm19$	6.799s	149	0.057228s	344	109	4.441129s
GF(55) mult	6	48	30	122	$22\pm 6$	0.829s	12	0.010317s	52	7	0.120845s
MQ-Toffoli (x3)	5	18	12	34	$11 \pm 4$	0.238s	4	0.005102s	20	2	0.03555s
MQ-Toffoli (x4)	7	30	20	59	$15\pm 6$	0.420s	∞	0.007605s	32	2	0.078723s
MQ-Toffoli (x5)	6	42	28	92	$26\pm9$	0.661s	∞	0.010962s	44	2	0.109068s
MQ-Toffoli (x10)	19	102	68	254	$69 \pm 11$	2.001s	∞	0.033435s	104	9	0.3145s
RC adder (6-qb)	14	93	11	157	$31 \pm 17$	1.376s	11	0.01955s	97	9	0.209832s
5 mod 4	5	28	19	46	$14\pm5$	0.320s	14	0.006838s	32	2	0.10531s
C-sum (mux 9)	30	168	24	424	$32 \pm 11$	3.267s	16	0.026376s	174	14	0.308804s
QFT (4-qubit)	5	46	30	79	$25\pm12$	0.588s	20	0.013631s	50	8	0.212407s
VBE-Adder	10	0 <i>L</i>	20	113	$22\pm7$	0.891s	14	0.013919s	72	L	0.189217s
Mod-reduce	11	105	31	175	$31 \pm 12$	1.403s	30	0.025929s	111	14	0.557424s
			EX	Table IV EXTRA BENCHMARK RESULTS: QISKIT AND EN COMPILER	Table IV RK RESULTS: QI	/ ISKIT AND EN	COMPILER.				
					1						