

Low-Power Rail-to-Rail Comparator in 130 nm CMOS Technology

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Abstract—The paper addresses a novel comparator topology capable of processing the input signal in rail-to-rail range, designed in standard general purpose twin-well nanoscale CMOS technology *without* two differential input pairs. The power supply voltage of 1.2 V was used and the operating temperature span was set to a standard industrial limits (from -20°C up to 85°C). Its application is aimed to low-power energy harvesting circuit, therefore its current consumption has been minimized as much as possible, since it stands out as a crucial parameter. The presented topology operates in so-called *current-mode* and represents a gate-driven version of already published topology, which was described in deep detail in [1]. The designed comparator has been verified for robustness and accuracy across all process and temperature corners, as well as by the Monte-Carlo analyses. Its power consumption does not exceed $1.05\ \mu\text{W}$ in worst-case scenario, while in the nominal conditions, the value remains safely in the first half of nW range. The topology also shows great potential for low-voltage applications, as well since it employs only two stacked transistors.

Index Terms—Low-Power, Comparator, CMOS, Rail-to-Rail, Energy Harvesting

I. INTRODUCTION

The ongoing popularity of hand-held and battery-powered devices is becoming even more pronounced by the onset of *Internet-of-Things* – *IoT* solutions on the market [2]. The ever-growing demand for batteries, and recently, the energy-harvesting units are driving the design specifications of consumer electronics into low-power and/or low-voltage domain. The design considerations of an integrated energy-harvesting circuits are strongly dependent on the type of employed harvesting element. However, the requirement, which is common for any energy harvester system is its own internal power consumption. Minimizing the quiescent current draw introduces another layer of challenges even for an experienced circuit designers as the overall power consumption of low-power / low-voltage circuits lies within the range of nW and μW .

An integral part of any power management unit is a voltage comparator, which is usually employed in the regulation feedback loop. There have been developed numerous comparator topologies with their own pros and cons [3]–[5]. In low-voltage and low-power systems, the ability of processing the input voltage in rail-to-rail range becomes a necessity. This introduces yet another challenge in terms of circuit design and

power consumption. The traditional approach usually employs two differential pairs, each comprised of opposite transistor types. Some recent designs resorted to employing rather exotic approaches, such as bulk-driving the MOS transistors [6]. This represents truly an elegant solution to achieving rail-to-rail input range without two differential pairs. However, it is applicable only for circuits with supply voltage below $V_{DD} \approx 0.6\text{ V}$ due to risk of latch-up effect [7]. The discussed novel topology represents an extension of already published bulk-driven low-voltage comparator, as it also works in current-mode, but the modifications introduced to the topology avail its application in standard gate-driven circuits with nominal levels of supply voltage. The novel topology, however, is still suitable for low-voltage applications as well, since it uses only two-staked transistors, which lowers the requirements for minimal supply voltage to keep transistors saturated.

The paper is organized as follows. The first part describes the theoretical background and the proposed comparator topology. The second section of the article discusses the achieved simulation results obtained from Monte-Carlo analysis, as well as Corner analyses using various process and temperature corner combinations. The final chapter concludes the paper along with our intended future research.

II. THE PROPOSED COMPARATOR

The presented rail-to-rail comparator is consist of two main parts. The first one is responsible for processing the input analog voltage and creating a *difference* signal. The second part is responsible for shaping the difference signal and generating the digital output. The proposed analog topology of rail-to-rail comparator is depicted in Fig. 1.

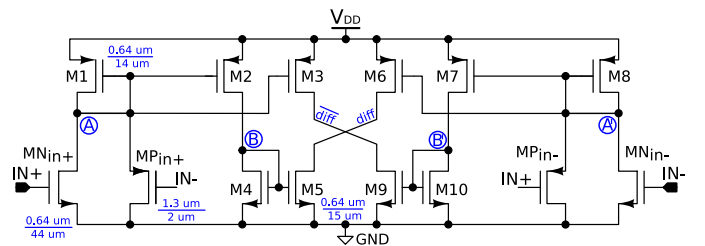


Fig. 1. The proposed topology of rail-to-rail analog core.

The circuit works in so-called *current-mode* and is fully symmetrical, as expected. Thanks to this fact, let us describe just the left-hand side of the presented topology. MOS transistors MN_{in+} and MP_{in+} act as current sources modulated by the input voltage level. The rail-to-rail input range is achieved by employing both transistor types in the input circuit branches. One transistor is connected as classic common-source amplifier, while the other acts as source-follower. One can observe the cross-coupled gate terminals of the respective devices. This ensures a complete symmetry of the analog core. Devices M1, M2 and M3 form a current mirror with unity mirroring ratio, copying the current into the rest of the circuit. Transistors M4 – M5 also create unity current mirror, in order to flip the current flow direction for the right-hand counterpart. The nodes *diff* and \overline{diff} interconnect both sides of the comparator analog core. The difference voltage generated in these nodes is obviously dependent on the input voltage difference (proportional to the current difference) and its small-signal amplification governed by (1).

For better clarity, we did not include the switching transistors in the schematic, which are activated when the comparator's function is being inhibited. In this case, the switches are used to tie-off the transistors' gates in the current mirror block and to disable the current flow in the input branches. The overall current consumption is minimized by the $\frac{W}{L}$ ratios of respective transistors. The increased channel length lowers the drain current and small-signal output conductance, but on the other hand it also lowers the device's transconductance. Hence, the biasing current and the maximum operational frequency are in direct contradiction as the design considerations and are therefore a subject of trade-off between the final circuit parameters. Another advantage of larger $W.L$ area of the designed transistors is an increased robustness and resistance to fabrication process variations [8].

The proposed topology also exhibits several interesting properties. The capability of working in ultra low-voltage conditions thanks to only two stacked transistors, which need to be kept in saturation. Another important property of the presented comparator topology is availability of introducing the voltage hysteresis into the transfer characteristics without any external components. By selecting different $\frac{W}{L}$ ratio of the input transistors or in the current mirror block, one can disbalance the current flow and therefore shift the tripping point of the comparator. The hysteresis does not have to be symmetrical or applied in both directions of the voltage sweep, which is yet another interesting possibility.

We have also carried out the small-signal analysis for the proposed circuit. Since the input branches are cross-coupled, we have to analyze the whole circuit, not just one half of it. In our case, we have chosen to set the input conditions as follows. The $IN+$ terminal acted as a small-signal input and $IN-$ terminal was connected to a constant reference voltage. The resulting small-signal model is depicted in Fig. 2.

The voltage gain in the node \overline{diff} can be expressed by (1). The considerations for simplifying the overall voltage gain include the following. All devices need to be in saturation

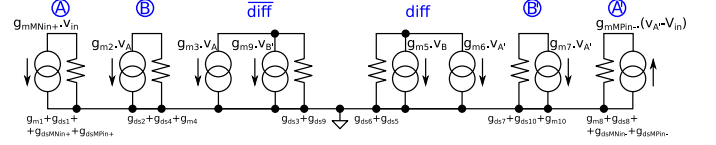


Fig. 2. The complete small-signal model of the proposed analog core.

regime, corresponding transistors have to be matched in layout representation and all transistors are designed with reasonable channel length so we can neglect their output conductance, when compared to their transconductance.

$$A_{V_{\overline{diff}}} \approx \frac{\left[\frac{g_{m3} \cdot g_{mM_{in+}}}{g_{m1}} + \frac{g_{m9} \cdot g_{m7} \cdot g_{mMP_{in-}}}{g_{m10} \cdot (g_{mMP_{in-}} - g_{m8})} \right]}{g_{ds3} + g_{ds9}} \quad (1)$$

The second major part of the proposed comparator is the digital block responsible for generating the output signal. Its schematic diagram is depicted in Fig. 3 along with the devices' dimensions.

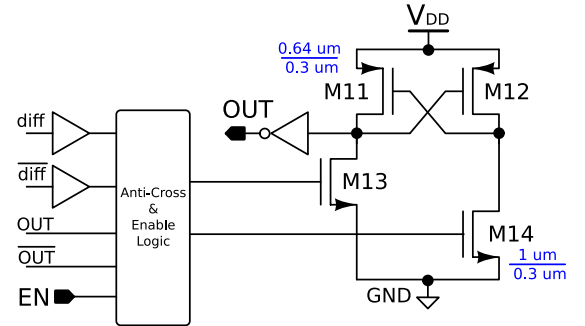


Fig. 3. The output latch along with the controlling logic.

Transistors M11 – M14 form a latching circuit, in order to increase the noise margin of the output node. The final inverter is sized according to loading capacitance and slew rate requirements. The buffers shape the difference signals from analog core, which are then processed by the digital controlling block. Despite its simplicity, this block has been described in HDL language and synthesized, in order to minimize the gate count and the static power consumption. The controlling block prevents the devices M13 and M14 from turning-on simultaneously, which would cause a catastrophic short between the power supply node and the ground. Such a scenario can occur when the power supply voltage is significantly rippled, which is probable with energy harvesting system.

III. SIMULATION RESULTS

The parameters of the designed comparator have been verified by various types of analyses. The most basic analysis of any voltage comparator is arguably its transfer characteristics. In our simulation scenario, we performed the DC analysis with three different reference voltages. One in the center of the voltage span and two voltages only 10 mV from the supply

rails, in order to verify the rail-to-rail capability. The corner analysis consisted of all possible process corner combinations with added temperature limits and room temperature. There have been 27 simulations carried out in total and the results of the described analysis are shown in Fig. 4.

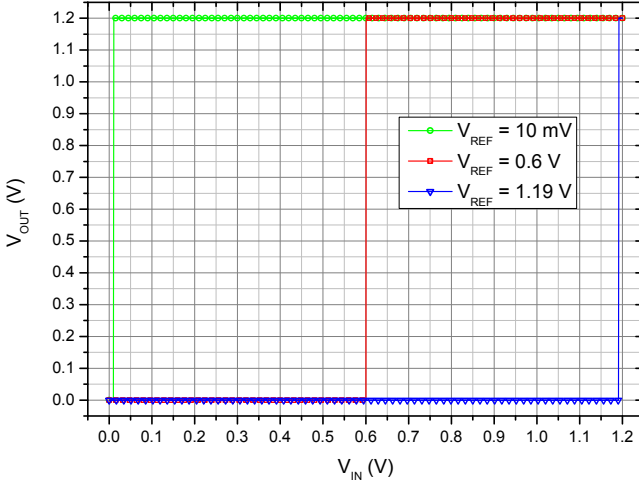


Fig. 4. Transfer characteristics in various PVT conditions.

As one can observe, the output voltage waveforms are overlapping each other, which can be considered a sign of robustness and stability in all PVT variations.

The most important parameter in terms of comparator's accuracy is definitely its input offset voltage. For purposes of investigating its value in our circuit design, we set up the transient Monte-Carlo analysis for temperature limits and the ambient room temperature, as well. The reference voltage was set to $V_{DD}/2$ and the input triangle voltage was swept over a long period of time, in order to minimize the effects of possible propagation delay. The simulations also took into account the transistor matching, general components mismatch and random process variations, as well. The histogram of the input offset voltage is displayed in Fig. 5.

The input offset voltage was calculated for both output edges separately, but were included in one statistical population. We have performed 500 simulations for each temperature, which results in 3000 offset values all together. The average value for 3000 samples remains below $3 \mu\text{V}$, which is truly an astonishing result for a circuit without post-processing or digital trimming. The standard deviation also remains in μV range, which also confirms very low value of expected measured offset voltage in reality. Such a low value of input offset voltage opens a relevant question about introducing an internal hysteresis (e. g. 5 mV), which would prevent the output from toggling due to noise fluctuations. However, we would like to verify the functionality of the novel topology without a deliberate input offset. If the laboratory measurements confirm the aforementioned concerns, the hysteresis will be applied in the re-design.

The overall power consumption as another crucial parameter is, as expected, dependent on input voltage conditions, since

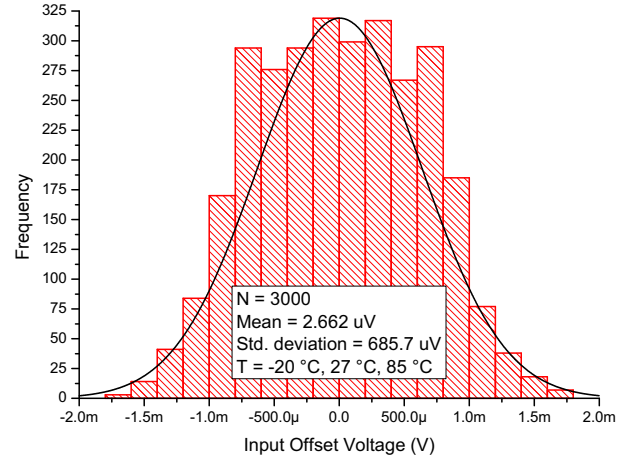


Fig. 5. Monte-Carlo analysis of input offset voltage for both output edges and various operating temperatures.

the input voltage modulates the current flow in the internal circuit branches. The highest current draw has been observed with both input voltages close to V_{DD} . The Monte-Carlo analysis of power consumption has been performed using the worst-case input voltage conditions at ambient temperature and both temperature limits, while calculating the average value of current drawn from the power supply over time. Our scenario consisted of 500 simulations for each operating temperature, which results in 1500 simulations in total. The histograms of described analysis along with calculated average values is depicted in Fig. 6.

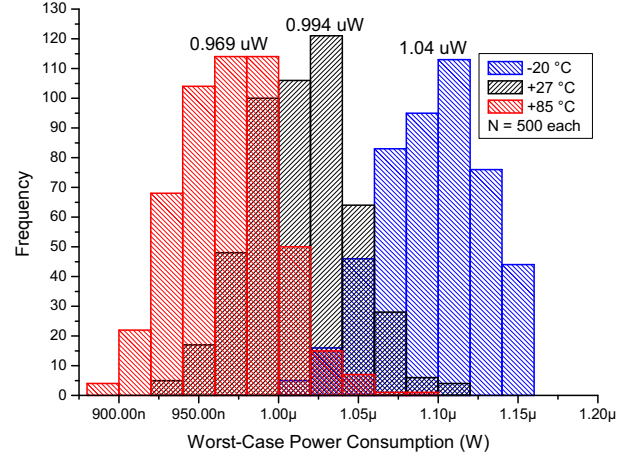


Fig. 6. Monte-Carlo analysis of power consumption at various temperatures with calculated average value.

All three histograms exhibit normal distribution with standard deviation about $\sigma \approx 30 \text{ nW}$, which can be considered a sign of robust design resistant to fabrication process variations and reliable indication of the real value obtained by laboratory measurement on real manufactured silicon sample. It is important to mention that the reported power consumption of the proposed comparator is intended for on-chip applications

without ESD structures and other significant parasitic loads. The dynamic properties of the proposed comparator have been investigated, as well. As stated above, the minimized power consumption affects the slew rate in the internal nodes tremendously. Hence, we can expect the maximum operational frequency in kHz range. We performed a transient simulation with digital signal acting as an input voltage and stepped the reference voltage level across the whole voltage range. This way, we verified the dependence on the overdrive voltage, as well as the reference voltage. The loading capacitance was set to $C_{LOAD} = 75$ fF, which is rather higher value for given CMOS technology considering the on-chip application of the comparator. The described simulation scenario was repeated for every PVT corner. The propagation delay was calculated for both output edge types and the obtained results are shown in Fig. 7.

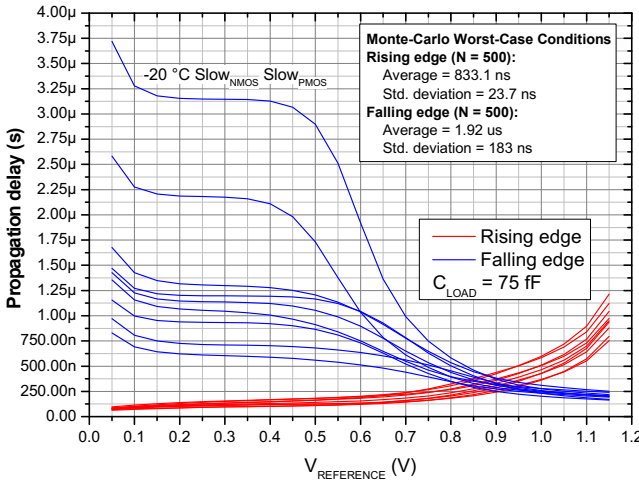


Fig. 7. Propagation delay for various reference voltages and PVT corners.

We also carried out Monte-Carlo analysis for the worst-case temperature and voltage conditions, which were $T_{AMB} = -20$ °C, $V_{REF} = 1.15$ V for rising output edge and $V_{REF} = 50$ mV for falling output edge. The results are inset into Fig. 7. The mismatch between the values from corner and Monte-Carlo analysis for falling output edge remains unexplained so far. However, the results of Monte-Carlo are by nature closer to reality and therefore can be considered more accurate and more favorable for practical applications. With propagation delay in range of μ s, we can therefore expect the maximum frequency in 10s, maybe in 100s of kHz in an on-chip applications.

IV. CONCLUSION

We have presented a novel topology of a low-power analog voltage comparator with rail-to-rail input range. The topology was designed in 130 nm CMOS technology and its parameters have been extensively verified by means of Corner and Monte-Carlo analyses in industrial temperature range. The obtained results confirm robustness, accuracy and low-power requirements of the proposed comparator working in

so-called current mode. The power consumption in nominal PVT conditions is reported at $P_{DD} = 330$ nW, while the *worst-case* scenario sets the power consumption right about $P_{DD} = 1$ μ W. The topology itself is also capable of proper functioning in ultra low-voltage applications, which makes it rather universal solution for low-voltage / low-power on-chip comparator design. Moreover, the circuit design can be fully automated by means of a spreadsheet or dedicated application while using g_m/I_D design methodology thanks to absence of an internal reference or biasing block. To minimize the power consumption even further, we implemented enable function, which also can be used to mimic a behavior of dynamic clocked comparators.

Our future research and development include the large-signal analysis of the analog core, as well as the laboratory measurements, which would be carried out on fabricated silicon chip samples. The proposed comparator will also be implemented in successive approximation analog-to-digital converter (SAR ADC) or in maximum power point tracking (MPPT) block to maximize the energy harvester's efficiency.

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REFERENCES

- [1] L. Nagy, D. Arbet, M. Kovac, M. Potocny, M. Sovcik, and V. Stopjakova, "Performance analysis of ultra low-voltage rail-to-rail comparator in 130 nm cmos technology," in *2019 IEEE AFRICON*, 2019, pp. 1–5.
- [2] L. Wang, C. Zhan, L. He, J. Tang, G. Wang, Y. Liu, and G. Li, "A Low-Power High-PSRR CMOS Voltage Reference with Active-Feedback Frequency Compensation for IoT Applications," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–4.
- [3] S. Babayan-Mashhadi and R. Lotfi, "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 2, pp. 343–352, Feb 2014.
- [4] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *2008 IEEE Asian Solid-State Circuits Conference*, Nov 2008, pp. 269–272.
- [5] Y. Li, W. Mao, Z. Zhang, and Y. Lian, "An ultra-low voltage comparator with improved comparison time and reduced offset voltage," in *2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Nov 2014, pp. 407–410.
- [6] L. Nagy, D. Arbet, M. Kovac, M. Potocny, M. Sovcik, and V. Stopjaková, "Dynamic properties of ultra low-voltage rail-to-rail comparator designed in 130 nm cmos technology," in *2020 23rd International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, 2020, pp. 1–4.
- [7] N. Rezzak and J.-J. Wang, "Single event latch-up hardening using tcad simulations in 130 nm and 65 nm embedded sram in flash-based fpgas," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1599–1608, 2015.
- [8] M. J. Pelgrom and A. C. Duinmaier, "Matching properties of mos transistors," in *ESSCIRC '88: Fourteenth European Solid-State Circuits Conference*, 1988, pp. 327–330.