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Keynote 2 – Past, Current, and Future of Faster, Cheaper, Better

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Abstract

The Mars Pathfinder landed in the Ares Vallis valley on July 4th, 1997, and after deploying the Sojourner rover and sending back detailed panoramic color photos the mission captured the world's attention and people's imagination. The Mars Pathfinder development was an example of doing design quickly, at less cost and having it work better than expected (give or take a few software "glitches"). So why does industry have so much trouble doing "Faster, Cheaper, Better" in larger and more complex FPGA based systems since then? This presentation takes a journey through insights gained using different tools, techniques and methods to sort through what works, where we need to go and what the future holds.

Topics covered are why ESL/HLS methods have limited acceptance, the "superman" dilemma, issues with both multi-core and RCC development, the problem with using languages (i.e. English) to describe system specifications and how software based agile and model based engineering techniques can greatly improve the FPGA development process..

Short Bio

Tim Gallagher is currently a Lockheed Martin Fellow working for the Space Systems Company Avionics group and the Software Engineering Technical Excellence team as a spaceborne reconfigurable computing specialist. Previously Tim was the Command & Data Handler FPGA technical lead for the next-gen GOES-R weather forecasting satellite program and Principle Investigator for the Advanced Software Multi-Core R&D effort targeting the Tilera based Maestro processor developed on the USG OPERA project.

Tim specializes in applying agile software methods for rapid error-free hardware development including model-based engineering, test driven development, high-level synthesis and auto-coding techniques along with researching space-based reconfigurable computing architectures and fault tolerance/SEU mitigation techniques.

Tim is also involved with outreach to HPEC researchers including as a member of the NSF Center for High-Performance Reconfigurable Computing (CHREC) and held the position as 2012 Chair of the Industry Advisor Board. Tim received his bachelor's degree in Electrical Engineering from the University of Maryland and master's degree in Computer and Electrical Engineering from the University of Colorado, Boulder.