Building Time-Triggered Schedules for typed-DAG Tasks with alternative implementations

Houssam-Eddine Zahaf*, Nicola Capodeici⁺ *Université de Nantes, LS2N, France ⁺Unimore university, HiPeRT Lab, Italy

Abstract— Hard real-time systems like image processing, autonomous driving, etc. require an increasing need of computational power that classical multi-core platforms can not provide, to fulfill with their timing constraints. Heterogeneous Instruction Set Architecture (ISA) platforms allow accelerating real-time workloads on application-specific cores (e.g. GPU, DSP, ASICs) etc. and are suitable for these applications. In addition, these platforms provide larger design choices as a given functionnality can be implemented onto several types of compute elements.

HPC-DAG (Heterogeneous Parallel Directed Acyclic Graph) task model has been recently proposed to capture real-time workload execution on heterogeneous platforms. It expresses the ISA heterogeneity, and some specific characteristics of hardware accelerators, as the absence of preemption or costly preemption, alternative implementations and on-line conditional execution.

In this paper, we propose a time-table scheduling approach to allocate and schedule a set of HPC-DAG tasks onto a set of heterogeneous cores, by the mean Integer Linear Programming (ILP). Our design allows to handle heterogeniety of resources, on-line execution costs, and a *faster* solving time, by exploring gradually the design space.

Index Terms—Real-time partitioning, heterogeneous architecture, unrelated, preemption, time-table.

I. INTRODUCTION

Cyber-physical embedded systems are increasingly complex and demand more and more powerful computational hardware platforms. COTS¹ vendors provide hardware platforms featuring multi-core CPU hosts with a number hardware accelerators, in order to support timing constraints of complex real-time applications with machine learning and image processing software modules.

Typically, these platforms feature different ISA architectures, and different characteristics for the different cores. For example, the Jetson AGX platform features 8 CPU with ARM V8, Volta GPU (Graphical Processing Unit), a Deep Learning Accelerators (DLA), a Programmable Vision Accelerator (PVA). The differences between the different types of cores include not only ISA, but as well as the task scheduling, i.e. CPU can be usually scheduled with preemptive scheduling approaches where preemption costs can be negligible, while recent GPUs enable preemptive scheduling but with very variable costs², while when a workloads starts executing on DLA or PVA, the latter can not be preempted.

[Houssam : Some bla bla about how good it is to express alternative, and conditionals]. [Houssam : Say that it is complex

to make non-time consuming ILPs to solve the conditional problem, therefore they are not considered in this paper]

When it comes to scheduling, there are two major approaches for designing and scheduling HPC-DAGs onto heterogeneous cores : time-triggered and event-based approaches. In event-triggered systems, tasks are scheduled as a consequence of events i.e. task activation, deadlines, priority, etc. therefore the schedule is not necessarily known before run-time [1]. In contrast time-triggered systems, the system designer precompute/or totally compute in offline static execution schedule, i.e. time windows, for every job of every task during the whole system lifetime. Time-triggered and event-based approaches are incomparable as each exhibit advantages and disadvantages with respect to each other.

In contrast to our previous work in which we focus on event-based schedulers, this paper presents a time-triggered scheduler for a set of HPC-DAG tasks onto a heterogeneous multicore platform.

Contributions .:

- 1) Formulation of the problem using several ILP
- 2) Accelerating the analysis
- 3) taking into account heterogeneity
- 4) Adding partitioning
- 5) Adding global scheduling
- 6) taking into account preemption costs

II. SYSTEM MODEL

A. Architecture model

A heterogeneous architecture is modeled as a set of *execu*tion engines $Arch = \{e_1, e_2, \ldots, e_m\}$. An execution engine is characterized by 1) its execution capabilities, (e.g. its Instruction Set Architecture), specified by the engine's tag, and 2) its scheduling policy. An engine's $tag tag(e_i)$ indicates the ability of a processor to execute dedicated tasks.

As an example, a Xavier based platform such as the *NVIDIA pegasus*, can be modeled using 16 engines for a total of five different engine tags: 8 CPUs, 2 dGPUs, 2 iGPUs, 2 DLAs and 2 PVAs.

Tags express the heterogeneity of modern processor architecture: an engine tagged by dGPU (discrete GPU) or iGPU (integrated GPU) is designed to efficiently run generic GPU kernels, whereas engines with DLA tags are designed to run *deep learning inference* tasks. A deep learning task can be implemented and compiled to run on any engine, including CPUs and GPUs, however its execution behavior will be

¹Commercial Off The Shielf

²The cost varies from some micro-seconds to couple of milliseconds.

different, and its execution time will probably be lower when running on DLAs.

Therefore, we allow the designer to compile the same task on different alternative engines with different trade-offs in terms of performance and resource utilization, so to widen the space of possible solutions. As we will see in the next section, the HPC-DAG model supports *alternative* implementations of the same code.

In this paper, we consider time triggered scheduling. For every engine we build a schedule table, that dictates the scheduling at run-time.

B. The HPC-DAG task model

A *task* is a Directed Acyclic Graph (DAG), characterized by a tuple $\tau = \{T, D, N, \mathcal{E}\}$, where: T is the period (exact interarrival time between two consecutive activation of task τ); D is the relative deadline; The set of all the nodes is denoted by N

An edge $e(n_i, n_j) \in \mathcal{E}$ models a precedence constraint (and related communication) between node n_i and node n_j . The set of *immediate predecessors* of a node n_j , denoted by $\operatorname{pred}(n_j)$, is the set of all nodes n_i such that there exists an edge (n_i, n_j) . The set of *predecessors* of a node n_j is the set of all nodes for which there exist a path toward n_j . If a node has no predecessor, it is a *source node* of the graph. In our model we allow a graph to have several source nodes. In the same way we define the set of *immediate successors* of node n_j , denoted by $\operatorname{succ}(n_j)$, as the set of all nodes n_k such that there exists an edge (n_j, n_k) , and the set of *successors* of n_j as the set of nodes for which there is a path from n_j . If a node has no successors, it is a *sink node* of the graph, and we allow a graph to have several sink nodes.

A node n_i can be a sub-task or an alternative node. A subtask $v \in \mathcal{V}$ is the basic computation unit. It represents a block of code to be executed by one of the engines of the architecture. A sub-task is characterized by:

- A tag tag(v) which represents the engines where it is eligible to execute. A sub-task can only be allocated onto an engine with the same tag;
- A worst-case execution time C(v) when executing the sub-task on the corresponding engine processor.
- P(v) Maximum number of preemptions allowed for subtask v.
- cost(v) : The cost to split (preempt) task v

An alternative node $a \in A$ represents alternative implementations of parts of the graph/task. During the configuration phase, our methodology selects one between many possible alternative implementations of the program by selecting only one of the outgoing edges of a and removing (part of) the paths starting from the other edges for a given job. This can be useful when modeling sub-tasks than can be executed on different engines with different execution costs. The selected edge may differ from an activation to another according the system state when the job is executed, in contrast to our previous work [1] where the same alternative configuration is selected during the system lifetime. An alternative nodes always has at least 2 outgoing edges, so they cannot be sinks.

Example 1. Consider the DAG task described in Figure 1a. Each sub-task node is labeled by the sub-task id and engine tag. An Alternative node are denoted by square boxes. The black boxes denotes corresponding junction nodes for alternatives.

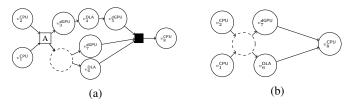


Fig. 1: Task specification and concrete tasks

Sub-tasks v_1^{CPU} and v_2^{CPU} are the sources (entry points) of the DAG. $v_1^{\text{CPU}}, v_2^{\text{CPU}}$ are marked by the **CPU** tag and can run concurrently: during the off-line analysis they may be allocated to the same or to different engines in a consecutive or parallel time windows. Sub-task v_4^{DLA} has an outgoing edge to v_5^{dGPU} , thus sub-task v_5^{dCPU} cannot start its execution before sub-task v_4^{DLA} has completed. Sub-tasks v_1^{CPU} and v_2^{CPU} have each one outgoing edge to the alternative node A. Thus, τ can continue the execution either:

- by following v₃^{dGPU} and then v₄^{DLA}, v₅^{dGPU} and finishing its instance on v₈^{CPU};
- 2) or by following a dummy node (denoted as dashed) to execute in parallel v_6^{DLA} or v_7^{dGPU} , and finishing its instance on v_8^{CPU} .

The two patterns are alternative ways to execute the same functionalities at different costs. Figure 1b represents one of the possible executions of task τ , where during the analysis, alternative execution pattern $(v_3^{dGPU}, v_4^{DLA}, v_5^{dGPU})$ has been dropped.

We consider a *periodic task* model, therefore parameter T represents the exact inter-arrival time between two instances of the same concrete task. When an instance of a task is activated at time t, all source sub-tasks are simultaneously activated. All subsequent sub-tasks are activated upon completion of their predecessors, and sink sub-tasks must all complete no later than time t + D. We assume *constrained deadline tasks*, that is $D \leq T$.

III. TIME TABLE CONSTRUCTION USING ILP

In this section, we describe how the time table for the HPC-DAG can be constructed. We consider both global and partitioned approaches. In the partitioned approach a sub-task is allocated to a given core during the system lifetime. Therefore, all execution time-windows of every job of a given sub-task are reserved on the same core, while in the global approach, different time intervals of the same job might be executed on different cores.

An optimal solution requires to assign every time unit from 0 to the hyper-period, on every core to a job or to *idle*.

Algorithm 1 Time-Table construction using ILPs

- 1: Input: Taskset \mathcal{T} , Architecture \mathcal{A} , Method : GLOBAL or PARTITIONED 2: **Output:** Time Table requirement task τ^*
- 3: it=0
- 4: while (not stop and not feasible) do
- nb int = 2^{it} 5:
- build_variables(nb_it); 6:
- 7: build objective();

build_sufficiency_constraints(); 8:

- build per proc overlapping constraints(); 9:
- build per job overlapping constraints(); 10:
- build finish before migrate constraints(); 11:
- 12: build_precedance_constraints();
- build non migration constraints(); 13.
- if (METHOD == PARTITIONED) then 14:
- build partitioning constraints(); 15:
- end if 16: 17: feasible = solve();
- if (feasible) then 18:
- 19:
- save_time_table
- return SUCCESS; 20:
- end if 21:
- 22: it + = 1
- 23. update stop condition(stop)
- 24: end while
- 25: return FAIL

Therefore, the design space to explore is large, and finding an optimal solution is an extremely time consuming operation. In this work, we explore the design space gradually. Rather than assigning processor time to jobs, we assign execution intervals to core.

Our approach selects a number of intervals per sub-task and increases it at each iteration. This allows to explore each iteration it explores a subset of the design space instead of exploring the whole design space at once, as described in Algorithm 1.

Our algorithm computes first the maximal possible number of intervals (nb_it) per job as nb_it = 2^{it} , where it denotes the iteration number starting from 0. Further, it iteratively increments it by 1. At each iteration, our algorithm builds an ILP and invokes the CPLEX solver.

If the ILP solver founds a feasible solution (i.e. a feasible schedule) our algorithm stops on SUCCESS, otherwise the system increases the number of intervals, and iteratively build and solve a new ILP with new variable list. When the maximum number if intervals is reached for every sub-task, and no feasible solution is found, the system aborts on fail. In the rest of this section, we describe how every ILP is built.

[Houssam : I need to think about if the algorithm is optimal or not? (doubt not)]

A. Building variables

At each iteration it is incremented and the number of intervals per sub-task changes. Hence, the first step to build our ILP is to define the variables list.

Our algorithm selects the number of intervals per sub-task at iteration it as $nb_i(v) = max\{nb_i, P(v)\}$. Therefore, sub-tasks that are executing onto a non-preemptive engine, $nb_i(v)$ is set to 1. For the sub-tasks executing on in a fully preemptive engine, the number of intervals is not defined in prior, $nb_it(v)$ is set to the maximum between nb_it and the sub-task worst case execution time. In the first iteration, every job must execute into a exactly one interval (i.e. nonpreemptively), even those that are fully preemptive as it = 0. For every interval, two variables are defined : s and f to

denote starting and finishing times respectively.

For every task, for every sub-task, for every job, for every interval, for every core, we generate f and s variables. Therefore, every variable is characterized by 5 indexes such that

 $s_{i,j,k,l,m}$ (respectively $f_{i,j,k,l,m}$) denotes the starting time (respectively finishing time) of the l^{th} interval of the k^{th} job of sub-task $v_{i,j}$ which is executing on core m. These variables and the relative constraints are generated only for cores where a given sub-task is allowed to execute, i.e. a sub-task that is meant to run on a GPU have no intervals defined CPU cores.

Variables $s_{i,j,k,l,m}$ and $f_{i,j,k,l,m}$ are bounded by the task activation, and task deadlines.

Therefore:

$$k \cdot \mathsf{T}_{i} \le \mathsf{s}_{i,j,k,l,m} \le \mathsf{f}_{i,j,k,l,m} \le k \cdot \mathsf{T}_{i} + \mathsf{D}_{i} \tag{1}$$

When a job execution is split to several intervals, its execution time is inflated by a penalty cost.

The procedure build_variables (Line 6) allows to build the variables and updates the task execution time as follows:

$$C(v)' = C(v) + \mathsf{nb}_{it}(v) * \mathsf{cost}(v)$$

B. Objective function

Once the list of variables are defined, our algorithm proceeds to build the objective function to maximize the slack for each job. Therefore, the objective function is set to maximize the differences between finishing and starting time for every interval, as follows :

$$\text{Maximize} \sum_{i=1}^{n} \sum_{j=1}^{|\mathcal{V}_i|} \sum_{k=1}^{H/T_i} \sum_{l=1}^{\mathsf{nb_it}(v_{i,j})} \sum_{m=1}^{M^{(\mathsf{tag}(v_{i,j}))}} \mathsf{f}_{i,j,k,l,m} - \mathsf{s}_{i,j,k,l,m}$$
(2)

Where :

- n : is the number of task in the system
- $|\mathcal{V}_i|$ The number of sub-tasks of task τ_i
- H/T_i The number of jobs between 0 and H the hyper period for task τ_i
- nb_it $(v_{i,i})$ The number of intervals in the current iteration, computed in the previous step.
- $M^{(tag(v_{i,j}))}$ The indexes of cores having the same tag as the current job.

C. Precedance constraints

To enforce the respect of precedance constraints, it is sufficient to express that the successors of a any sub-task, can start before it ends. In other words, any sub-task starting time must be greater to all its immediate predecessors finishing time. For sub-task $v_{i,j}$, multiple constraints can be generated as follows:

$$\forall k \in \{0, \cdots, \frac{H}{\mathsf{T}_{i}}\}, \quad \forall l \in \mathsf{nb_it}(v_{i,j}), \quad \forall m \in M^{tag(v_{i,j})}$$

$$\forall v_{i,j'} \in \mathsf{succ}(v_{i,j}), \quad \forall l' \in \mathsf{nb_it}(v_{i,j'}), \quad \forall m' \in M^{tag(v_{i,j'})}$$

$$\mathsf{f}_{i,j,k,l,m} \leq \mathsf{s}_{i,j',k,l',m'}$$
(3)

This constraints must be generated for every job, for every sub-task in every task. Please notice that these constraints are generated between successors within the same task instance (same k).

The precedance constraints between the different instances are enforced by the variables s and f bounds generated in variables building step.

D. Interval sufficiency constraints

After enforcing precedance constraints, we need to ensure that every job of every sub-task will receive sufficiently processor time to execute for its worst case execution time, including the costs of splitting the task (preemption). Therefore, the sum of interval lengths for every instance, must be larger than the job worst case execution time, as defined in following equation:

$$\forall i, \forall j, \forall k, \sum_{l} \sum_{m} \mathsf{f}_{i,j,k,l,m} - \mathsf{s}_{i,j,k,l,m} \ge \mathsf{C}(v_{i,j})'$$

E. Overlapping constraints

At this stage, only the constraints to ensure a single task execution have been defined. However, we need to ensure that the different tasks executing on the same cores have a correct behavior. Therefore, it is required that the the same processor is not allocated to different jobs at the same time and that the same job does not have reserved intervals on different cores at the same time. We call these constraints overlapping constraints.

First, we show how an o overlapping constraint can be expressed for intervals [s, f] and [s', f'], i.e :

$$[s, f] \cap [s', f'] = \emptyset$$

In Figure 2, we presents two scenarios scenarios where two interval [s, f] and [s', f'] overlap. Overlapping can be partial i.e. only a part of the interval is shared as in Sub-figure (a) or a total inclusion Sub-Figure (b).

In Figure 3, we present the only two cases to check that an overlapping is prohibited. Indeed, The first is interval should either finish before the first one **or** start after the second one as it is defined in Equation (4).

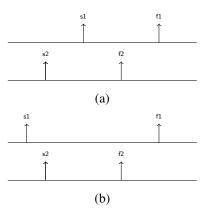


Fig. 2: Example of overlapping

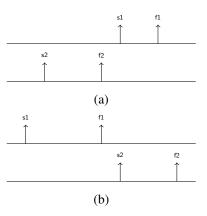


Fig. 3: Example of valid intervals

$$f \le s' \text{ or } f' \le s$$
 (4)

Equation (4) ensures that two intervals do not overlap, but need to be linearized.

We start first by linearizing the inequality $f1 \leq s2$ as follows :

$$\begin{cases} f - \mathcal{M}x_1 - \mathbf{s}' \le 0\\ f + \mathbf{M} - \mathcal{M}x_1 - \mathbf{s}' \ge 0 \end{cases}$$
(5)

Where M is a very big number and x_1 is a binary variable that the solver sets to 1 if $f \le s'$.

Similarly, $f' \leq s$ is linearized as follows:

$$\begin{cases} f' - \mathcal{M}x_1 - \mathbf{s} \le 0\\ f' + \mathbf{M} - \mathcal{M}x_1 - \mathbf{s} \ge 0 \end{cases}$$
(6)

As an interval can not be on the left and on the right at the same time, we enforce that only one situation is selected by :

$$x_1 + x_2 = 1 \tag{7}$$

Now that we presented how two intervals can be enforced to not overlap. We describe now how overlapping constraints are generated. As described earlier, two types of overlapping must be prohibited : (i) those on the same core, and (ii) those of the same job.

For the overlapping intervals of the same core, the constraints in Equation (5), (6), (7) must be generated of every couple of intervals allocated to the same core having the same index of processor (index m in the variables name) as in the following equation :

 $\forall k,$

$$\forall i, \forall i', \forall j, \forall j', \forall m, \forall m', \forall l, \forall l'$$

$$[\mathbf{s}_{i,j,k,l,m}, \mathbf{f}_{i,j,k,l,m}] \cap [\mathbf{s}_{i,j,k,l,m}, \mathbf{f}_{i,j,k,l',m'}] = \emptyset$$
(8)

For the overlapping intervals of the same job, the constraints in Equation (5), (6), (7) must be generated for every couple of intervals of the job, i.e. having the same task, sub-task and job index (i.e. the same i, j, k in the variables name) as in the following equation :

$$\forall i, \forall j, \forall k, \forall m', \forall m, \forall l, \forall l', [\mathsf{s}_{i,j,k,l,m}, \mathsf{f}_{i,j,k,l,m}] \cap [\mathsf{s}_{i,j,k,l,m}, \mathsf{f}_{i,j,k,l',m'}] = \emptyset$$
(9)

The core overlapping intervals constraints must be generated only when considering the global approach. Indeed, in the partitioned approach the same task will be always allocated on the same core, therefore the job overlapping constraints are sufficient as tasks are forced to be allocated to the same core, therefore can not have non-empty intervals in the more than one core as it will be shown in the next section.

F. Partitioning constraints

At design time, one may allocate a sub-task to a particular core. To enforce sub-task allocation without modifying the design of the ILP, we ensure that only the intervals of the subtask on the allocation core can have positive lengths, while the length of all intervals on the other cores have a length equal to zero.

Therefore, for all intervals of a given sub-task $v_{i,j}$ on a core k, we define an allocation variable $a_{i,j,m}$. $a_{i,j,m}$ is equal to 1, if the interval length is strictly greater than zero, i.e:

$$a_{i,j,m} = \begin{cases} 1, & \text{if} \exists k, l, m \text{ such } \mathsf{f}_{i,j,k,l,m} > \mathsf{s}_{i,j,k,l,m} \\ 0 & \text{Otherwise} \end{cases}$$
(10)

Equation (10) is linearized as follows :

$$\mathsf{f}_{i,j,k,l,m} - M \cdot a_{i,j,m} - \mathsf{s}_{i,j,k,l,m} \le 0 \tag{11}$$

$$f_{i,j,k,l,m} + (1 - a_{i,j,m})M - s_{i,j,k,l,m} \ge 0$$
(12)

Please notice that the same variable $a_{i,j,m}$ is defined for all intervals of the same sub-task and on the same core, therefore the same variable $a_{i,j,m}$ is used for all intervals having the processor index (i.e. k).

Further, we enforce that only a single variable is set equal to one :

$$\forall i, j, m \sum a_{i,j,l,m} = 1;$$

G. Handling alternative nodes

IV. ACCELERATING RESOLUTION

References

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