Bidirectional DC-DC Converter Topologies for Low-Voltage Battery Interface: Comparative Assessment

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***Abstract*—The growing interest towards efficient and reliable bidirectional DC-DC converter topologies for interfacing low-voltage (LV) batteries, eg. *48 V*, with a high-voltage (HV) DC-link, eg. *400 V*, has driven the research toward the investigation of many different topologies. In this paper, three isolated and bidirectional topologies have been selected and compared to each other, where these topologies are seen as the state-of-the-art topologies for battery-fed systems. The introduced comparison includes the number of used semiconductor devices and passive elements, the rated voltage and current of the different semiconductor devices, the forecasted switching and conduction losses using PLECS, and the estimated volume and power losses of the employed magnetic elements. Furthermore, the comparison includes simulation results using PLECS considering a *1.5 kW* power level.**

***Index Terms*—Battery, bidirectional, boost converter, current-fed, dual-active bridge (DAB), energy storage, isolated, microgrids, push-pull converter.**

I. Introduction

The widespread deployment of energy storage systems (ESSs) is a consequence of the high penetration of the different renewable energy sources and the existence of many critical loads as well [1], [2]. Moreover, the present and future trends towards the electric vehicles is increasing the interest in these different ESSs [3]. Consequently, many research activities have been conducted in order to achieve robust and efficient operation of these ESSs from many perspectives, such as the technology of the employed energy storage element itself and the used power conditioning stage (PCS), i.e. the utilized interfacing layer between the energy storage element and the load [4], [5].

Depending on the type of the employed energy storage element and the load nature as well, many different power converter topologies can be utilized in order to ensure the desired optimum and robust operation [6]. For battery-fed systems, which is the main scope of this paper, bidirectional and isolated operations are mandatory to be guaranteed by the employed PCS. In addition to that, it is of paramount importance to ensure a continuous current with minimal current ripple at the battery side.

One of the typical and commonly used battery-fed power systems, is interfacing the low-voltage (LV), e.g. *48 V*, batteries with the high-voltage (HV), e.g. *400 V*, DC-link bus that is typically used in DC microgrids. For such typical system, many structures with different characteristics have been studied in literature [6]–[11]. Among them, this paper considers three different bidirectional and isolated DC-DC converters, where these topologies are seen as the state-of-the-art for battery-fed power systems. The first topology, which is commonly used, is the dual-active bridge (DAB) topology, whose circuit diagram is shown in Fig. 1a with an LC filter at the battery side in order to ensure a continuous input current [12], [13]. Meanwhile, the other two topologies are current-fed ones without any additional LC filter, where one of them is the isolated boost with coupled-inductor (IBCI) topology shown in Fig. 1b [14], [15], while the other one is the current-fed push-pull converter (IPPC) topology shown in Fig. 1c [16], [17].

The rest of this paper is organized as follows: Section II reviews the basic operation and modulation of the considered state-of-the-art topologies shown in Fig. 1. Then, a $1.5\ kW$ battery-fed system is designed using each of these topologies, and then simulated in Section III. Starting from the introduced simulation results in Section III, a comparative assessment is introduced in Section IV, where this comparison includes the number of used semiconductor devices and passive elements, the rated voltage and current of the different semiconductor devices, the forecasted switching and conduction losses using PLECS, and the estimated core volume and power losses of the employed magnetic elements. Finally, conclusions are reported in Section V.

II. Review of the Basic Operation and Modulation

The basic principle of operation behind those state-of-the-art topologies, shown in Fig. 1, can be simplified using the model shown in Fig. 2. This basic operation implies the control of the transferred energy between two stiff voltage sources through the leakage inductance of the employed magnetic element as depicted in Fig. 2. This can be done by controlling the phase shift between the two sources and/or the amplitude of the fundamental component [12], [14]. This is depicted in Fig. 3, in which the basic phase shift modulation (PSM) is shown

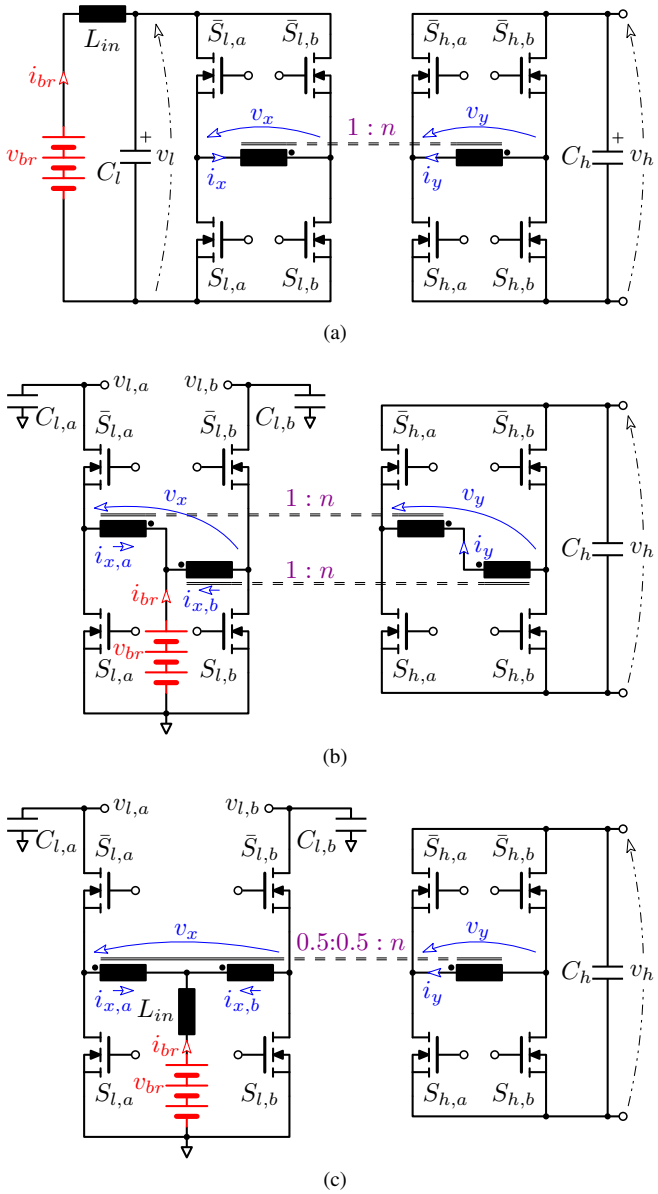

Fig. 1. State-of-the-art bidirectional and isolated DC-DC converter topologies for battery-fed power systems. (a) Dual-Active Bridge (DAB) with an LC filter at the battery side; (b) isolated boost with coupled-inductor (IBCI); and (c) current-fed push-pull converter (IPPC). Note that v_{br} is the low-voltage (LV) battery voltage (eg. 48 V) and v_h is the high-voltage (HV) DC-link voltage (eg. 400 V).

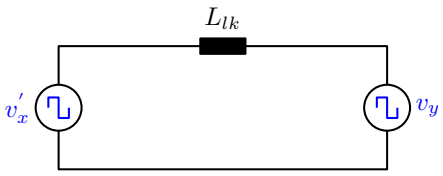

Fig. 2. Simplified model of the state-of-the-art topologies shown in Fig. 1. Note that $v_x' = n \cdot v_x$ and L_{lk} is the magnetic element leakage inductance referred to the high-voltage (HV) DC-link side.

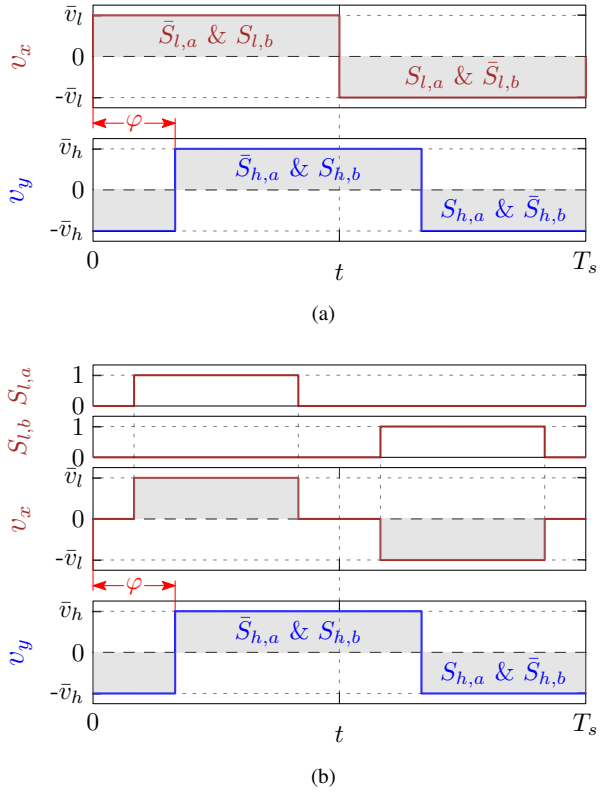

Fig. 3. Modulation schemes of the state-of-the-art-topologies. (a) Phase shift modulation (PSM); (b) Pulse width plus phase shift modulation (PW-PSM). Note that T_s is the switching period.

in Fig. 3a [12], [13], while the pulse width plus phase shift modulation (PW-PSM) is depicted in Fig. 3b. Using the PSM shown in Fig. 3a, a 50% duty ratio square wave voltage is generated from each bridge and the phase shift (φ) between those two voltages controls the power flow. Meanwhile, under the PW-PSM, a three-level voltage can be generated from any of the two bridges, i.e. any of v_x and/or v_y can be a three-level voltage. This is clarified in Fig. 3b considering only a three-level voltage at the battery side, which is the common implementation. This modulation strategy, when adopted for the two current-fed topologies here considered, allows to control the clamp capacitor average voltages $\bar{v}_{l,a}$ and $\bar{v}_{l,b}$, i.e the amplitude of voltage v_x, thus compensating for the battery voltage variation.

Fig. 1a shows the circuit diagram of the DAB, in which two B4-bridges are utilized in addition to a high frequency transformer. Moreover, an LC filter is employed at the LV battery side in order to ensure a continuous battery current with a certain peak-to-peak current ripple.

On the other hand, the IBCI comprises two isolated boost converters with two coupled-inductors, whose secondaries are series connected to a B4-bridge as shown in Fig. 1b.

Finally, the IPPC, whose circuit is depicted in Fig. 1c, can be seen as a combination between the DAB and the IBCI, where a high frequency transformer is used similar to the DAB, while the structure of the low-voltage side bridge is similar to the IBCI using two series connected primaries of the employed

TABLE I
PARAMETERS OF THE 1.5 kW BATTERY-FED SYSTEM USING THE DIFFERENT TOPOLOGIES

Configuration	DAB Fig. 1a	IBCI Fig. 1b	IPPC Fig. 1c
v_{br} (V)	$48^{(i)}$		
v_h (V)	$400^{(i)}$		
f_s (kHz)	60		
L_{lk} $(\mu H)^{(ii)}$	160		
n	8	4	4
L_{in} (μH)	3.5	/	3.5
L_m $(\mu H)^{(iii)}$	/	$30^{(iv)}$	/
C_l (μF)	27.2	$C_{l,a} = 6.8$ $C_{l,b} = 6.8$	$C_{l,a} = 6.8$ $C_{l,b} = 6.8$
C_h (μF)	5		

$^{(i)}$ average nominal value
$^{(ii)}$ referred to the secondary side, i.e. to v_y
$^{(iii)}$ referred to the primary side, i.e. to v_x
$^{(iv)}$ assuming $\pm 3\%$ of mismatch in the simulation

transformer. In addition to that, an inductor (L_{in}) is used at the battery side in order to smooth the input current and manage the voltage ripple across the LV capacitors. Note that L_{in} is the same as the DAB in terms of the sizing.

III. 1.5 kW BATTERY-FED SYSTEM: SIMULATION RESULTS

In order to figure out the basic differences among the three topologies shown in Fig. 1, a 1.5 kW battery-fed system is designed using each of these topologies, where the parameters of this system are listed in Table I. Since only one operating point is considered for this comparison, which is the nominal one, the PSM shown in Fig. 3a is used for all the three topologies. In this case, the turns ratio (n) has been selected for each topology in order to match the amplitudes of the voltages applied to the leakage inductance at nominal conditions, i.e. $\bar{v}_h \approx n\bar{v}_l$.

It is worth to note the following aspects are considered for the designed 1.5 kW battery-fed system:

- since the battery current ripple, for an ideal IBCI topology, is equal to zero under the PSM, a $\pm 3\%$ of mismatch in L_m for each coupled-inductor is assumed;
- the input inductor L_{in} is designed in order to limit the battery peak-to-peak current ripple to be less than 3% of the average current value at full-load;
- the value of the filter capacitor C_l is increased in the DAB in order to maintain the same percentage of voltage ripple of the IBCI and the IPPC.

This system is simulated using PLECS and the obtained simulation results are shown in Fig. 4. In this figure, the differential voltages of the LV and the HV sides (v_x and v_y respectively), the LV dc-link voltage (v_l), the HV dc-link voltage (v_h), the battery current (i_{br}), the ac current at the LV and the HV sides (i_x and i_y respectively), the current of phase a upper and lower switches for the LV side ($i_{\bar{S}_{l,a}}$ and $i_{S_{l,a}}$ respectively), and the current of phase a upper and lower switches for the HV side ($i_{\bar{S}_{h,a}}$ and $i_{S_{h,a}}$ respectively) are shown for each topology. Over and above that, for each switch current waveform, the peak value ($\hat{i}$) and the RMS value (I) are mentioned.

These simulation results reveal the following aspects:

- $\bar{v}_l$ in the IBCI and the IPPC is twice the DAB case (with a 50% duty cycle, the step-up gain of these topologies is equal to 2);
- the peak-to-peak value of i_x in the DAB is twice the IBCI and the IPPC;
- the DC flux inside the IPPC transformer equals zero ideally as the resultant DC flux components from the two primaries, i.e. from $i_{x,a}$ and $i_{x,b}$, cancels each other inside the core;
- for the IBCI and the IPPC, the current stresses of the lower switches at the LV battery side is much higher than the upper switches due to the DC current component;
- the thermal stresses of each pair of switches in the LV battery side is the same for the DAB, unlike the IBCI and the IPPC.

IV. COMPARATIVE STUDY

A. Semiconductor Devices

1) Numbers of Devices: Comparing among the three topologies, it can be seen that the same number of semiconductor devices is utilized in each topology.

2) Voltage and Current Ratings: From the simulation results shown in Fig. 4, it can be seen that the current and voltage stresses of the HV side switches are the same for the three topologies. Meanwhile, for the LV side switches, these stresses are the same for the IBCI and the IPPC topologies, while the DAB is completely different from them. It can be seen that the DAB has lower voltage stresses for the LV side switches compared to the IBCI and the IPPC topologies, but with higher current stresses. This is summarized in Fig. 5a, in which a normalized comparison between the three topologies in terms of the peak switch voltage and current, and RMS current is introduced.

3) Switching and Conduction Losses: For the sake of examining the switching and conduction losses in each topology, a PLECS model has been used in order to calculate these losses. Fig. 5b shows the normalized comparison between the three topologies in terms of the calculated switching and conduction losses at full-load of the LV and the HV sides switches. From this figure, it can be seen that the HV side has the same losses in the three topologies, and minor differences exist for the LV side total losses in the three topologies, but with the DAB showing reduced losses. Moreover, Fig. 6a reports the distribution of these losses among the different switches at full-load, from which it can be seen that the thermal stresses of each pair of switches at the LV side is not equal for the IBCI and the IPPC, unlike the DAB. Finally, the variation of these losses considering different load points is depicted in Fig. 6b.

It is worth to note that the used switch models are as follows: for the HV side switches in the three topologies,

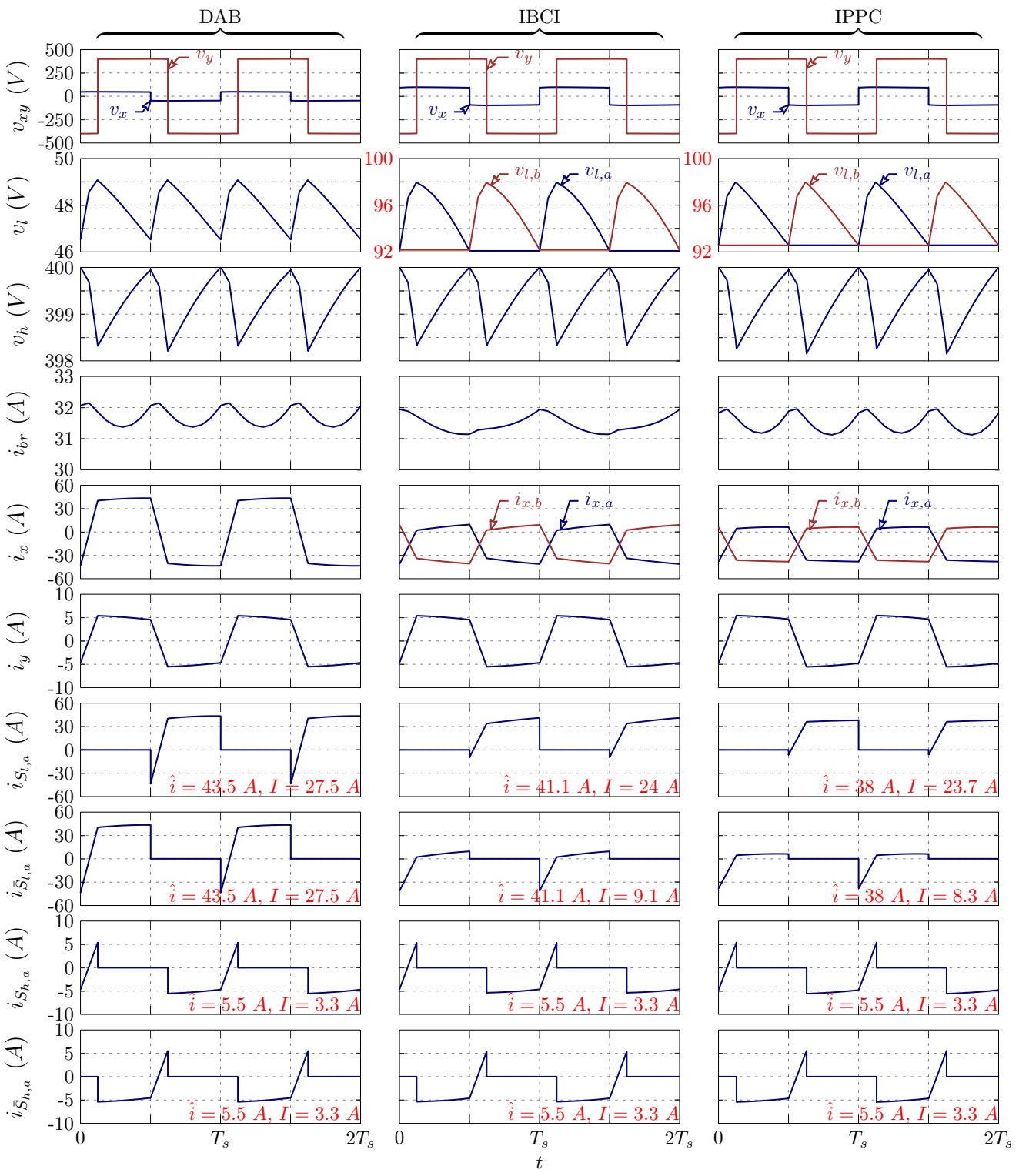

Fig. 4. Obtained simulation results for the three different topologies using PLECS at full-load condition. For each topology, the differential voltages of the LV and the HV sides (v_x and v_y respectively), the LV dc-link voltage (v_l), the HV dc-link voltage (v_h), the battery current (i_{br}), the ac current at the LV and the HV sides (i_x and i_y respectively), the current of phase a upper and lower switches for the LV side ($i_{\bar{S}_{l,a}}$ and $i_{S_{l,a}}$ respectively), and the current of phase a upper and lower switches for the HV side ($i_{\bar{S}_{h,a}}$ and $i_{S_{h,a}}$ respectively) are shown from top to bottom. Note that for each switch current waveform, the peak value ($\hat{i}$) and the RMS value (I) are mentioned, and T_s is the switching period.

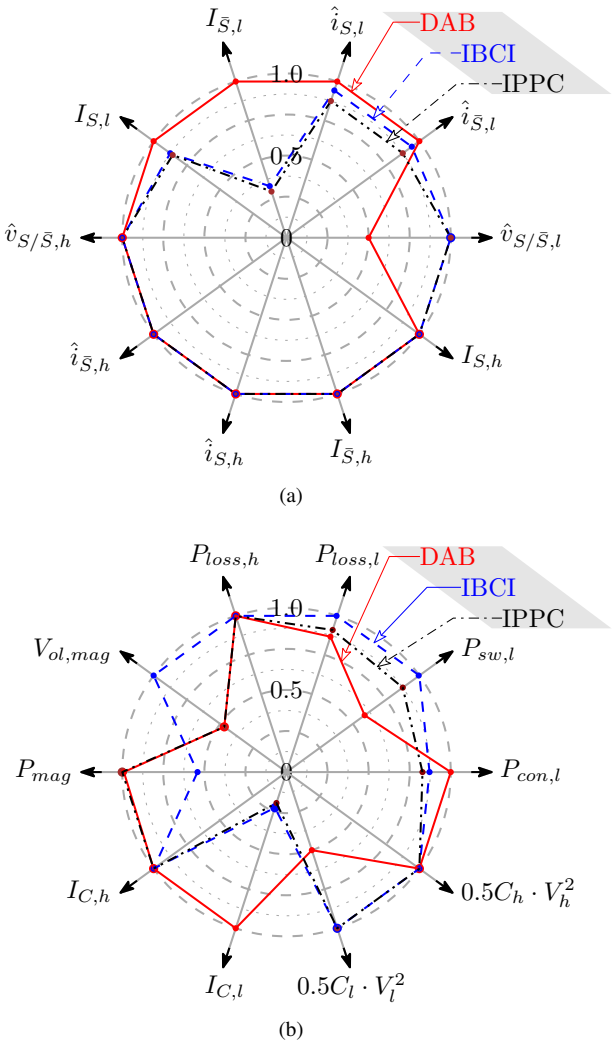

Fig. 5. Normalized comparison among the three different topologies. (a) Voltages and currents of the different switches, where $\hat{v}_{S/\bar{S},l}$ and $\hat{v}_{S/\bar{S},h}$ are the rated voltages of the LV and HV sides respectively, $\hat{i}_{\bar{S},l}$ and $\hat{i}_{S,l}$ are the peak currents of the upper and the lower switches at the LV side respectively, $I_{\bar{S},l}$ and $I_{S,l}$ are the RMS currents of the upper and the lower switches at the LV side respectively, $\hat{i}_{\bar{S},h}$ and $\hat{i}_{S,h}$ are the peak currents of the upper and the lower switches at the HV side respectively, and $I_{\bar{S},h}$ and $I_{S,h}$ are the RMS currents of the upper and the lower switches at the HV side respectively; (b) switching and conduction losses, magnetic volume and power losses, and RMS current and stored energy in the capacitors, where $P_{con,l}$, $P_{sw,l}$, and $P_{loss,l}$ are the LV bridge conduction, switching, and total losses respectively, $P_{loss,h}$ is the HV bridge total losses, $V_{ol,mag}$ is the forecasted volume of the magnetic elements cores, P_{mag} is the forecasted power losses of the magnetic elements, $I_{C,h}$ and $I_{C,l}$ are the RMS currents of the HV and LV side capacitors respectively, and $0.5C_l \cdot V_l^2$ and $0.5C_h \cdot V_h^2$ are stored energy at the LV and HV capacitors respectively.

an FCP110N65F MOSFET is used, while for the LV side switches an FDP075N15A MOSFET is used in the IBCI and the IPPC, and an FDP053N08B MOSFET is used in the DAB. Then, following the procedure in [18], the switching energies have been calculated for each switch and used in PLECS in order to calculate the switching and conduction losses for each topology.

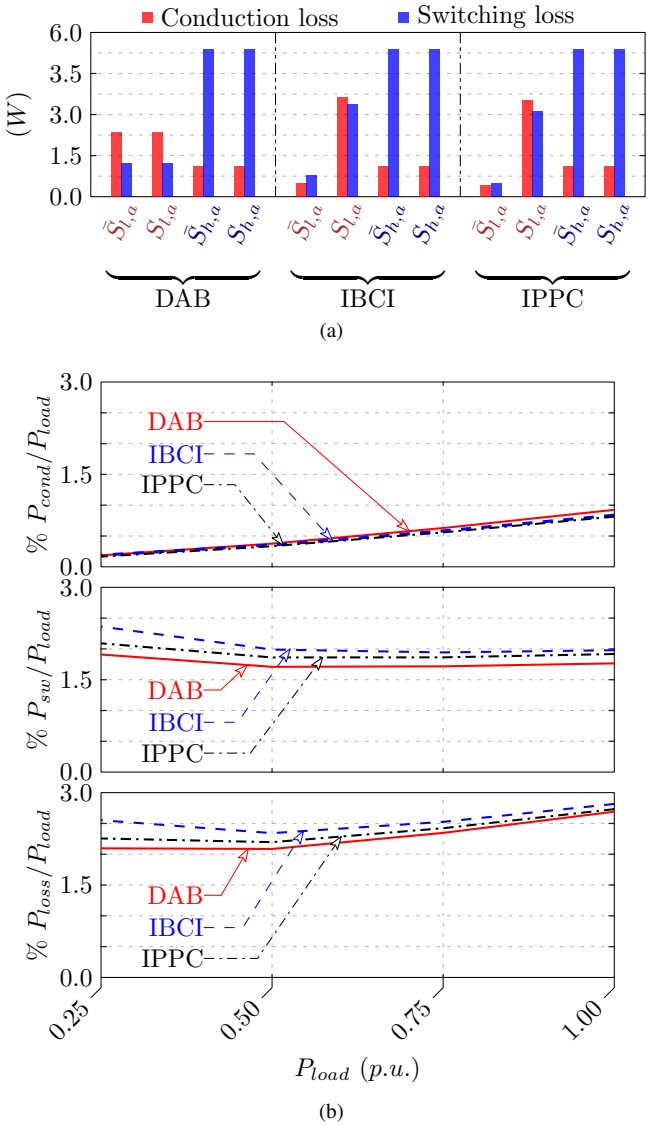

Fig. 6. Calculated switching and conduction losses using PLECS for the different topologies. (a) Losses distribution of phase a upper and lower switches at the LV and HV sides at full-load condition, where $\bar{S}$ represents the upper switch, while S represents the lower switch as depicted in Fig. 1; (b) losses variation considering different load points, where P_{cond}, P_{sw}, P_{loss}, and P_{load} are the conduction losses, the switching losses, the total losses, and the load power respectively.

B. Passive Elements

1) Number of Magnetic Elements: From Fig. 1, it can be seen that the three topologies are utilizing the same number of magnetic elements, where a transformer and a filter inductor are used with the DAB and the IPPC, while two coupled-inductors are used with the IBCI.

2) Volume and Power Losses of Magnetics: Although the three topologies are utilizing the same number of magnetic elements, the forecasted volume and power losses are different (see Fig. 5b). From this figure, it can be seen that the IBCI gives higher volume with lower power losses compared to the DAB and the IPPC. It is worth to note that this is dependent on

the design procedure, i.e. the volume of the magnetic elements in the DAB can be enlarged and less power losses can be obtained considering reduced peak flux.

Note that the design procedure introduced in [19] has been used to design the different magnetic elements in these topologies and the same core shape and material has been considered.

3) Capacitors RMS Current: The RMS current of the different capacitors can be concluded from the switches current in Fig. 4. It can be seen that the RMS current of the HV side capacitor, i.e. C_h, is the same for the three topologies. Meanwhile, the RMS current of the LV side capacitor, i.e. C_l, is much higher for the DAB, which is around four times the IBCI and the IPPC topologies as shown in Fig. 5b.

4) Capacitors Volume: The volume of the employed capacitors is proportional to the stored energy, i.e. $(0.5C \cdot V^2)$. Hence, Fig. 5b shows the normalized value of $(0.5C_l \cdot V_l^2)$ and $(0.5C_h \cdot V_h^2)$ for the LV and the HV sides capacitors respectively. From this figure, it is obvious that the three topologies have the same capacitor volume at the HV side, but the DAB is utilizing smaller volume at the LV side due to the higher effective switching frequency of the employed capacitors.

V. Conclusion

In conclusion, this paper has introduced a comparative assessment among three isolated and bidirectional DC-DC converters for battery interface. These topologies are the dual-active bridge (DAB), the isolated boost with coupled-inductor (IBCI), and the current-fed push-pull converter (IPPC). The comparison among these topologies shows that the DAB has several merits, like:

- smaller switch voltage stresses at the LV side;
- smaller volume of magnetics, which is similar to the IPPC;
- equal thermal stresses of each pair of switches;
- smaller volume of the required capacitance.

Meanwhile, the DAB suffers the following demerits:

- higher power losses in the magnetic elements, which is similar to the IPPC, compared to the IBCI. These power losses can be reduced by increasing the volume of the employed cores and designing for lower peak flux;
- higher RMS current of the LV side capacitor.

On the other hand the IBCI benefits from the possibility of controlling the amplitude of LV side differential voltage (v_x) in order to match the HV side differential voltage (v_y) considering a wide range of battery voltage. Finally, the IPPC is similar to the IBCI from many perspectives except the volume and power losses of the employed magnetic elements.

Acknowledgement

This project has received funding from the Electronic Components and Systems for European Leadership Joint Undertaking under grant agreement No 737434. This Joint Undertaking receives support from the European Unions Horizon 2020 research and innovation program and Germany, Slovakia, Netherlands, Spain, Italy.

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