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Prototyping and Measurements for a LiFi System

Kun Chen Hu[1], Ana García Armada[1], Matilde Sánchez-Fernández[1] and Antonio Royo[2]
[1]Department of Signal Theory and Comunications, Universidad Carlos III de Madrid (Spain)
[2]UVAX Concepts S.L., Parque Empresarial Tactica, Paterna Valencia, (Spain)
Email: kchen@tsc.uc3m.es - agarcia@tsc.uc3m.es - mati@tsc.uc3m.es - a.royo@uvax-concepts.com

***Abstract*—We are witnessing a revolution in wireless technology where Light Fidelity (LiFi) emerges as one potential candidate. In this paper we present a LiFi prototype that allows us to verify the feasibility of deploying this technology. The prototype is based on two Spartan 6 FPGAs and uses a Light Emitting Diode (LED) to transport the information through amplitude changes of the light. The receiver uses a low dark current PIN photodiode. We describe the system design, the receiver algorithms and the measurement set-up. We present some measurements where in a Line of Sight (LOS) channel the received pulses are shown to match the transmitted ones.**

I. Introduction

We are witnessing a revolution in wireless technology where the users are demanding an enormous increase of data rates in the range of $\times 1000$ [1]. The traditional radio spectrum is close to saturation, thus increasing the bandwidth available for a transmission will necessarily imply exploring new bands. In this demand scenario, there is a need to develop and explore new techniques that are able to cope with the user requirements.

Light Fidelity (LiFi) emerges as one of these new technologies. It transports the information through modulation of the light emitted by a LED, whose response time imposes a bandwidth limitation to the all system. An interesting use case of LiFi appears with its combination with the Power Line Communication (PLC) technology, where the latter may be used as a distributing network and LiFi provides the wireless access to the users [2].

The term of LiFi was coined firstly by Edinburgh University's Prof. Harald Haas in 2001 [3]. Many experts claim that LiFi represents the future of mobile internet thanks to its reduced cost and greater efficiency becoming an alternative to WiFi as the basic technology for Internet of Things (IoT).

The aim of our project is to show the feasibility of a LiFi prototype and, to showcase its potential application in an outdoor scenario through street lights reaching 10Mbps. In a previous paper [4], we showed some simulation results and a preliminary design of a LiFi prototype. Here we detail the first empirical design and some measurements that allow us to verify the feasibility of deploying such a system.

The rest of the paper is organized as follows: section II consists of an overview of the system model and the chosen electronic devices, in section III we show the prototype implementation and the measurement set-up, section IV provides some measurements results and finally in section V some conclusions are pointed out.

II. Overview of the Prototype

Our main objective is to build a prototype so as to measure the channel and existing interference and provide a proof of concept of a LiFi system. To achieve this goal, we will be using two Spartan 6 FPGAs by Xilinx, as shown in Fig. 1, to set the basic architecture and model all required signal processing blocks to carry out the experiments.

Fig. 1. Basic architecture

A. Transmitter hardware design

The transmitter side is built using a Spartan-6 XC6SLX16 in CS324 package with two additional conditioning circuits, see Fig.2, the left one only has a single LED and the right one has six LEDs. Both of them converts the voltage pulses into current, and this is in turn converted into light variations.

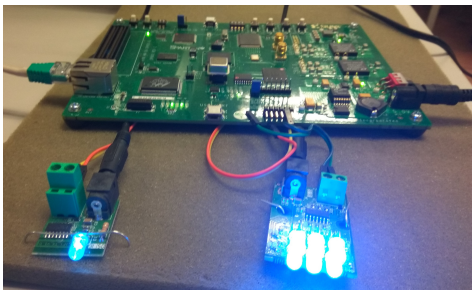


Fig. 2. Transmitter FPGA and conditioning circuit.

The conditioning circuits is basically formed by some LEDs and an hex inverter buffer/driver, see Fig.3, which has the feature of high-voltage open-collector outputs to interface with high-level circuits or for driving high-current loads. We are aware of there is not any element which can synchronize the transmission of the six LEDs. However, the average propagation delay time of chosen hex inverted is only 8ns. Surely it will not the responsible for any deformation caused at the received pulses.

Our idea of developing two conditioning boards is to characterize the attenuation of channel having two transmission

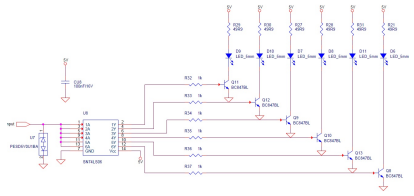


Fig. 3. Schemattic of the transmitter conditioning circuit

powers. Assuming that we are in short distance and using the free space equation of Friis, we can obtain that:

$$\frac{P_{R1}}{P_{R2}} = \frac{P_{T1} \cdot d_2^2}{P_{T2} \cdot d_1^2}, \tag{1}$$

where P_{Ti} and P_{Ri} are the transmitted and received power of each circuit in a distance d_i.

If we have the same receptor circuit, so its sensitivity is the same for any emitter, the previous (1) is equal to 1. Thus the relation of the two distances is:

$$\frac{d_1^2}{d_2^2} = \frac{P_{T1}}{P_{T2}} = \frac{V_{T1}^2}{V_{T2}^2} \rightarrow \frac{d_1}{d_2} = \frac{V_{T1}}{V_{T2}} = \frac{N_1}{N_2} = \frac{1}{6}, \tag{2}$$

where V_{Ti} is the voltage at transmitter and N_i is the number of LEDs. Hence, the relation of the distance is just the relation of LEDs number at the transmitter.

B. Receiver hardware design

The receiver side is built using a Spartan-6 XC6SLX45 in CS324 package with an additional conditioning circuit which converts the received light to two-level voltages, as shown in Fig. 4.

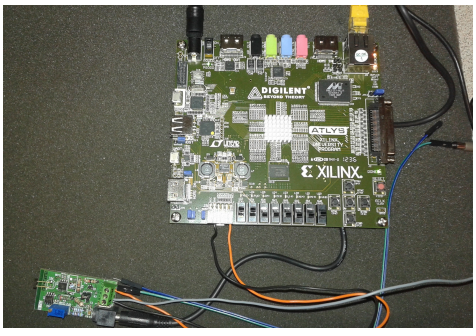


Fig. 4. Receiver FPGA and conditioning circuit

For the receiver conditioning circuit several electronic components have been chosen based on the following specific criteria:

- The main goal of this circuit is to convert the light variations to current. For that purpose we have chosen a photodiode that offers a low dark current, so no stray light can reach the photosensitive area from the side or back. This allows reliable optical measurements in the visible to near-infrared range.
- The circuit is also needed to convert the current to voltage using a low input bias current precision amplifier, which has internally a cancellation circuitry.
- The voltage is compared using another amplifier with an increased dynamic range and a high slew rate for higher speed applications. Furthermore, a low noise component is needed to be suitable for small-signal conditioning.
- Finally a bipolar transistor designed for switching applications is added. So the FPGA will receive digital pulses.

Additionally, we have set up an extra output which enables to measure the intermediate received signal after the comparator. This makes it possible to debug the system and detect any potential problem.

To analyse the operating frequency of the prototype, we have to look at several constraints. At the receiver, since the amplifier's slew rate (defined as the rate of change of the voltage per unit time) is $SR = 3.6$V/us, the maximum frequency is given by

$$f_{max} = \frac{SR}{2\pi V_0} = \frac{3.6}{2\pi 5} = 114.5kHz \tag{3}$$

where V_0 is the peak amplitude of the waveform with a value of 5V. However, we are going to work with a square wave signal which has many harmonics. Hence, we can not work at the maximum frequency, so we have decided to set the operational frequency to 25KHz.

III. Prototype Implementation and Measurement Set-up

The complete measurement system is shown in Fig. 8 and is described in the following.

A. Software development

At both ends of the system, there are two computers which send and receive standard Ethernet frames, so the prototype can be connected to any external network based on IP and Ethernet protocols.

For this purpose a program in C has been developed which generates raw Ethernet packets with random information and length at the transmitter.

At the receiver, we are sniffing all the received Ethernet frames using Wireshark for the purpose of measuring and benchmarking the system performance.

B. FPGA development

The main functions and basic architecture for transmission and reception are built in the FPGAs. The transmitter FPGA receives the Ethernet frames from the computer. After analysing each frame to check that is correct, it must process these bits according to the standard [5]. At the other end, the receiver FPGA processes the received pulses undoing all the operations made by the transmitter.

The architecture design is described in Fig. 8. As can be seen, both sides have an Ethernet block integrated to receive and transmit frames.

The transmitter processing consists on:

- Frame delimiter: its main duty is to count the number of bytes in the current frame. This size must be fulfilled in the frame header.

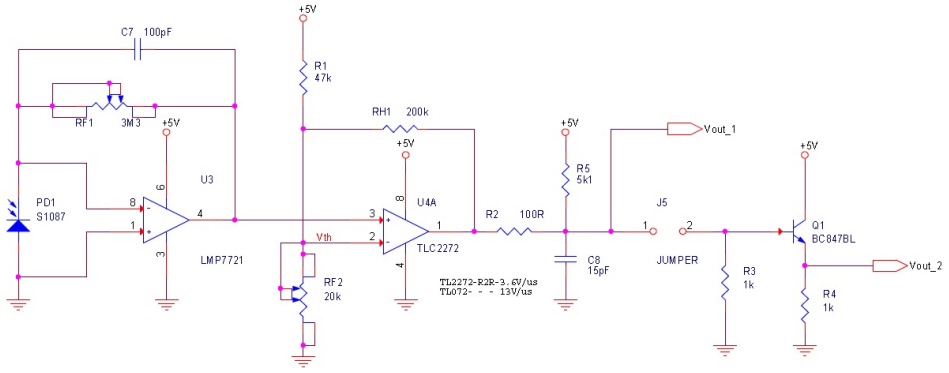


Fig. 5. Schematic of receiver conditioning circuit.

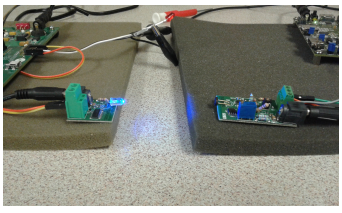


Fig. 6. Transmitter and receiver conditioning circuits

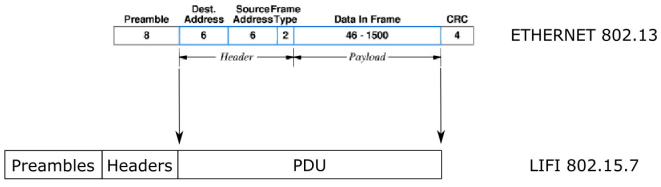


Fig. 7. Ethernet frames encapsulated into LiFi frames.

- Header builder: according to the standard it is mandatory to build the header with some important information, for example the frame length and CRC protection.
- Big Size FIFO: meanwhile the header is being computed, the whole frame is saved into a FIFO with the maximum Ethernet frame size.
- DSP Tx: once the header and payload are ready, they are processed according to the standard [5] to include a Manchester encoder.
- Packet FIFO: this special FIFO will hold the data until a complete frame is saved.
- Emitter: each bit is transmitted according to the transmission frequency which is fixed by the receiver.

The receiver processing consists on:

- Receiver: it samples the data according to the established operational frequency which is 25KHz.
- Synchronizer: as un any receiver, the first operation to be performed is finding the starting point of a frame.
- DSP Rx: undo all the operations performed in the transmitter, including a Manchester decoder.
- Header Extractor: extract valuable information from the header and deliver it to the synchronizer.

C. Synchronizer

A very important block at the receiver is the synchronizer. For a good compromise between complexity and performance, we have developed a full parallel correlator based on Hamming distance. There is a shift register which holds the last L bits. Those bits are compared to the original preamble sequence using an XOR operation. After that, the number of ones are counted using a high speed parallel counter. If this value is above a specific threshold it will be considered that it as a valid preamble, otherwise the synchronizer will continue with this operation. We have evaluated by simulation that the synchronizer operation lasts only 6 clock cycles, which will not impact to the system in terms of speed.

IV. Measurements

In this section we explain some measurements performed with the described prototype. With the actual hardware design, that is intended for a proof of concept, we are only able to successfully transmit when there is LOS between transmitter and receiver and the distance is very reduced, below 5.4cm with only a single LED and 34cm with six LEDs, which satisfy perfectly (2).

In Fig. 9a the continuous frames reception is shown at the intermediate output. The ambient light is imperceptible because of the chosen photodiode, so if we switch on or off the light, the received pulses will not be corrupted, as seen in Fig. 9b. The amplitude of the signal shown at the top is the FPGA output which is 2.5V and is used to drive the transmitter conditioning board. The bottom signal is the received signal at the debugging output which is 250mV. However if we inject a light interference using the flash of any mobile camera which not only adds a offset, but also saturates the receiver. To overcome the offset we need to implement a high pass filter using a simple RC circuit; and to solve the saturation problem we need to integrate an Automatic Gain Control (AGC).

If we measure one single pulse period we can verify its frequency, as seen in Fig. 10a. The measured value matches perfectly the theoretical one. In addition we show the measurement of the ambient noise which corresponds approximately to 7.5mV, giving approximately 30dB of Signal to Noise Ratio (SNR).

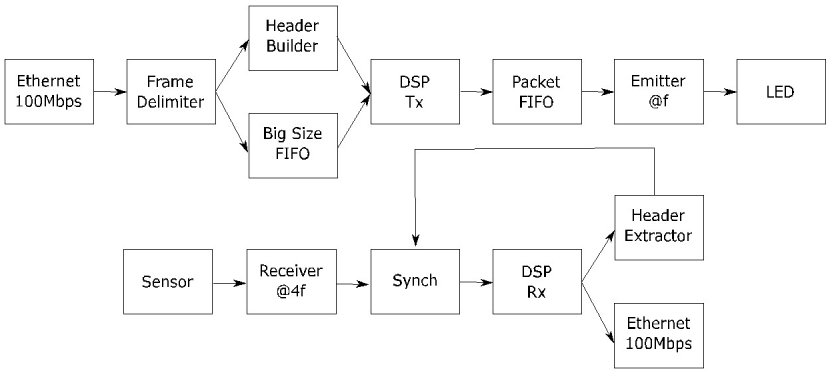
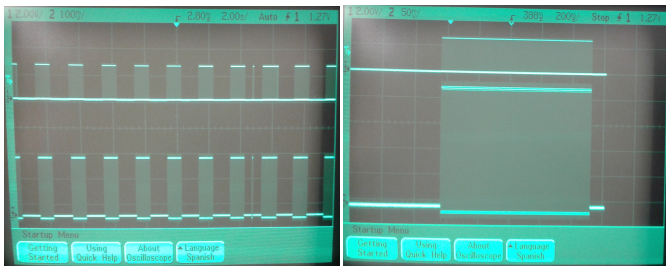
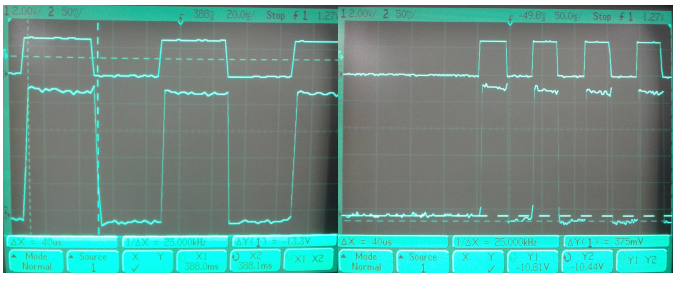


Fig. 8. Block Diagram



(a) Several frames (b) One frame

Fig. 9. Received frames



(a) Frequency (b) Noise

Fig. 10. Measurements

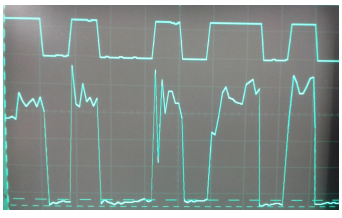


Fig. 11. Degraded pulses

If the transmitter and receiver boards are separated a longer distance, the signal will be degraded as seen in Fig. 11. This signal is now not strong enough to drive the bipolar transistor correctly, so the digital output signal will also be wrong and the synchronizer is not able to find the starting point. To improve this performance, a gain amplifier is being designed for the receiver.

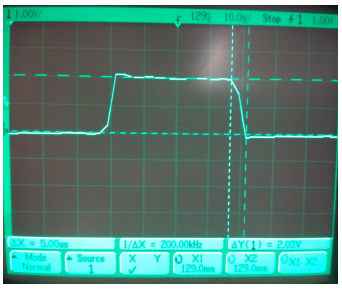


Fig. 12. Fall-time measure

Finally, we will measure the rise and fall time for both transmitter circuits. There not exists a fixed value for them, but the worst result is 5us for both times and both circuits, see Fig. 12. This result shows us that the six transmitter LEDs is quite well integrated, and the separation distance among them are insignificant compare with the link distance.

V. Conclusion

We have described a complete LiFi prototype that has been developed to evaluate the feasibility of this technology and our design decisions.

We have shown that the prototype works correctly and Ethernet frames are transmitted and received thorugh variations of the light emitted by a LED and received by a photodiode. However, there are several improvements that are needed and constitute our future work. In particular, we are working to integrate an amplifier and some error correction codes that will allow a better transmission range.

In conclusion, we have prototyped and tested a LiFi system showing the feasibility of this promising technology.

Acknowledgement

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REFERENCES

[1] Ericsson. (2016) Ericsson mobility report. [Online]. Available: http://www.ericsson.com/res/docs/2016/mobility-report/

[2] K. P. Pujapanda, "Lifi integrated to power-lines for smart illumination cum communication," in *Communication Systems and Network Technologies (CSNT), 2013 International Conference on*, April 2013, pp. 875–878.

[3] H. Haas. (2011) Wireless data from every bulb. [Online]. Available: https://www.ted.com/

[4] V. M. Baeza and M. Sánchez-Fernández and A. G. Armada and A. Royo, "Testbed for a lifi system integrated in streetlights," in *Networks and Communications (EuCNC), 2015 European Conference on*, June 2015, pp. 517–521.

[5] "IEEE Standard for Local and Metropolitan Area Networks–Part 15.7: Short-Range Wireless Optical Communication Using Visible Light," *IEEE Std 802.15.7-2011*, pp. 1–309, Sept 2011.