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***Abstract*—Hardware redundancy techniques are routinely used for mitigation purposes in radiation-hardened integrated circuits. Duplication indeed has been proved effective to harden the well known DICE memory cell against SEUs. In this work, we nonetheless report, on simulation basis, the possibility of a dynamic fault mechanism that may turn an SET into an error. We also introduce and validate a countermeasure that alleviates this weakness.**

***Index Terms*—Radiation hardening, DICE memory cell, dynamic fault model, SEE**

I. Introduction

Electronic devices are continuously improved in order to reduce their dimensions [1] and still become more robust to failures [2]. Among the different causes of failures to which an electronic device is subject, there are environment perturbations (e.g. by intense solar activity) [3] and human-induced perturbations (e.g. laser attacks aimed at acquiring sensitive information) [4]. The study of the different effects to which these devices are exposed is important to maintain their proper functioning when operating in extreme environments or under malicious attacks.

Considering space applications, the robustness of electronic devices in the face of ionizing radiation is of great importance. It can cause damage to collected data, operational problems in the systems, and premature wear of electronic components. This study focuses on Single Event Effects (SEE), which are random in nature and can be caused by a single ionizing particle with enough energy to induce disturbances or even a permanent failure in electronic systems [5]. This type of effect can be classified a s d estructive o r t ransient, t he latter being the focus of this study.

There are different approaches to mitigate or counter such effects on electronic devices and systems, including the use of new materials and manufacturing processes [6], new MOSFET layouts [7] and through the design of circuit-level hardening techniques that detect and prevent certain types of failures [8].

Within this context, this study was carried out in order to evaluate the functioning of a SEU (Single Event Upset) hardened memory cell, to show the possibility of inducing failures in that same memory cell and to propose a countermeasure to detect and treat such failures. All data obtained and analyses presented were performed through parametric simulations of electronic devices and circuits, taking into account a simple approach based on transient pulses consistent with TCAD or multi-physics tools, allowing observing effects in standard or hardened cells [9].

This article is organized as follows. Section II addresses the effects of radiation in integrated circuits (IC), focusing on SEE, techniques for mitigating these effects, it also introduces the radiation-hardened Dual-Interlock-Storage-Cell (DICE). Section III presents the possibility of injecting a dynamic-fault in the DICE cell, showing through simulations that it is possible to prevent the writing of data in a memory cell of this type. Section IV proposes a countermeasure against such dynamic-faults, describing its operation and showing through results by simulation its effectiveness. The conclusions of this study are presented in section V.

II. Radiation hardening

A. Radiation-induced faults and mitigation techniques

1) Radiation-induced errors: When exposed to harsh and radioactive environments ICs may suffer from various types of radioactive effects. In this work, we do not consider the cumulative total ionizing dose effects induced by X or gamma rays, protons and electrons, that can cause IC malfunction mainly due to threshold shifts and increased leakage [10]. We rather focused on SEEs that are induced by ionizing particles passing through a device and that may induce transient errors [5].

As an ionizing particle passes through silicon, it creates electron-hole pairs along its track due to direct ionization by the incident particle itself or ionization by secondary particles created by nuclear reactions between the incident particle and the affected device [11]. These charge carriers may recombine without any noticeable effect on the circuit's activity. An exception exists when the charge carriers are induced in the vicinity of a transistors reverse biased PN junction (drain/bulk, source/bulk or Nwell/Psubstrate): a place where there exists a strong electric field [11]. As a consequence, the charge carriers drift in opposite directions and a current pulse is induced (it vanishes as the charges are exhausted). It may last a few

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hundreds of picoseconds and may have an amplitude as large as a few mA (depending on the amount of induced charges and on the dynamic of their collection) [5]. This charge carriers collection phenomenon can be decomposed in two successive parts [12]. At first, the depletion region (hence the electric field) is stretched along the particle track, the charges nearby are collected in a few picoseconds generating a peak current: a phenomenon called funneling [12]. In a second time, the remaining charges are collected in a longer phenomenon, called diffusion [12]. The current decreases slowly until all charges are collected. In turn, this current pulse creates a transient voltage pulse, which may induce an error if induced (1) directly in a memory cell (a SEU) or (2) in a logic gate and if it propagates until being captured by a downstream Flip-Flop (a Single Event Transient, SET).

2) Mitigation techniques: Since the first evidence of SEEs [3], the radiation effect community started studying and developing countermeasures. Several mitigation principles were introduced: Error Detection And Correction techniques (or EDAC, e.g. based on spatial or temporal redundancy), sensors monitoring the currents at the root cause of SEEs (e.g. the bulk current sensors introduced by [13]), cells hardening through architecture redesign [8], [14], or even the use of the Silicon On Insulator (SOI) technology as an alternative to the usual CMOS bulk [15].

Spatial or temporal redundancy techniques [16], [17] are often used to mitigate SEEs, they respectively consist in making several times the same logical operations with redundant hardware blocks or at different moments (using the same hardware). It relies on the assumption that only one set of operations would be erroneous due to the local and non-deterministic nature of SEEs, making it possible to detect errors (in the case of duplication) or even to correct them (using triplication with majority vote [17]).

In our research, we considered a SEU-hardened memory cell using a duplication technique, it is described hereafter.

B. The radiation-hardened Dual-Interlock-Storage-Cell

The DICE memory cell [14] achieves SEU hardening through duplication of the internal nodes storing its logical state. A usual 6T SRAM memory cell has two internal nodes which logical values, `01` or `10`, represent either a `1` state or a `0` state. The DICE memory cell, depicted in figure 1, has four internal nodes $Q1$, $Q11$, $Q2$, $Q22$ to store its logical value: either `1010` to represent the logical state `1`, or `0101` to represent state `0`. It has four CMOS inverters with an original connection of the transistor gates. It is designed to recover from a single radiation-induced logical inversion of any of its internal nodes (see subsection II-C for a simulation-based illustration of the mechanism at play). Access to the internal nodes for writing and reading operations takes place simultaneously through four access transistors (`M8`, `M9`, `M10`, `M11` in figure 1).

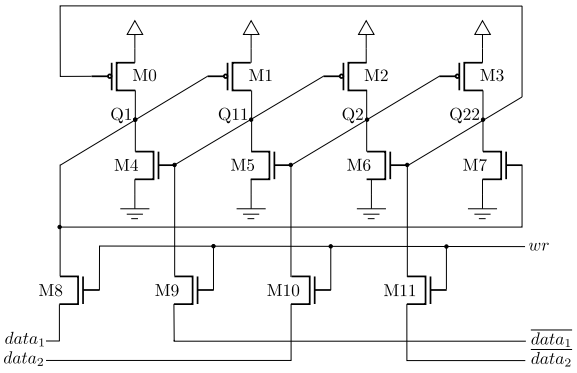

Fig. 1. Transistor-level view of the DICE cell.

C. Simulation of the DICE cell mitigating a SEU

In this subsection, we illustrate on simulation-based, the SEU mitigation mechanism of the DICE memory cell[1]. As a radiation-induced transient current is at the root cause of SEEs, we used a current source to model this phenomenon in our analog simulations. It outputs a tunable double exponential current transient based on the modeling works reported in [18], [19]. Orders of magnitude of amplitudes and temporal profiles used in electrical simulations are consistent with transient pulse issued from TCAD or multi-physics tools [9], [20]. The main parameters we considered were the current peak value (up to a few hundreds of μA) and the pulse duration (up to several hundreds of ps). Simulations were performed on circuits designed at the 65 nm CMOS technology node (VDD = 1.2 V). From the schematic of the DICE cell (and of the other gates used in our tests), we derived a layout and extracted its parasitic elements that we used in our simulations.

We considered an SEE arising when the DICE cell stores a `0` state ($Q1 = Q2 =$ `0` and $Q11 = Q22 =$ `1`). It consists in a transient current denoted I_{rad} in figure 2 (top red waveform). It was applied between the drain of transistor `M0` (a SEE-sensitive transistor in state `0`) and its bulk biasing contact to VDD. It starts at 2.6 ns in the simulation, at this time the DICE cell is in memory mode (i.e. its access transistors are in OFF state with their command signal `wr` at `0`). It has a peak amplitude of 200 μA, a rise time of 0.04 ns and a fall time of 0.38 ns. Figure 2 also displays the effect of the transient current on the cell's four internal nodes $Q1$, $Q11$, $Q2$, and $Q22$.

The main effect of the transient current is to drive $Q1$'s voltage from 0 V to 1.2 V. As a result, transistor `M1` is turned `OFF`, which puts node `Q11` into a high impedance state (HZ) because transistor `M5` is also `OFF`: the HZ state preserves $Q11$'s voltage that remains almost unchanged. $Q1$'s voltage modification also turns transistor `M7` `ON`; while `M3` is `ON`, a direct consequence is that the voltage of node $Q22$ goes approximately to VDD/2. As the transient current vanishes, $Q1$ returns to its original 0 V voltage (the change in $Q22$ voltage was not sufficient to prevent this through the command of

[1]Note that we did not consider any charge sharing effect between several sensitive areas in this work.

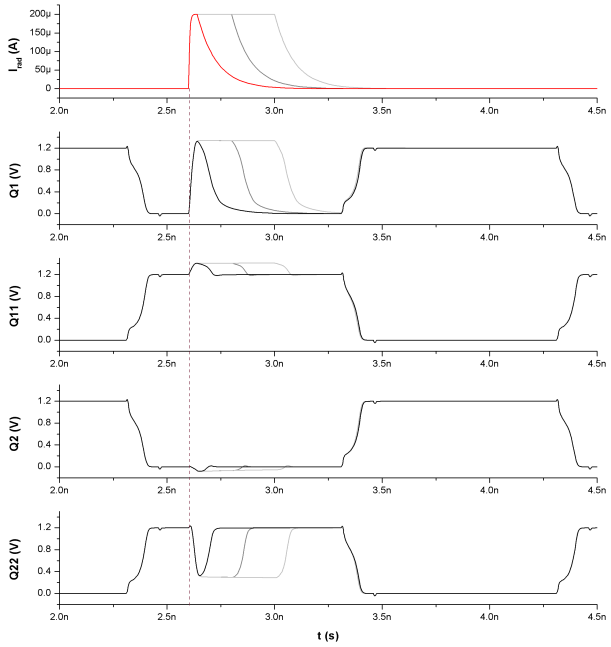

Fig. 2. Simulation of an electric current induced (I_{rad}) at node $Q1$ of the DICE cell.

transistor M0). Then, $Q22$ also returns to its initial voltage. The DICE cell was able to withstand the SEU thanks to the duplication of its internal nodes and to the preservation of its state on the duplicated nodes. For illustration purposes, we also ascertained the same SEU mitigation property when increasing the transient current duration to 0.17 ns and 0.37 ns (drawn in light gray in Fig. 2). These parameters are far beyond the threshold needed to induce a SEU in a 6T SRAM cell [21], [22] (note that these shapes of transient currents are no longer consistent with those induced by a SEE, however, it is an easy way to illustrate the mitigation properties of the DICE cell against an increase of the collected charge). Similar behaviors and the same SEU mitigation property are observed when the transient current is applied to the other nodes of the DICE cell (either in state 1 or 0).

This illustrates the strength of the DICE memory cell in mitigating SEUs in memory mode. However, its immunity to SEU may be put at risk during the writing phase as we explain in the next section.

III. Injection of a Dynamic Fault into a Radiation-Hardened Cell

The previous section acknowledges on simulation basis the (already known) ability of the DICE memory cell to withstand SEUs. However, if a single transient current is unable to induce a flip of the DICE's state, we wondered whether it may prevent a value to be written inside the DICE during the writing phase. Thus, inducing an error through a mechanism that shares similarities with a SET. It may happen if the logical state to be written is the complementary value of the DICE current state (e.g. while trying to write a 1 inside a DICE cell storing a 0).

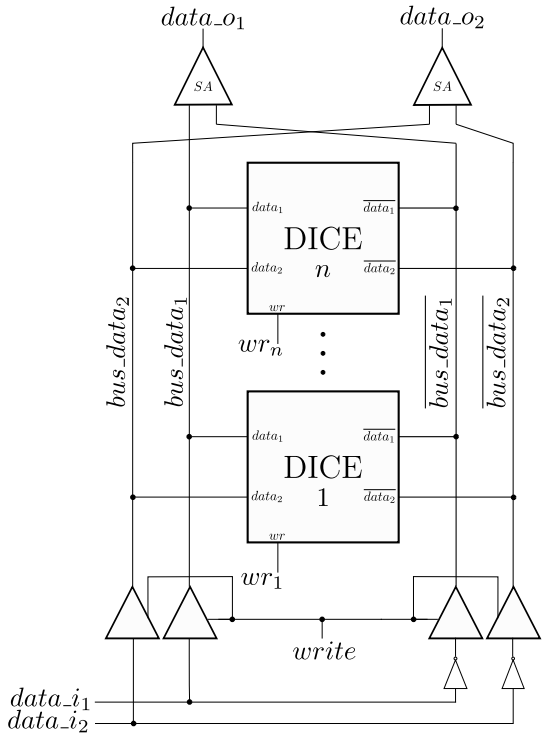

Fig. 3. DICE cell test bench for dynamic fault testing.

To explore further what we called a dynamic fault model, we considered what could be the architecture of a RAM memory using DICE cells as memory elements in a SEE-hardened IC.

A. DICE-based RAM memory

Figure 3 displays the test bench used in our simulations. It represents the architecture of one column of the RAM memory made of DICE memory cells (numbered from 1 to n).

The DICE cells are interconnected in parallel, so that each one can be accessed at a time for writing or reading through the activation of its wr signal. Substituting DICE to SRAM cells doubles the number of bit lines (a DICE cell has four inputs/outputs): denoted $bus\_data_{1,2}$ and $\overline{bus\_data_{1,2}}$. We considered a case study of a circuit using duplication as a radiation-hardening technique. Hence, the value to be written is duplicated in signals $data\_i_1$ and $data\_i_2$ which are fed to the bit lines through four buffers (and two inverters for inversion purposes) commanded by a $write$ signal. The $data\_o_1$ and $data\_o_2$ output signals are obtained thank to sense amplifier blocks connected to the bit lines (they are not considered in this study).

B. Simulation-based evidence of dynamic faults

Figure 4 displays the simulation results of a dynamic fault induced into a DICE cell preventing it from passing from a 0 to a 1 state.

The write phase involved the successive activation of two signals: $write$ and wr to propagate, respectively, the data to be written to the bit lines and then inside the DICE cell (they

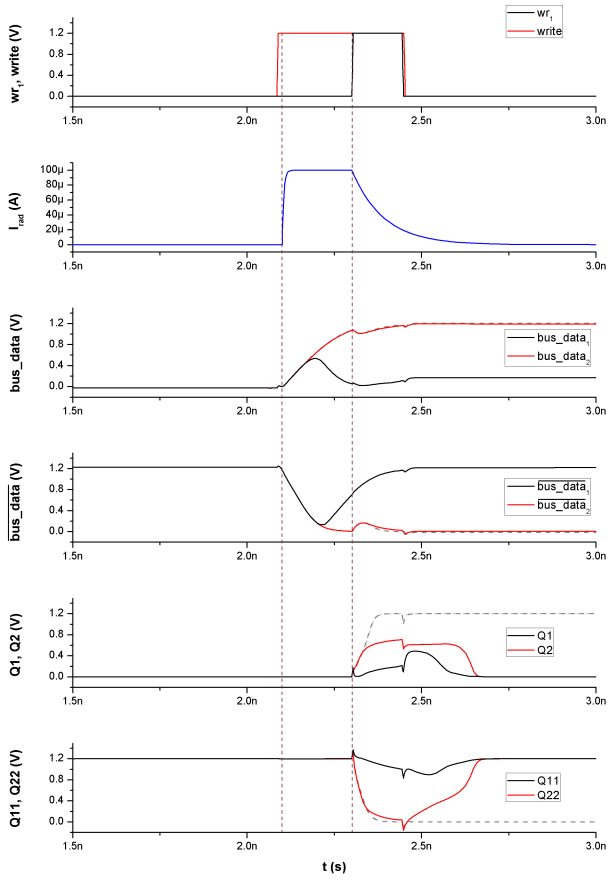

Fig. 4. Simulation of a dynamic fault targeting a DICE cell.

respectively last 140 ps and 360 ps, settings related to a reliable write in error-free operation). The dynamic fault is caused by a current pulse (denoted I_{rad} in Fig. 4) starting shortly after the activation of the $write$ signal: it has an amplitude of 100 μA and a duration of 200 ps. It is induced on the $data\_i_1$ signal and propagates, in the form of SETs, to the bus_data_1 and $\overline{bus\_data_1}$ bit lines (depicted in black[2] in the third and fourth waveforms of Fig. 4). It prevents them from reaching the normal 1.2 V and 0 V voltages they should attain before the activation of wr (the bus_data_2 and $\overline{bus\_data_2}$ bit lines, depicted in red, are not corrupted). As a result, nodes $Q1$ and $Q11$ are almost stuck at their initial 0 V and 1.2 V values during the whole write window (depicted in black in the two bottom waveforms). Though, nodes $Q2$ and $Q22$ (depicted in red) are at first evolving to follow the write value, they finally return to their initial value when the write window closes (wr goes back to 0 V). Note that this dynamic fault phenomenon resembles the SEU mitigation mechanism described in subsection II-C: the voltages of two nodes (here $Q1$ and $Q11$) prevent the DICE cell state from changing.

Two important parameters to characterize how transient current contributes to the induction of a fault are the critical charge (Q_{crit}) and the collected charge (Q_{coll}) [23]. The collected charge is defined by the integral of the transient electric current over time, allowing the calculation of the charge injected in the node of the circuit by the event [23]. The critical charge, in turn, is the minimum collected charge necessary for such a fault to occur [23]. For evaluation purposes and to allow other studies to be carried out from this one, the charge collected in this simulation was calculated, being a value of approximately 28.5 fC. This value is consistent with the collected charge values expected for nano technologies, as can be seen in [24], and it is also a value close to the critical charge, since the simulations were performed using the smallest amplitude of electric current and pulse duration that generated a fault in the circuit.

This simulation shows that a SEE induced at a single node ($data\_i_1$) may induce an error in a SEE-hardened DICE cell if it happens during its writing phase, a so-called dynamic fault. Similar dynamic faults may also be induced when the initial SET arises on node $data\_i_2$ and for a `1` state to `0` state writing of the DICE cell.

IV. Thwarting Dynamic Faults

This section aims to present a countermeasure, named *Holding Block* (HB), which detects and thwarts the effects of such a dynamic error. In a first step, the description of this circuit explains how to detect a disturbance arising during the writing phase. Then, a solution is presented to guaranty the completion of the writing process of the DICE cell. The general overview of this protection circuit inside the memory map is proposed. Finally, simulations demonstrate the positive effect of HB.

A. Countermeasure Description

In the previous section, we demonstrated how a SET induced during the writing phase, may result into creating a dynamic fault that corrupts the DICE memory cell. Here, a countermeasure is presented to fight against this weakness. Its underlying principle is to take advantage of the transient nature of SEEs by extending the write window beyond the perturbation duration (by an amount of time sufficient to ensure the correct completion of the write process). The whole protection circuit is depicted in figure 5. To strengthen the memory, we first need to detect the dynamic fault. To that end, a XOR gate between bus_data_1 and bus_data_2 is used to raise an $alarm$ signal if there is a difference between the states of the bus wires.

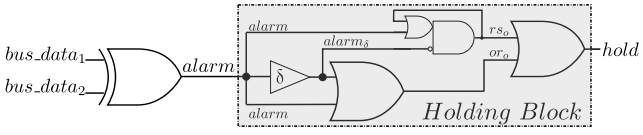

Fig. 5. Architecture of the Holding Block Circuit.

HB has one input, the $alarm$ signal and one output, the $hold$ signal. It has to increase the $write$ and wr signals until

[2]The simulation results of a SEE-free simulation are also depicted in dashed gray lines in Fig. 4 for illustration purposes.

the attack ends (i.e. $alarm$ returns to zero) and until that the selected memory cell is written to the expected value. So, the $hold$ signal needs to stay at high level even after the $alarm$ signal has been raised and pulled down (its duration is that of the transient perturbation). Simulations of two cases of how the $hold$ signal is built in the HB block are displayed in figure 6. A delay element δ is used to generate a delayed image of the alarm: $alarm_\delta$.

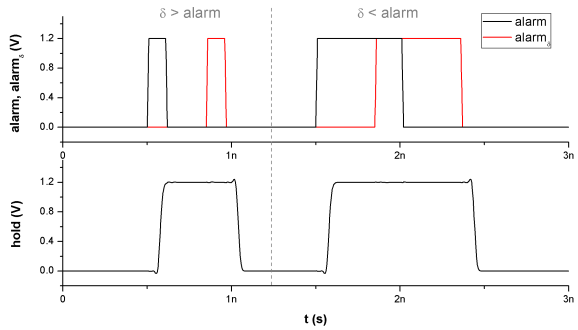

Fig. 6. Simulation of the HB response for different alarm durations.

Two cases have to be considered:

- First, the case of an alarm signal that is longer than δ (as reported in the right part of Fig. 6). Combining $alarm$ and $alarm_\delta$ with an OR gate, signal or_o is obtained which shape is a pulse of a duration equal to the duration of $alarm$ added to δ (passed on to $hold$ through another OR gate).
- The second case may arise if the alarm signal is shorter than δ (drawn in the left part of Fig. 6). In this case, or_o has a two pulses shape that cannot be used to extend the write window. We used a simple RS OR-AND latch circuit to build the rs_o signal and to cover this second case. The obtained signal rs_o produced a suitable $hold$ signal when ORed with or_o.

In both cases, the $hold$ signal keeps a high logical level that may be used to extend the wr and $write$ pulse durations inside the RAM memory. The next subsection describes the insertion of the HB block inside the memory.

B. Countermeasure insertion inside the memory block

Figure 7, describes how to insert two *Holding Block* circuits in the DICE-based RAM memory. As we have two duplicated data buses, ($bus\_data_{1,2}$) and ($\overline{bus\_data_{1,2}}$), an HB circuit is needed for each one. Each bus has its own fault detector, producing signals $alarm_1$ and $alarm_2$. Then, $hold_1$ and $hold_2$ signals are looped back inside all the previous wr and $write$ signals. This combinatorial function is done with the two three-inputs OR gates. In normal functioning (i.e. SEE-free), the writing process is guaranteed by the original writing signals $write$ and wr. When a SEE occurs, depending on which bus is targeted, $hold_1$ or $hold_2$ will increase the write time window of the memory cell in order to write the correct value inside the DICE cell.

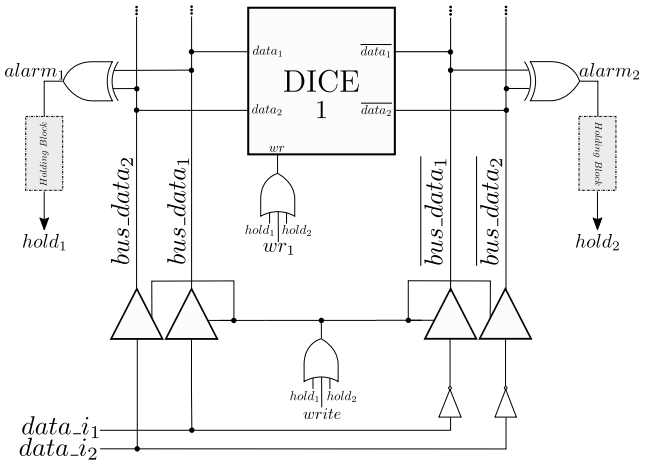

Fig. 7. HB insertion in the DICE based memory.

C. Simulation of the dynamic fault countermeasure

Figure 8 reports the simulation results obtained after updating our design with the HB countermeasure (as exposed in Fig. 7). We considered the same settings as in subsection III-B: an SEE that prevented the DICE cell from being written (from state 0 to state 1).

The radiation-induced transient current, I_{rad}, starts at 2.1 ns with a 100 μA peak current and a 200 ps duration (identical to the I_{rad} of Fig. 4). From the onset of this SEE up to 360 ps later (the normal error-free duration of the $write$ signal), the bit line signals and the internal nodes of the DICE evolve in an identical way as in Fig. 4. From that point, the $write$ and wr signals stay activated thanks to the $hold_{1,2}$ signals for a duration equal to the SEE duration (200 ps in this instance) added to δ (we set δ equal to the activation duration of wr). As a result, the write window is increased in order to allow for the write process to be completed without any error: the DICE cell goes to state 1. This behavior can be observed on signals bus_data_1, $\overline{bus\_data_1}$, $Q1$, $Q11$, $Q2$, and $Q22$. For illustration purposes, the dashed gray waveforms in Fig. 8 reproduce the dynamic fault case.

Note that the $alarm_{1,2}$ signals are also used to indicate at higher abstraction level that the write process lasts longer than usual (it may be necessary to delay a subsequent write operation).

V. Conclusion

The results presented in this article reveal an original dynamic fault mechanism in the architecture of the DICE radiation-hardened cell: the simulations we performed made it possible to induce a dynamic-fault preventing the correct writing of data in the memory cell. As an improvement alternative, a circuit was proposed to detect and prevent the induction of the faults seen here. The performed simulations indicate an adequate functioning of the proposed mitigation circuit as an additional countermeasure to the system.

This first study opens doors for carrying out experimental tests and new studies using multi-physics approach, both in

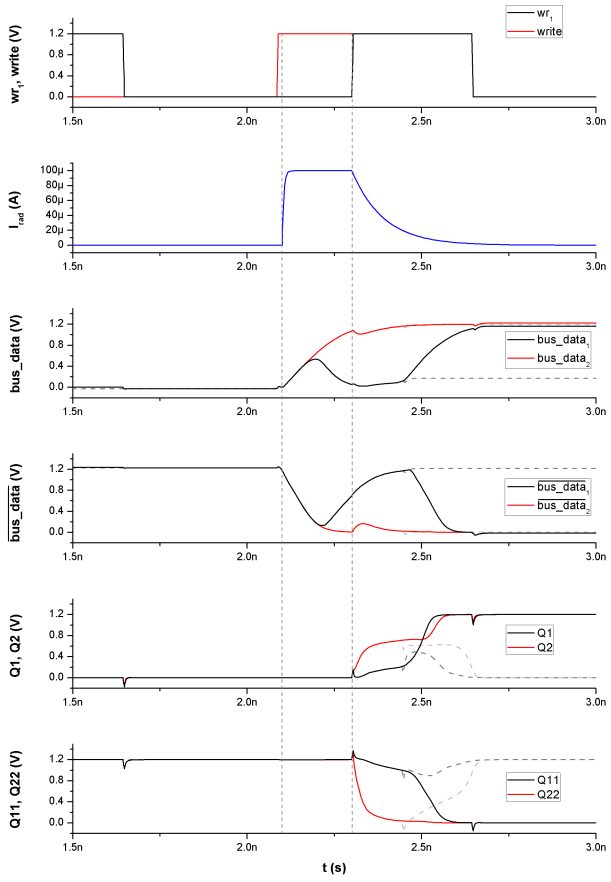

Fig. 8. Simulation of the DICE test bench with countermeasures.

relation to the injection of dynamic-faults in the DICE cell, as well as for a better evaluation of the additional circuit proposed as a countermeasure (a 65 nm CMOS ASIC embedding DICE cells was manufactured). These studies together can validate the data presented here and contribute to the development of electronic systems more robust to failures by SEE.

ACKNOWLEDGMENT

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