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Scalable Analysis Techniques for Microprocessor Performance Counter Metrics

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1 Introduction

Contemporary microprocessors provide a rich set of integrated performance counters that allow application developers and system architects alike the opportunity to gather important information about workload behaviors. These counters can capture instruction, memory, and operating system behaviors. Current techniques for analyzing data produced from these counters use raw counts, ratios, and visualization techniques to help users make decisions about their application source code.

While these techniques are appropriate for analyzing data from one process, they do not scale easily to new levels demanded by contemporary computing systems. Indeed, the amount of data generated by these experiments is on the order of tens of thousands of data points. Furthermore, if users execute multiple experiments, then we add yet another dimension to this already knotty picture. This flood of multidimensional data can swamp efforts to harvest important ideas from these valuable counters.

Very simply, this paper addresses these concerns by evaluating several multivariate statistical techniques on these datasets. We find that several techniques, such as statistical clustering, can automatically extract important features from this data. These derived results can, in turn, be feed directly back to an application developer, or used as input to a more comprehensive performance analysis environment, such as a visualization or an expert system.

2 Microprocessor Hardware Performance Counters

Modern microprocessors include integrated hardware support for non-intrusive monitoring of a variety of processors and memory system events, commonly referred to as hardware counters [3, 9]; this capability is very useful to both computer architects [2] and applications developers [15]. These counters fill a gap that lies between detailed microprocessor simulation and software instrumentation. Software instrumentation can introduce perturbation into an application and the measurement process itself. On the other hand, these counters have relatively low perturbation and can provide insightful information about processor and memory-system behavior. Even though this information is statistical in nature, it does provide a window into certain behaviors that are realistically impossible to gather otherwise. For instance, on IBM's Power3 microprocessor, these events include various categories of instructions, cache misses, branch predictions, memory coherence operations, and functional unit utilization.

Several tools and microprocessors have added additional functionality to simple event counting. Intel's Itanium processors [6] have features that allow monitoring based

on an instruction address range, a specific instruction opcode, a data address range, and/or the privilege level. In addition, the Itanium supplies event address registers that record the instruction and data addresses of data cache misses for loads, the instruction and data addresses of data TLB misses, and the instruction addresses of instruction TLB and cache misses.

DEC/Compaq implemented another useful strategy for hardware counters: instruction sampling within the microprocessor. Using this approach, a performance-monitoring tool, such as ProfileMe [4] or DCPI [1], could arbitrarily choose to measure performance characteristics as they flowed through the processor pipeline. The tool could, then, gather this information over the execution of an application and attribute performance problems to certain instructions.

```
call f_start_section(1,0,ierr)
call hydxy( ddd, ddd1, ithread)
call deltat(" Finished X sweep",2)
call f_end_section(rank, 1,0,ierr)
BARRIER
call flag_clear
BARRIER
call f_start_section(2,0,ierr)
call hydyz( ddd1, ddd, ithread)
call deltat(" Finished Y sweep",2)
call f_end_section(rank, 2,0,ierr)
BARRIER
call flag_clear
```

Figure 1: Sample code segment from function runhyd3 of sPPM.

2.1 Counting Hardware Events

Our approach to using hardware counters rests on bracketing targeted code regions with directives that program the counters to capture events of interest, start and stop the counters, and store the counter values. Users can insert these directives several ways: manually or by using a compiler, a binary editor, or dynamic instrumentation. Hardware counters do require the appropriate operating system and library support to attribute counts appropriately to the proper processes and threads.

G: Instrumentation ID	P: MPI Task	S: Instance	Counter value							
			1	2	3	4	5	6	7	8
1	1	1	8305760504	7795651387	2265349817	14689488	72993923	3744267304	2123235784	1253921843
1	1	2	8233114700	7587713598	2257442295	8987587	72816919	3612932116	2100752913	1260163691
1	2	1	8197360363	7701750765	2233070347	14695959	73425197	3736956914	2075722824	1237231534
1	2	2	8135138668	7593760051	2207456335	9172755	73699055	3590374684	2060311042	1230463969
2	1	1	8326329304	7559198564	2401195595	14583869	72382972	3717326869	2078653081	1233604083
2	1	2	8291791110	7421248463	2334628952	8509892	72074918	3540521698	2060023498	1230670879
2	2	1	8405106757	7645055689	2415396992	14655896	72785214	3708798229	2104739801	1248538508
2	2	2	8381061956	7523753702	2377276028	8606055	72608329	3553288776	2084495857	1256915516

Table 1: Counter values from code segment.

Figure 1 shows a code segment from sPPM [11] that has been instrumented with high level library routines written on top of MPX [10] and PAPI [3] in order to capture eight hardware counter values: total processor cycles, total instructions, cycles stalled waiting

for memory accesses, floating point divide instructions, L1 cache misses, floating point instructions, load instructions, and store instructions.

As Figure 1 illustrates, every execution of this sequential code segment will generate one instance of counter values for each MPI task. Therefore, applications that execute this code segment millions of times will generate millions of instances of counter values. Table 1 shows the raw counter value table that is generated from the code segment in Figure 1, using two MPI tasks. The *G* column lists the instrumentation identifiers that represent different regions of the code. The *S* column lists instances of these regions. Clearly, in real experiments, this data management problem can become intractable!

3 Multivariate Statistical Techniques for Performance Data

As we illustrated in Section 2, each instrumentation point for an application can generate a vast number of hardware counter values. Multiple experiments can aggravate this issue even further. To analyze this data, we turn to multivariate statistical techniques to help focus the user's attention on the important metrics and the distribution of those metrics.

3.1 Performance Metric Spaces

For further analysis, we model these values as points in a multidimensional space. To make this notion more formal, consider a set of k dynamic performance metrics, hardware counters in our case, measured on a set of P parallel tasks, on a set of g instrumentation regions, and on s samples. Abstractly, one can then view these events as defining a collection of these points that describe parallel system characteristics. Following [14], if R_i denotes the range of metric k, we call the Cartesian product

$$M = R_1 \times R_2 \times \ldots \times R_k$$

a performance metric space. Thus, the ordered k-tuples

$$(v_1 \in R_1; v_2 \in R_2; \ldots ; v_k \in R_k) \qquad (1)$$

are points in M. It is important to note that this definition of the metric space does not include the dimensions of instrumentation identifier, parallel task identifier, or measurement instance. Furthermore, this model assumes that this higher-dimension data can be down-sampled into this space as appropriate. For instance, we collect all the points for one instrumentation region across all tasks and across all measurements and then project it into this metric space. This situation would generate $k \times P \times s$ points. While this trivial example illustrates our formalization, we expect to use our techniques on much larger systems where $k > 10$, $g > 10$, $P >> 10$, and $s >> 10$.

The goal of our analysis techniques is now clear; we must reduce this massive number of measurement points and the dimensionality of the metric space to a comprehendible scale. Traditional multivariate statistical techniques warrant investigation as vehicles for understanding this data. In fact, projection pursuit [14] and clustering [12] have been applied to understanding real-time performance data; this previous work strongly suggests that such techniques will be useful for managing hardware counter data. These multivariate statistical techniques allow users to draw inferences from observations with multiple variables (dimensions) and they include dimension reduction and classification.

3.2 Data Preparation

Raw data as generated by reading the hardware counters directly can provide useful information; however, in the context of performance analysis, derived metrics are important. For example, the raw metric for number of cycles supplies a useful estimate of how long a code region executed; however, the derived metric of number of instructions divided by the number of cycles (IPC or instructions per cycle) can directly emphasize code regions that are performing poorly. On the other hand, raw metrics are necessary to help gauge the overall importance of code regions per se. For instance, the IPC of a code region that accounts for only minuscule numbers of cycles during the application execution is irrelevant.

3.3 Clustering

Clustering is a rudimentary, exploratory technique that is helpful in understanding the complex nature of multivariate relationships [7]. It provides a familiar means for assessing dimensionality, detecting outliers, and suggesting attractive hypotheses about relationships between the data. Cluster analysis makes no assumptions about the number of clusters or the cluster structure. It relies only on a metric that calculates the similarities or distances between data points. There have been a wide variety of clustering algorithms proposed. Major differences are whether particular methods simply partition data points into a given number of groups or build more complicated cluster (or data point) hierarchies.

In the context of hardware counter data, we propose both hierarchical and non-hierarchical methods will help users identify equivalence classes of data points and an 'important' subset of entire performance metrics that make more contribution to the existence of those classes.

We demonstrate how hierarchical algorithms give users insights about overall cluster structure of a data set by means of dendrogram, while nonhierarchical methods, such as the k-means algorithm, provide an efficient method to explain the importance of each metric on a cluster configuration by using F-ratio of each metric (Section 4.4). F-ratio is a technique for univariate analysis of variance that is defined as $\frac{Between-ClusterVariablity}{Within-ClusterVariablity}$. Hence, metrics that vary greatly among different clusters and remain the same in the same cluster yields higher F-ratio.

K-means and F-ratio can also be employed when the decision on number of clusters is not obvious. This situation happens often when users do not have reasonable prior knowledge about target application's behavior. K-mean and F-ratio methods provide a means by which a system can automatically partition data points into a number of clusters as to maximize the between-cluster variability relative to the within-cluster variability.

3.4 Factor Analysis

Factor analysis is a multivariate technique that makes it possible to describe the covariance relationships among many variables in terms of a few underlying quantity, factors. In the context of hardware counter space, we propose it will reduce the dimensionality of our performance metric space, $M = [R_1 \times R_2 \times ... \times R_k]$, by assembling highly correlated metrics in a peer group while separating uncorrelated ones into the other groups. (e.g. $[R_a, R_b, R_c]$, x$[R_d]$x...x $[R_i, R_j\ R_k]$). This grouping can guide users to choose a right set of metrics for refining their code optimization efforts.

In the factor analysis model, our metrics space M can be rewritten as

$$R_1 - \upsilon_1 = l_{11}F_1 + l_{12}F_2 + \ldots + l_{1m}Fm + \varepsilon_1$$
$$R_2 - \upsilon_2 = l_{21}F_1 + l_{22}F_2 + \ldots + l_{2m}Fm + \varepsilon_2$$
$$\vdots$$
$$R_p - \upsilon_p = l_{p1}F_1 + l_{p2}F_2 + \ldots + l_{pm}Fm + \varepsilon_p$$

Where F_i is i^{th} common factor, R_j j^{th} metrics, υ_k mean of R_j, and coefficient l_{ji} is the loading of R_j on the factor F_i. As this notation suggests, grouping R's that have higher loadings for a particular F will yield a group whose R's are highly correlated.

3.5 Principal Component Analysis

define.

4 Evaluation

We empirically evaluated our techniques on an operational prototype with two applications. We scale each application up to 128 tasks. As Figure 1 illustrates, we first instrument the application and collect hardware counter data on the target platform. We then clean, merge, and prepare this data for statistical analysis. Next, we apply several statistical techniques to the prepared data. In the future, we expect to feed the results from these analyses into a comprehensive performance analysis environment or automated performance tool.

4.1 Instrumentation and Data Collection

We manually instrument our target applications with source code annotations. Each instrumentation point identifies a code region to capture hardware counter metrics as Figure 1 illustrates. Hence, each application has g instrumented code regions as defined in Section 3.1. For these experiments, we assume that each region captures the same set of k hardware metrics.

In this framework, our tool can either write the each sample for each region to a tracefile during execution or accumulate the samples for each region and write the accumulated metrics to a file at termination. In the former context, tracefiles would grow at a rate proportional to $k \times g \times s$ for each parallel task. We implemented both modes, but still, we use the latter technique, which generates only $k \times g$ measurement points for each parallel task, here to prevent an explosion of data and measurement overhead in the application. Our statistical techniques remain valid for accumulated data; however, this selection has the drawback that accumulated measurements can hide certain performance phenomena.

At termination of the application experiment, each parallel task P generates a local file. Our prototype merges these P local files into one global file, containing all accumulated measurements for an application, and having size proportional to $k \times g \times P$. With all these raw metrics for one application now in one file, we can easily apply our statistical techniques to this file with a filter. This filter also manipulates the raw metrics for data cleaning and generating useful derived metrics as described in Section 3.2.

4.2 Platform

We ran our tests on an IBM SP system, located at Lawrence Livermore National Laboratory. This machine is composed of sixteen 222 MHz IBM Power3 8-way SMP nodes, totaling 128 CPUs. Each processor has three integer units, two floating-point units, and two load/store units. Its 64 KB L1 cache is 128 way associative with 32 byte cache lines and L1 uses a round-robin replacement scheme. The L2 cache is 8 MB in size, which is four-way set associative with its own private cache bus. At the time of our tests, the batch partition had 15 nodes and the operating system was AIX 4.3.3. Each SMP node contains 4GB main memory for a total of 64 GB system memory. A Colony switch--a proprietary IBM interconnect--connects the nodes. We compiled the various tests with the IBM XL and KAI Guide compilers using IBM's MPI library in user-space mode. Our test jobs ran on dedicated nodes, although other jobs were concurrently using the network.

4.3 Applications

We evaluate our proposed techniques on two scalable applications. Each application has different computational and communication characteristics [13]. SPPM, for example, has large blocks of floating point computation with infrequent, large messages, while SMG2000 is at the other end of the spectrum, having frequent, small messages with smaller blocks of computation.

sPPM [11] solves a 3-D gas dynamics problem on a uniform Cartesian mesh, using a simplified version of the Piecewise Parabolic Method. The algorithm makes use of a split scheme of X, Y, and Z Lagrangian and remap steps, which are computed as three separate sweeps through the mesh per timestep. Message passing provides updates to ghost cells from neighboring domains three times per timestep. OpenMP provides thread-level parallelism within MPI tasks.

Sweep3D [5, 8] is a solver for the 3-D, time-independent, particle transport equation on an orthogonal mesh and it uses a multidimensional wavefront algorithm for "discrete ordinates" deterministic particle transport simulation. Sweep3D benefits from multiple wavefronts in multiple dimensions, which are partitioned and pipelined on a distributed memory system. The three dimensional space is decomposed onto a two-dimensional orthogonal mesh, where each processor is assigned one columnar domain. Sweep3D exchanges messages between processors as wavefronts propagate diagonally across this 3-D space in eight directions.

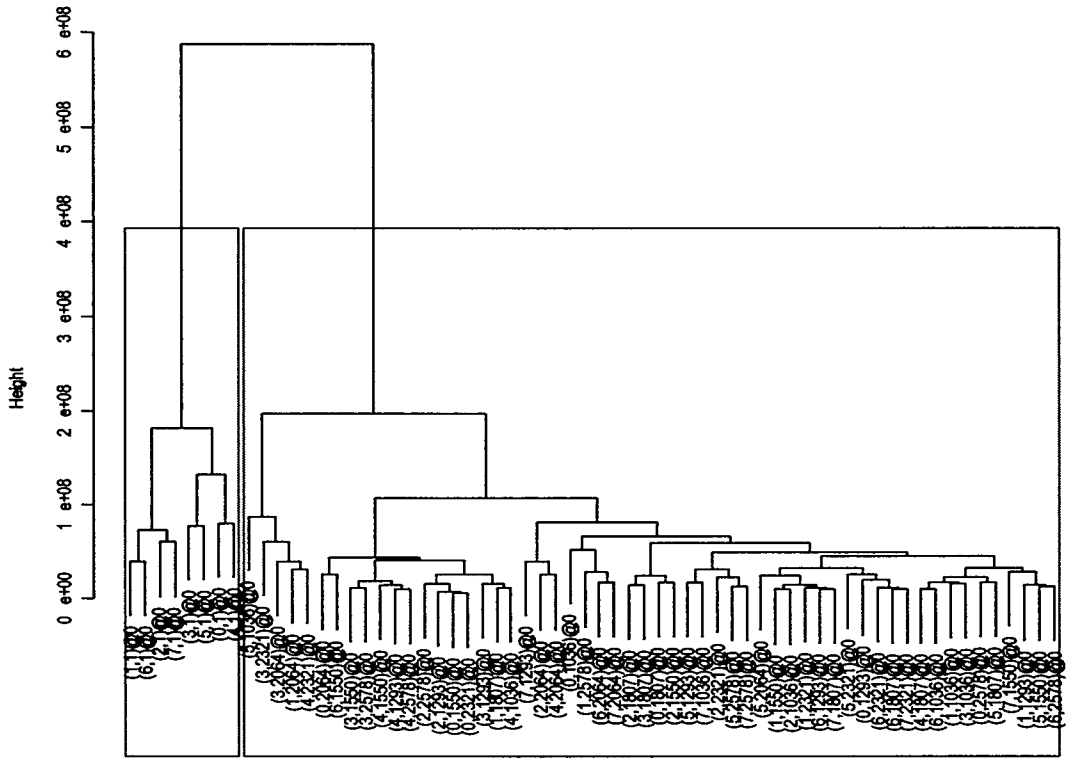

Figure 2: Dendrogram for a section of sPPM using raw metrics.

4.4 Clustering

4.4.1 Agglomerative Hierarchical Method

This method gives users insights about overall cluster structure that exist in a data space by constructing dendrograms. Figure 2 shows the dendrogram for one instrumented section of an sPPM experiment with 8 MPI tasks and 8 OpenMP threads per task. Since sPPM exploits parallelism with message passing for inter-node communication and OpenMP within shared memory for thread level parallelism, it is expected to have at least two natural clusters. AHM clearly identifies in Figure 2 the existence of two classes; one housing all 56 slave threads and the other cluster containing the 8 master threads.

Figure 3 illustrates the dendrogram of the same section of sPPM using derived metrics. As expected, the configuration does not change much from Figure 2, suggesting that the two clusters are performing similarly and any changes to code for either the master thread or the slave thread will propagate to its peers. Statistical techniques only with raw metrics would not immediately provide this type of perspectives.

Figure 4 shows the dendrogram for the raw metrics of a section of Sweep3d for an experiment using 64 MPI tasks. In this case, three clusters are sufficiently different. Our initial results show that because Sweep3d decomposes the global 3-D problem onto a 2-D orthogonal mesh for processor assignment, the assignment creates two different equivalence classes: one for internal processors (right), and one for corner and edge processors (center and left). Other techniques, such as projecting clusters (and data points) into principal component space, should be used to identify cluster configuration.

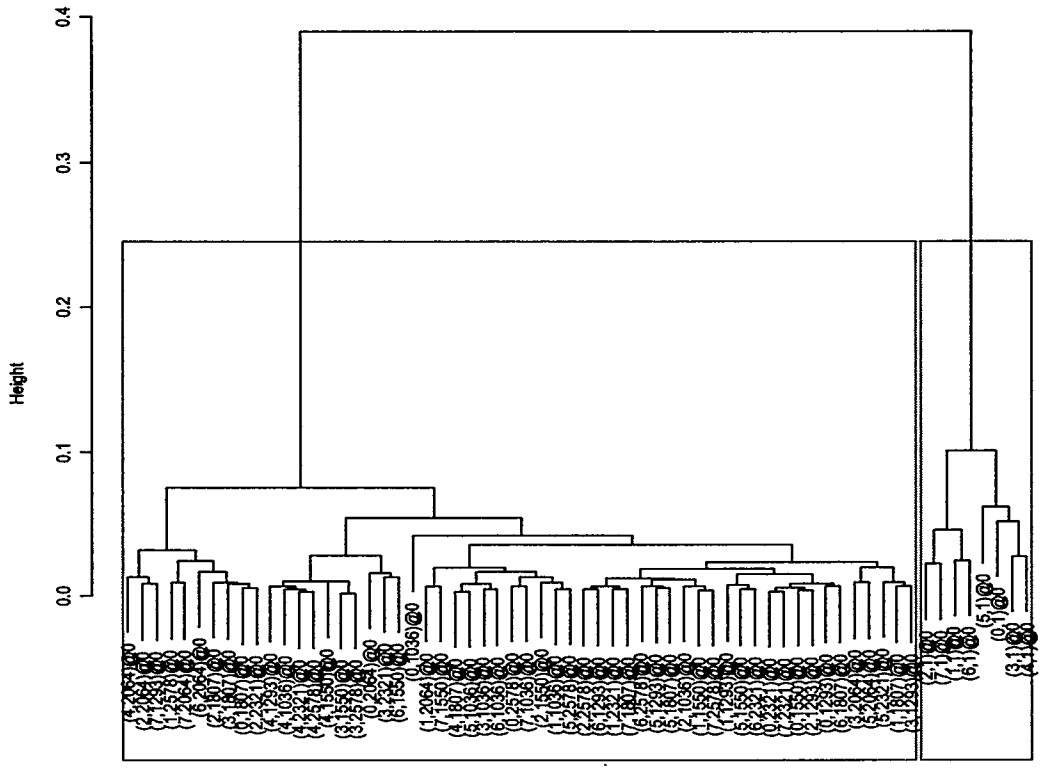

Figure 3: Dendrogram for a section of sPPM using derived metrics

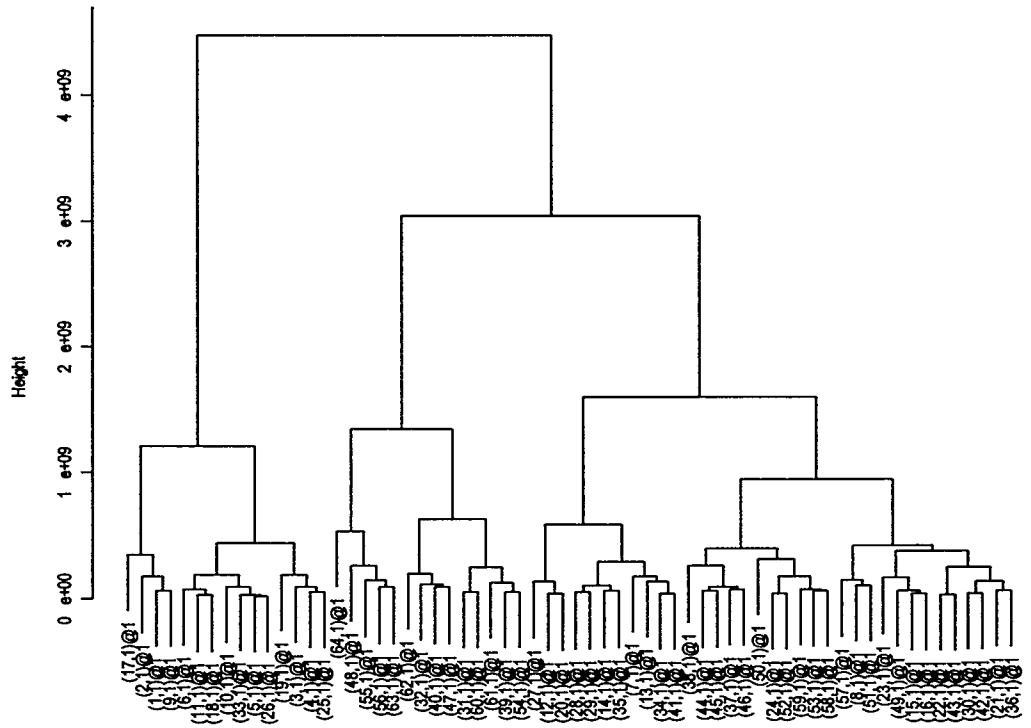

Figure 4: Dendrogram for sweep section of sweep3d using raw metrics.

4.4.2 k-means clustering and F-ratio

While AHM gives a general idea about cluster structure, it is not entirely convenient to compare clusters and compute the importance of an individual metrics that yield the particular cluster configuration. Using k-means clustering and F-ratios, we ordered metrics for the same section on sPPM by their F-ratio in Table 2. It suggests that PAPI_MEM_SCY (Cycles Stalled Waiting for Memory Access), PAPI_SR_INS (Store instructions executed), and PAPI_L1_TCM (L1 total cache misses), are the three major reasons that we have two distinct clusters.

Metrics	F-ratio
PAPI.MEM.SCY	**7.914255**
PAPI.SR.INS	**5.124050**
PAPI.L1.TCM	**5.097693**
PAPI.TOT.IIS	3.488066
PAPI.LD.INS	3.473341
PAPI.FP.INS	2.498332
PAPI.TOT.CYC	1.673567
PAPI.FDV.INS	0.161107

Table 2: Metrics ordered by F-ratio size for a section of sPPM.

4.5 Factor Analysis

Table 3 shows the result of factor analysis on the same section of sPPM. Each column represents loadings of metrics for each factor. As it suggests, it is reasonable to group together those metrics with bigger loadings per column.

Metric	Factor1	Factor2	Factor3
PAPI.LD.INS	**-0.658**	**0.519**	**0.541**
PAPI.BR.PRC	0.000	0.000	**0.792**
PAPI.L1.DCM	**0.969**	0.13	-0.161
PAPI.FXU.IDL	-0.244	**0.883**	-0.290
PAPI.BTAC.M	**0.799**	0.000	0.324
PAPI.FP.INS	**-0.974**	0.199	0.000
PAPI.MEM.WCY	**0.957**	0.000	0.000
PAPI.SR.INS	0.000	**0.690**	0.000

Table 3: Factor Analysis of sPPM (with three factors assumed).

By setting a somewhat arbitrary threshold, 0.5, we are able to make four groups: {PAPI.L1.DCM, PAPI.BTAC.M, PAPI.FP.INS, PAPI.MEM.WCY}, {PAPI.FXU.IDL, PAPI.SR.INS}, {PAPI.BR.PRC} and PAPI.LD.INS. We verified the metrics in the same group are highly correlated by scanning correlation matrix. Users can now select a representative metric per group for the further analysis.

5 Conclusions

Scalable computing platforms will generate tremendous volumes of performance data, especially when monitoring low-level, frequent events like those produced by microprocessor performance counters. Developers will need new techniques to help them gain insight into this massive dataset. Traditional multivariate statistical techniques can

play a prominent role in this effort by reducing the dataset dimensionality and classifying similar datapoints. Our experiments on several applications demonstrate the feasibility of this approach and highlight several useful implementation strategies. For example, our experiments with sPPM and Sweep3d clearly confirmed that clustering on both raw and derived metrics can allow a user to understand the performance implications across all tasks in the application. We hope to feed results from this collection of statistical analysis techniques directly to the user, or to a sophisticated performance analysis system, such as a visualization or an expert system.

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Appendix A: PAPI Power3 Hardware Events

Name	Description
PAPI_L1_DCM	Level 1 data cache misses (PM_LD_MISS_L1,PM_ST_L1MISS)
PAPI_L1_ICM	Level 1 instruction cache misses (PM_IC_MISS)
PAPI_L1_TCM	Level 1 cache misses (PM_IC_MISS,PM_LD_MISS_L1,PM_ST_L1MISS)
PAPI_CA_SNP	Requests for a snoop (PM_SNOOP)
PAPI_CA_SHR	Requests for exclusive access to shared cache line (PM_SNOOP_E_TO_S)
PAPI_CA_ITV	Requests for cache line intervention (PM_SNOOP_PUSH_INT)
PAPI_BRU_IDL	Cycles branch units are idle (PM_BRU_IDLE)
PAPI_FXU_IDL	Cycles integer units are idle (PM_FXU_IDLE)
PAPI_FPU_IDL	Cycles floating point units are idle (PM_FPU_IDLE)
PAPI_LSU_IDL	Cycles load/store units are idle (PM_LSU_IDLE)
PAPI_TLB_TL	Total translation lookaside buffer misses (PM_TLB_MISS)
PAPI_L1_LDM	Level 1 load misses (PM_LD_MISS_L1)
PAPI_L1_STM	Level 1 store misses (PM_ST_L1MISS)
PAPI_L2_LDM	Level 2 load misses (PM_LD_MISS_EXCEED_L2)
PAPI_L2_STM	Level 2 store misses (PM_ST_MISS_EXCEED_L2)
PAPI_BTAC_M	Branch target address cache misses (PM_BTAC_MISS)
PAPI_PRF_DM	Data prefetch cache misses (PM_PREF_MATCH_DEM_MISS)
PAPI_TLB_SD	Translation lookaside buffer shootdowns (PM_TLBSYNC_RERUN)
PAPI_CSR_FAL	Failed store conditional instructions (PM_RESRV_CMPL)
PAPI_CSR_SUC	Successful store conditional instructions (PM_ST_COND_FAIL)
PAPI_CSR_TOT	Total store conditional instructions (PM_RESRV_RQ)
PAPI_MEM_SCY	Cycles Stalled Waiting for memory accesses (PM_CMPLU_WT_LD,PM_CMPLU_WT_ST)
PAPI_MEM_RCY	Cycles Stalled Waiting for memory Reads (PM_CMPLU_WT_LD)
PAPI_MEM_WCY	Cycles Stalled Waiting for memory writes (PM_CMPLU_WT_ST)
PAPI_STL_ICY	Cycles with no instruction issue (PM_0INST_DISP)
PAPI_STL_CCY	Cycles with no instructions completed (PM_0INST_CMPL)
PAPI_BR_CN	Conditional branch instructions (PM_CBR_DISP)
PAPI_BR_MSP	Conditional branch instructions mispredicted (PM_MPRED_BR_CAUSED_GC)
PAPI_BR_PRC	Conditional branch instructions correctly predicted (PM_BR_PRED)

PAPI_FMA_INS	FMA instructions completed (PM_EXEC_FMA)
PAPI_TOT_IIS	Instructions issued (PM_INST_DISP)
PAPI_TOT_INS	Instructions completed (PM_INST_CMPL)
PAPI_INT_INS	Integer instructions (PM_FXU0_PROD_RESULT,PM_FXU1_PROD_RESULT,PM_FXU2_PROD_RESULT)
PAPI_FP_INS	Floating point instructions (PM_FPU0_CMPL,PM_FPU1_CMPL)
PAPI_LD_INS	Load instructions (PM_LD_CMPL)
PAPI_SR_INS	Store instructions (PM_ST_CMPL)
PAPI_BR_INS	Branch instructions (PM_BR_CMPL)
PAPI_FLOPS	Floating point instructions per second (PM_CYC,PM_FPU0_CMPL,PM_FPU1_CMPL)
PAPI_TOT_CYC	Total cycles (PM_CYC)
PAPI_IPS	Instructions per second (PM_CYC,PM_INST_CMPL)
PAPI_LST_INS	Load/store instructions completed (PM_LD_CMPL,PM_ST_CMPL)
PAPI_SYC_INS	Synchronization instructions completed (PM_SYNC)
PAPI_FDV_INS	Floating point divide instructions (PM_FPU_FDIV)
PAPI_FSQ_INS	Floating point square root instructions (PM_FPU_FSQRT)

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