Security, Performance and Energy Implications of Hardware-assisted Memory Protection Mechanisms on Event-based Streaming Systems

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I. HARDWARE-ASSISTED MEMORY PROTECTION MECHANISMS

Major cloud providers such as Amazon [1], Google [2] and Microsoft [3] provide nowadays some form of infrastructure as a service (IaaS) which allows deploying services in the form of virtual machines [4], containers [5] or bare-metal [6] instances. Although software-based solutions like homomorphic encryption exit, privacy concerns [7] greatly hinder the deployment of such services over public clouds. It is particularly difficult for homomorphic encryption to match performance requirements of modern workloads [8]. Evaluating simple operations on basic data types with HElib [9], a homomorphic encryption library, against their unencrypted counter part reveals, that homomorphic encryption is still impractical under realistic workloads.

In recent attempts to enable privacy-preserving operations, publish/subscribe systems among other types of communication services have received much attention. Meanwhile, Intel and AMD have introduced hardware-assisted memory protection mechanisms inside x86 processors to provide answers overcoming the limitation of current software-based solutions. With the launch of the Skylake generation, Intel added a new technology called Software Guard Extension (SGX) [10] to their processors. SGX allows applications to create secure enclaves protecting the confidentiality and integrity of data and its associated code during execution. An application has to be signed and shipped as an unencrypted shared library (respectively a shared object on Linux systems) in order to be executed in an enclave. Execution of an enclave on a genuine Intel processor with enabled SGX technology can be ensured by a remote attestation protocol. The enclave is stored in the enclave page cache (EPC) when executed; a limited memory area predefined at boot time. Page eviction is handled by the SGX driver and confidentiality, integrity, replay and tamper protected by the *memory encryption engine* (MEE) [11]. AMD's recently introduced Zen microarchitecture is capable of transparently encrypting memory pages using their novel technologies Secure Memory Encryption (SME) and Secure Encrypted Virtualization (SEV). SME and SEV make use of ephemeral encryption keys required by an AES engine located on the core's memory controller. While SME

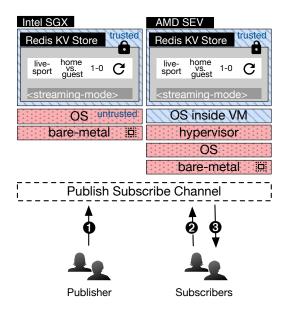


Fig. 1: Architecture of our system and differences when deployed with Intel SGX and AMD SEV-ES. The components with a diagonally hatched pattern on a blue background are trusted, those with a dotted red background are untrusted, respectively. Redis is configured in *streaming-mode* [13].

creates a single key to encrypt the entire system's memory, SEV can generate and assign a key to a limited number of distinct virtual machines and a single hypervisor running on the processor. The creation of the memory keys is delegated to the *secure processor* (SP), an ARM TRUSTZONE-enabled system-on-chip (SoC) embedded on-die [12].

II. ARCHITECTURE

We designed and implemented a simple yet pragmatic eventbased streaming system to evaluate our execution. The core of our system consists of a key-value store with native support to register and trigger callback functions associated to CRUD operations (*i.e.*, create, read, update, delete) on key-value entries. These callback functions implement matching filters for subscribers of a publish/subscribe system, that will receive events upon notification of the channel.

The main components of the event-based streaming system are depicted in Figure 1 with Intel SGX (left) and AMD

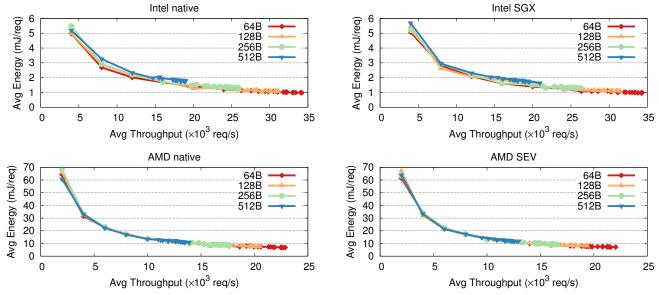


Fig. 2: Macro-benchmark: energy cost of publish/subscribe.

SEV (right). All potentially sensitive components *i.e.*, the key-value store and its content, the callback functions and the endpoints of the publish/subscribe channels, have to be protected by SGX or SEV. However, only the key-value store entries are considered to be protected by SGX or SEV in our implementation. Furthermore, we do not include other additional stages in the processing pipeline nor do we explicitly include broker or broker overlays [14]. Under these carefully controlled conditions side-effects of SGX and SEV can be better highlighted on the main processing node, in particular memory-bound operations and their energy cost.

The workflow of operations is as follows. First, a subscriber manifests its interests by subscribing to the channel (Figure 1-1). Then, publishers start emitting events with a given content, e.g., the results of a sport event (Figure 1-1). As soon as the content is updated, a callback function is triggered (Figure 1-1). Finally, the potential subscriber(s) receive the event (Figure 1-1).

III. IMPLEMENTATION

The architecture was implemented on top of well-known open-source systems and libraries. Redis [15] (v4.0.8), an efficient and lightweight in-memory key-value store, is used as core component. It also features a built-in publish/subscribe system, which is exploited in order to realize our experimental platform. Publishers and subscribers connect to the channels provided by Redis using Jedis [16] (v2.9.0) Java bindings for Redis. The callback system is implemented by leveraging Redis' ability to load external modules [17]. Despite Redis being a single threaded application, modules can be run in a multi-threaded setup.

While applications run under AMD SEV do not require any changes, they do need to be modified under Intel SGX. Graphene-SGX [18] is a library allowing to run unmodified applications inside enclaves and was used for this benchmark.

In order to run unmodified applications under SGX, a manifest file has to be provided to Graphene-SGX specifying the resources, *e.g.*, shared libraries, files, network endpoints, which the enclave is allowed to make use of. The manifest file is pre-processed by an auxiliary tool generating signatures that are later checked by the Graphene loader.

Various workloads were injected using YCSB [19], v0.12.0 commit 3d6ed690, to record latency, throughput, performance and energy values.

IV. EVALUATION

The benchmark measures the latency from the moment a publisher emits a new event until the moment all subscribers receive the content of the event. Four different configurations of the system are evaluated: (i) Intel without SGX protection, (ii) with SGX by leveraging Graphene, (iii) AMD without memory protection and (iv) AMD with SEV. Publishers are configured such that they inject new events at fixed throughputs with fixed message sizes ranging from 64 B up to 512 B.

Measured latencies for smaller message sizes are consistently lower for higher throughputs (requests/second). The cost of serialization reduces the efficiency of our system for larger message sizes. A pairwise comparison of the configurations for Intel and AMD reveals how these memory protection mechanisms are negatively affecting the observed latencies, which is particularly evident for Intel configurations. This observation is further confirmed by bandwidth usage values.

The energy cost of messages send over the publish/subscribe system is shown in Figure 2. As the system begins to occupy a significant amount of the machine's resources, energy consumption begins to increase at a linear rate relative to the target throughput. This behavior is reflected by the decreasing energy cost per message before reaching a minimal energy cost.

Memory requirements do not exceed the available EPC for the Intel configurations under these evaluation settings.

Consequently, the measurements indicate that both memory protection mechanisms consume an even amount of energy compared to their native setup.

Due to the energy being recorded for the entire system using an external power measurement device, it becomes difficult to make an implication on the energy consumption of the memory protection mechanisms. In a next step we are developing tools to measure the energy consumption of precesses at a much finer grained level, for instance the processor's core. Such tools would then give us the opportunity to observe in more detail the influence of memory protection mechanisms on processes and assist in the development of novel security and energy-aware system components.

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